

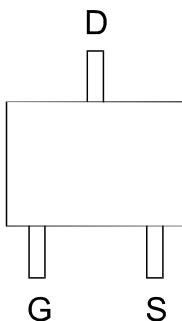
GENERAL DESCRIPTION

The MESS84W is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching and low in-line power loss are needed in a very small outline surface mount package.

PIN CONFIGURATION

(SOT-323)

Top View

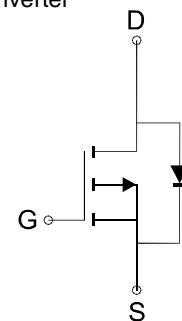


FEATURES

- $R_{DS(ON)} \leq 5\Omega @ V_{GS} = -10V$
- $R_{DS(ON)} \leq 6\Omega @ V_{GS} = -5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter



P-Channel MOSFET

Ordering Information: MESS84W(Pb-free)

MESS84W-G (Green product-Halogen free)

Absolute Maximum Ratings ($T_A=25^\circ C$ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	-60	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain	$T_A=25^\circ C$	I_D	-0.2	A
	$T_A=70^\circ C$	I_D	-0.16	
Pulsed Drain Current		I_{DM}	-0.8	A
Maximum Power Dissipation	$T_A=25^\circ C$	P_D	0.34	W
	$T_A=70^\circ C$	P_D	0.22	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	367	°C/W

*The device mounted on 1in² FR4 board with 2 oz copper



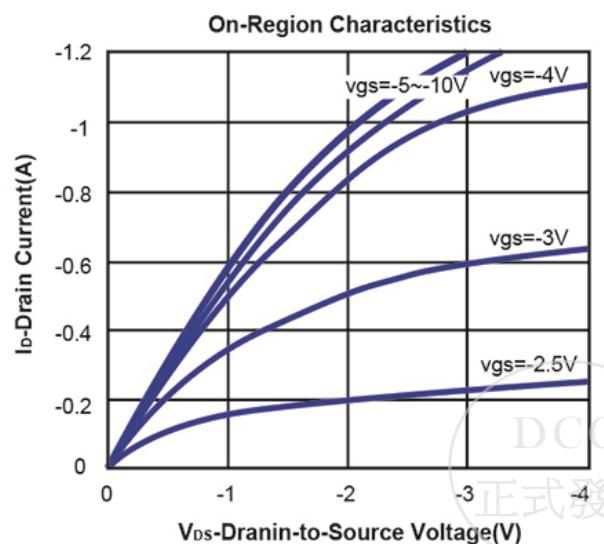
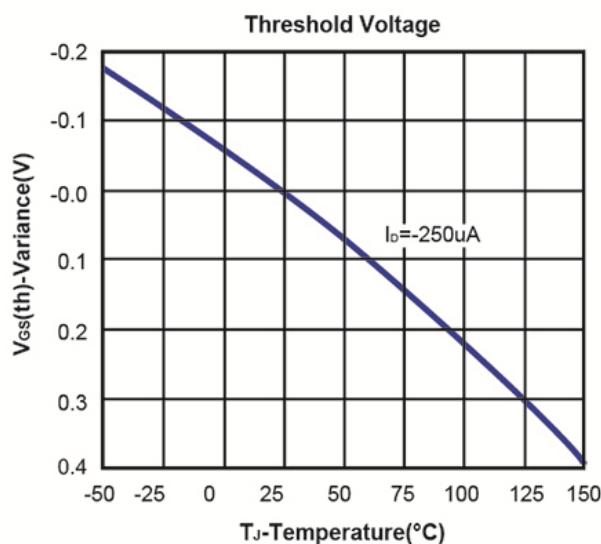
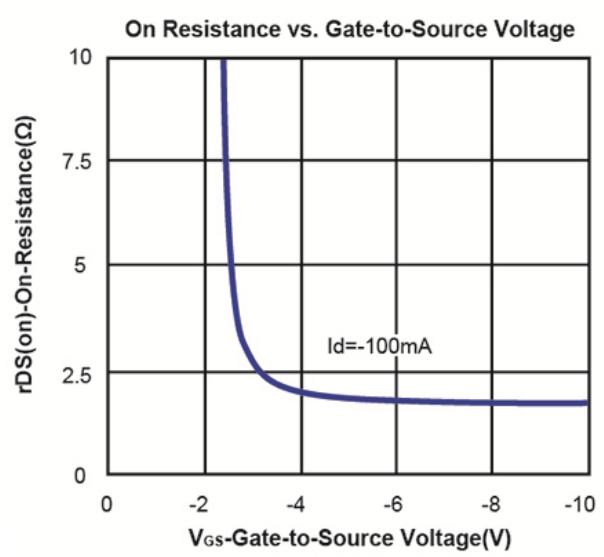
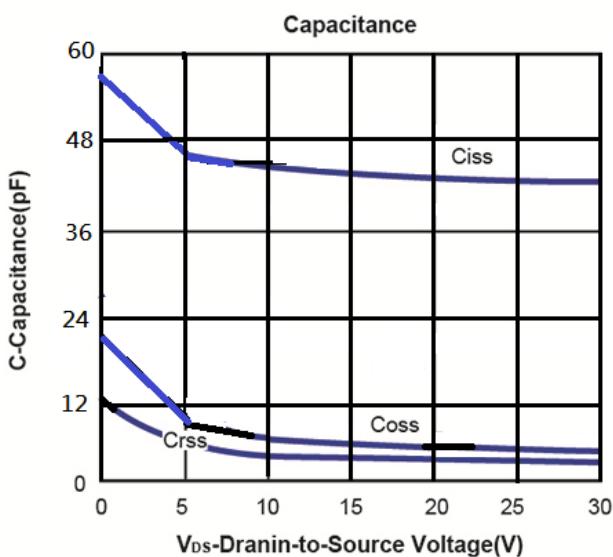
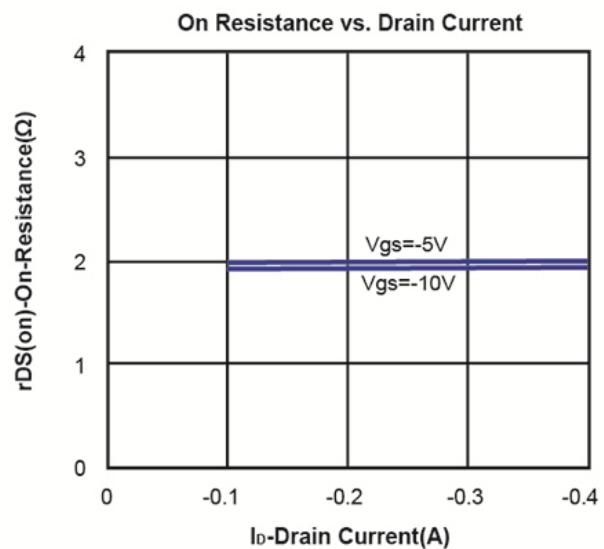
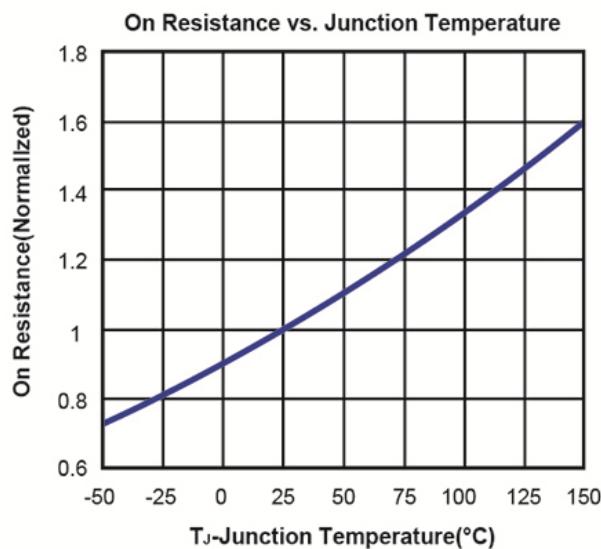
Electrical Characteristics ($T_A = 25^\circ C$ Unless Otherwise Specified)

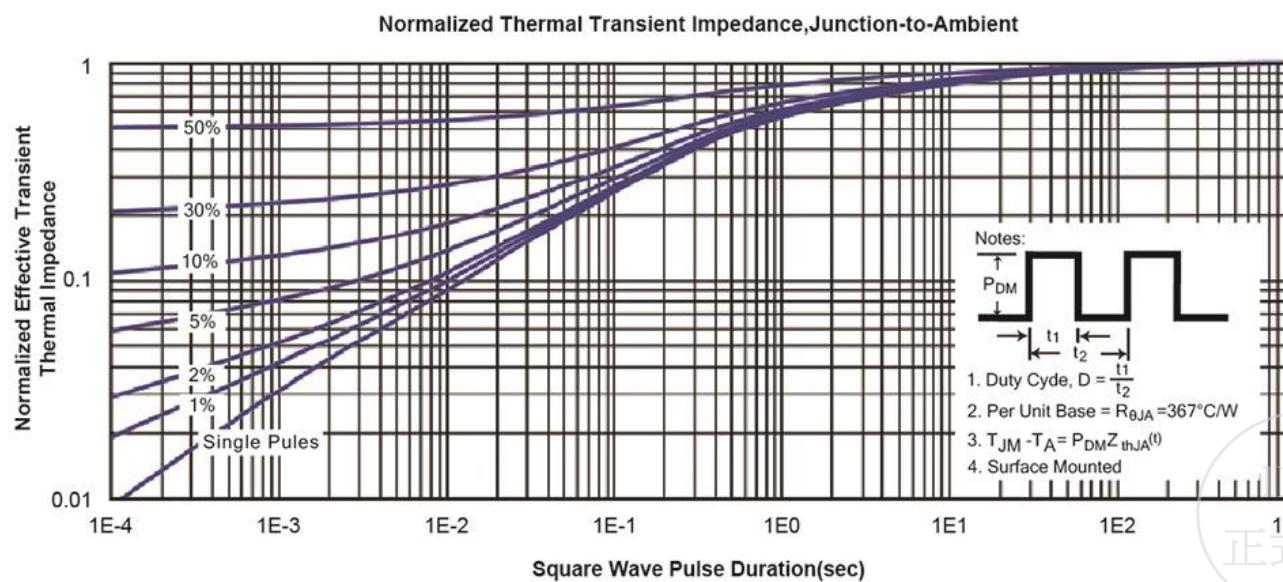
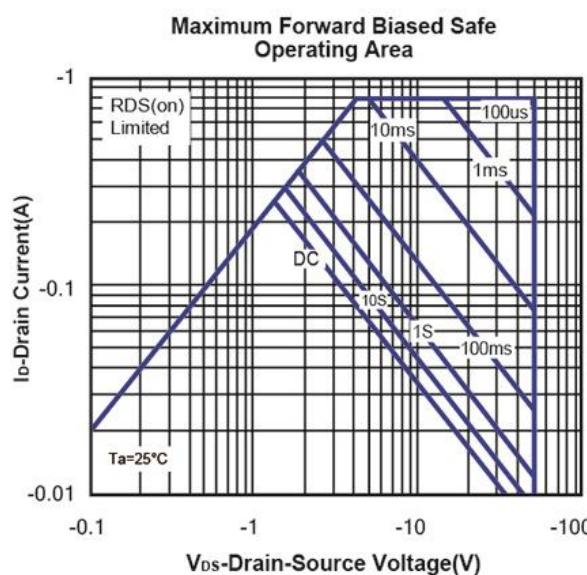
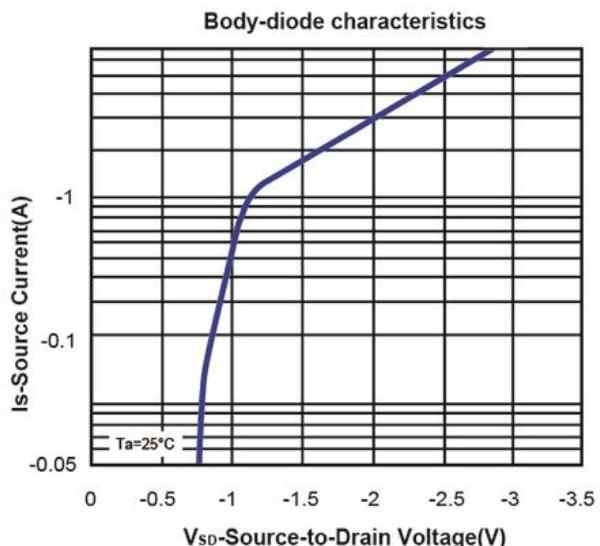
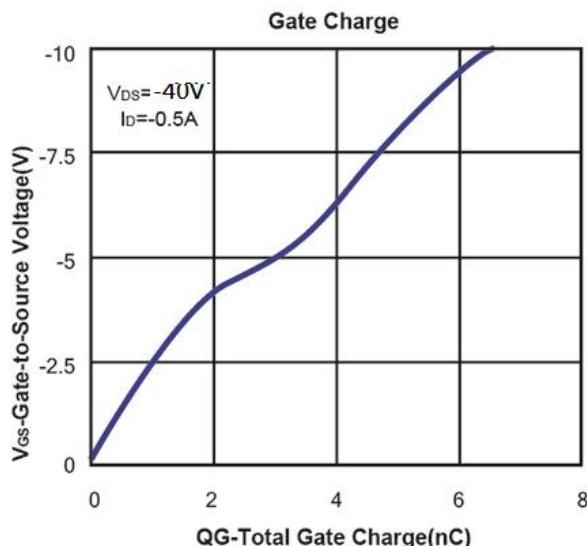
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250 \mu A$	-60			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250 \mu A$	-0.8		-2.0	V
I_{GSS}	Gate Leakage Current	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-60V, V_{GS}=0V$			-1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance	$V_{GS}=-10V, I_D= -100mA$		2	5	Ω
		$V_{GS}=-5V, I_D= -100mA$		2	6	
V_{SD}	Diode Forward Voltage	$I_S=-0.1A, V_{GS}=0V$			-2.9	V
DYNAMIC						
Q_g	Total Gate Charge	$V_{DS}=-40, V_{GS}=-10V, I_D=-0.5A$		6.6		nC
Q_g	Total Gate Charge			2.3		
Q_{gs}	Gate-Source Charge	$V_{DS}=-40, V_{GS}=-4.5V, I_D=-0.5A$		2.4		
Q_{gd}	Gate-Drain Charge			0.7		
C_{iss}	Input Capacitance			42		pF
C_{oss}	Output Capacitance	$V_{DS}=-30V, V_{GS}=0V, f=1MHz$		4		
C_{rss}	Reverse Transfer Capacitance			2		
$t_{d(on)}$	Turn-On Delay Time	$V_{DS}=-15V, R_L = 50\Omega$ $V_{GS}=-10V, R_G=25\Omega$ $I_D=-0.3A$		13.7		ns
t_r	Turn-On Rise Time			6.2		
$t_{d(off)}$	Turn-Off Delay Time			15.9		
t_f	Turn-Off Fall Time			2.8		

Notes: a. Pulse test; pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$

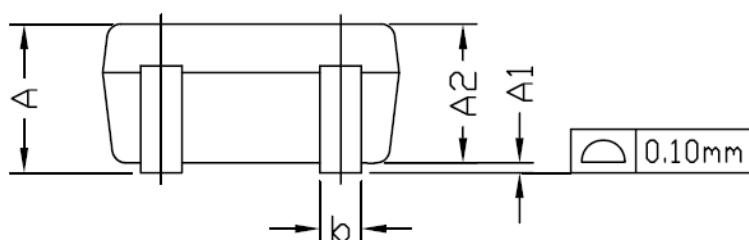
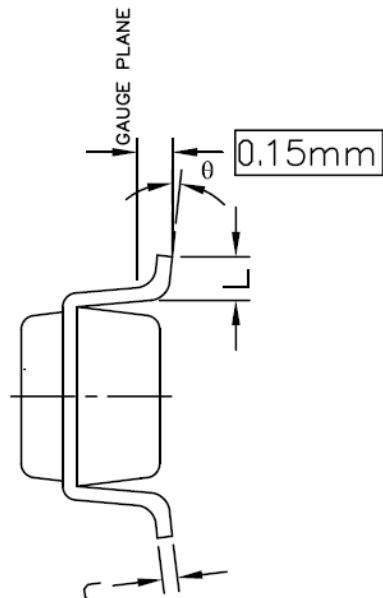
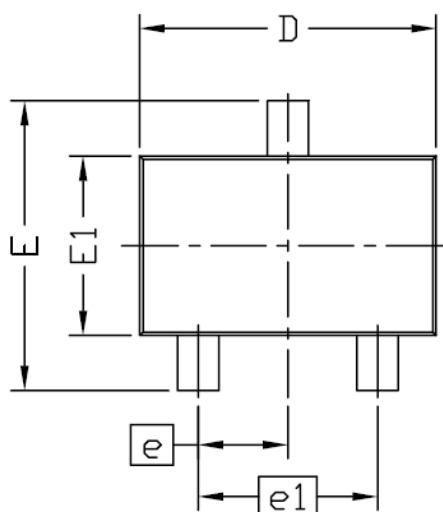
b. Matsuki Electric reserves the right to improve product design, functions and reliability without notice.







SOT-323 Package Outline



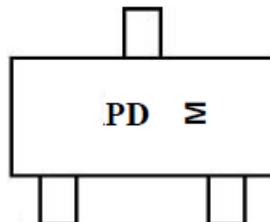
DIM	MILLIMETERS (mm)	
	MIN	MAX
A	-	1.10
A1	0.00	0.10
A2	0.7	1.00
b	0.15	0.30
c	0.08	0.22
D	1.85	2.15
E	1.80	2.40
e	0.65 BSC	
e1	1.30 BSC	
E1	1.1	1.4
L	0.26	0.46
θ	0°	8°



Device name: MESS84W/ MESS84W-G

Package: SOT-323

Marking Code:



PD: Device Marking Code

M: Date code

MONTH CODE

ODD YEARS(2007,2009)

Jan	1
Feb	2
Mar	3
Apr	4
May	5
Jun	6
Jul	7
Aug	8
Sep	9
Oct	T
Nov	V
Dec	C

EVEN YEARS(2006,2008)

Jan	E
Feb	F
Mar	H
Apr	J
May	K
Jun	L
Jul	N
Aug	P
Sep	U
Oct	X
Nov	Y
Dec	Z

