MFE3006 (SILICON)
thru
MFE3008

N-CHANNEL DUAL-GATE SILICON-NITRIDE PASSIVATED MOS FIELD-EFFECT TRANSISTORS

. . . depletion mode (Type B) dual gate transistors designed for VHF amplifier and mixer applications. These types are specified as follows:

MFE3006 – RF Amplifier @ 100 MHz
MFE3007 – RF Amplifier @ 200 MHz
MFE3008 – Mixer @ 100 and 200 MHz

- Silicon Nitride Passivation for Excellent Long Term Stability
- High Common-Source Power Gain –
  MFE3006: G_{ps} = 20 dB (Min) @ f = 100 MHz
  MFE3007: G_{ps} = 18 dB (Min) @ f = 200 MHz
- High Common-Source Conversion Gain –
  MFE3008: G_{ps} = 14 dB (Min) @ f = 100 MHz
  G_{ps} = 10 dB (Min) @ f = 200 MHz
- Low Reverse Transfer Capacitance –
  C_{rss} = 0.02 pF (Typ) @ V_{DS} = 15 Vdc

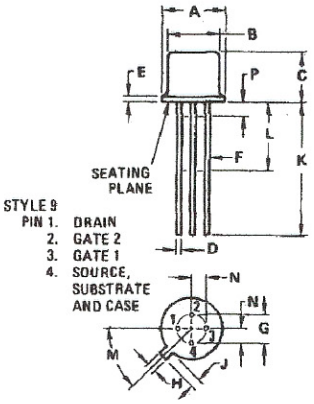
N-CHANNEL

DUAL GATE MOS FIELD-EFFECT TRANSISTORS

TYPE B

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	+25	Vdc
Gate 1 Source Voltage	V_{G1S}	±35	Vdc
Gate 2 Source Voltage	V_{G2S}	±35	Vdc
Drain Current	I_D	30	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	300 2.0	mW mW/°C
Operating Junction Temperature Range	T_J	-65 to +175	°C
Storage Temperature Range	T_{stg}	-65 to +175	°C



STYLE 9
PIN 1. DRAIN
2. GATE 2
3. GATE 1
4. SOURCE, SUBSTRATE AND CASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.53	0.016	0.021
E	–	0.76	–	0.030
F	0.41	0.48	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

ALL JEDEC dimensions and notes apply

CASE 20-03
TO-72

HANDLING PRECAUTIONS:

MOS field-effect transistors have extremely high input resistance. They can be damaged by the accumulation of excess static charge. Avoid possible damage to the devices while handling, testing, or in actual operation, by following the procedures outlined below:

1. To avoid the build-up of static charge, the leads of the devices should remain shorted together with a metal ring except when being tested or used.
2. Avoid unnecessary handling. Pick up devices by the case instead of the leads.
3. Do not insert or remove devices from circuits with the power on because transient voltages may cause permanent damage to the devices.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

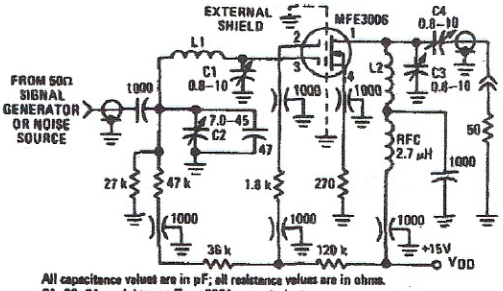
Substrate Connected to Source

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage (I_D = 10 μAdc, V_S = 0, V_{G1} = V_{G2} = -4.0 Vdc)		$V_{(BR)DSX}$	25	–	–	Vdc
Gate 1 to Source Cutoff Voltage (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 200 μAdc)		$V_{G1S(off)}$	–	–	-3.0	Vdc
Gate 2 to Source Cutoff Voltage (V_{DS} = 15 Vdc, V_{G1S} = 0, I_D = 200 μAdc)		$V_{G2S(off)}$	–	–	-3.0	Vdc
Gate 1 Reverse Leakage Current		I_{G1SS}				nAdc
(V_{G1S} = -10 Vdc, V_{G2S} = 0, V_{DS} = 0)			–	–	1.0	
(V_{G1S} = -35 Vdc, V_{G2S} = 0, V_{DS} = 0)			–	–	10	
Gate 2 Reverse Leakage Current		I_{G2SS}				nAdc
(V_{G2S} = -10 Vdc, V_{G1S} = 0, V_{DS} = 0)			–	–	1.0	
(V_{G2S} = -35 Vdc, V_{G1S} = 0, V_{DS} = 0)			–	–	10	
ON CHARACTERISTICS						
Zero-Gate Voltage Drain Current (V_{DS} = 15 Vdc, V_{G1S} = 0, V_{G2S} = 4.0 Vdc)	MFE3006	I_{DSS}	2.0	7.0	18	mAdc
	MFE3007		5.0	10	20	
	MFE3008		2.0	9.0	20	
SMALL-SIGNAL CHARACTERISTICS						
Forward Transadmittance (Gate 1 to Drain)		Y_{fs}				μmhos
(V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 10 mAdc, f = 1.0 kHz)	MFE3006/8		8000	–	18,000	
	MFE3007		10,000	–	18,000	
Input Capacitance		C_{iss}				pF
(V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 10 mAdc, f = 1.0 MHz)	MFE3006/8		–	4.5	6.0	
	MFE3007		–	4.5	5.5	
Output Capacitance		C_{oss}				pF
(V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 10 mAdc, f = 1.0 MHz)	MFE3006/8		–	2.5	4.0	
	MFE3007		–	2.5	3.5	
Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 10 mAdc, f = 1.0 MHz)		C_{rss}	–	0.02	–	pF
Common-Source Noise Figure		NF				dB
(V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 10 mAdc, R_S = 1000 Ohms)						
f = 100 MHz, Figure 1	MFE3006		–	2.5	4.0	
f = 200 MHz, Figure 4	MFE3007		–	3.0	4.0	
Common-Source Power Gain		G_{ps}				dB
(V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 10 mAdc)						
f = 100 MHz, Figure 1	MFE3006		20	25	–	
f = 200 MHz, Figure 4	MFE3007		18	21	–	
Level of Unwanted Signal for 1.0% Cross Modulation (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 10 mAdc)		–	–	100	–	mV
Common-Source Conversion Power Gain		G_{ps}				dB
(V_{DS} = 15 Vdc, V_{G2S} = 0.5 Vdc, Local Oscillator Voltage = 3.0 Vrms)						
Signal Frequency = 100 MHz, Local Oscillator Frequency = 130 MHz, Figure 3	MFE3008		14	17	–	
Signal Frequency = 200 MHz, Local Oscillator Frequency = 230 MHz, Figure 6	MFE3008		10	13	–	

TEST CIRCUITS

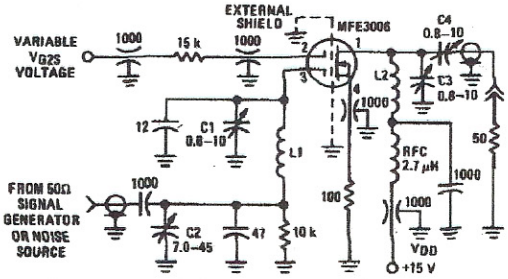
f = 100 MHz

FIGURE 1 – NOISE AND POWER GAIN



All capacitance values are in pF; all resistance values are in ohms.
C1, C3, C4: Johanson Type 2951 or equivalent
C2: Centralab Type 825-G.N. or equivalent
L1: 5 Turns #16 AWG Wire (Internal diameter 5/16", Length 5/8")
L2: 5 Turns #16 AWG Wire (Internal diameter 3/8", Length 5/8")
Adjust C1, C2, C3 and C4 for maximum signal output; C1 and C2 for minimum noise figure, before measuring power gain.
Overall bandwidth = 3.0 MHz @ -3.0 dB
4.5 MHz @ -6.0 dB

FIGURE 2 – GAIN REDUCTION



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C1, C3, C4: Johanson Type 2951 or equivalent
C2: Centralab Type 825-G.N. or equivalent
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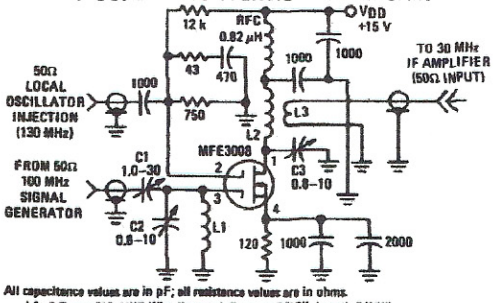
L2: 5 Turns #16 AWG Wire (Internal diameter 3/8", Length 5/8")
Overall bandwidth = 3.0 MHz @ -3.0 dB
4.5 MHz @ -6.0 dB

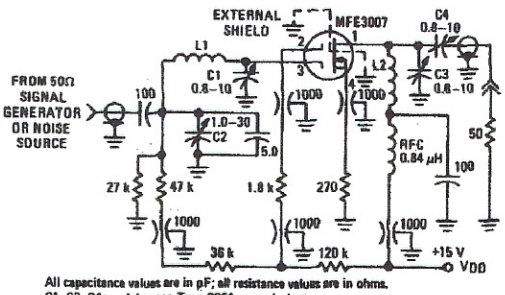
FIGURE 3 – CONVERSION POWER GAIN



All capacitance values are in pF; all resistance values are in ohms.
L1: 6 Turns #16 AWG Wire (Internal diameter 5/16", Length 7/16")
L2: 25 Turns #32 AWG Wire wound on 1/4" O.D. ceramic form
L3: 4 Turns #26 AWG Wire wound on top of and at dc supply end of L2
C1: Johanson Capacitor Type 3908 or equivalent
C2, C3: Johanson Capacitor Type 2850 or equivalent

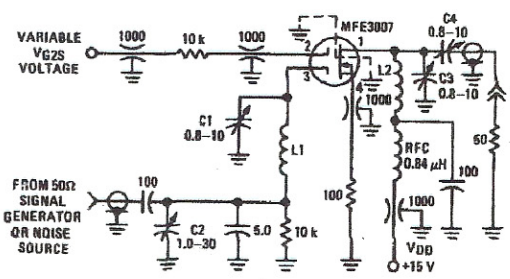
f = 200 MHz

FIGURE 4 – NOISE AND POWER GAIN



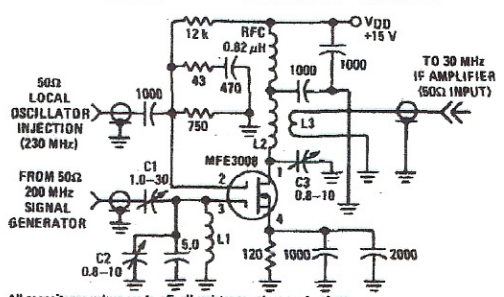
All capacitance values are in pF; all resistance values are in ohms.
C1, C3, C4: Johanson Type 2951 or equivalent
C2: Johanson Type 3908 or equivalent
L1: 4 Turns #16 AWG Wire (Internal diameter 1/4", Length 3/4")
L2: 5 Turns #16 AWG Wire (Internal diameter 1/4", Length 3/4")
Adjust C1, C2, C3 and C4 for maximum signal output; C1 and C2 for minimum noise figure, before measuring power gain.
Overall bandwidth = 9.5 MHz @ -3.0 dB
14 MHz @ -6.0 dB

FIGURE 5 – GAIN REDUCTION



All capacitance values are in pF; all resistance values are in ohms.
C1, C3, C4: Johanson Type 2951 or equivalent
C2: Johanson Type 3908 or equivalent
L1: 4 Turns #16 AWG Wire (Internal diameter 1/4", Length 3/4")
L2: 5 Turns #16 AWG Wire (Internal diameter 1/4", Length 3/4")
Overall bandwidth = 9.5 MHz @ -3.0 dB
14 MHz @ -6.0 dB

FIGURE 6 – CONVERSION POWER GAIN



All capacitance values are in pF; all resistance values are in ohms.
L1: 2 Turns #16 AWG Wire (Internal diameter 1/4", Length 1/4")
L2: 25 Turns #32 AWG Wire wound on 1/4" O.D. ceramic form
L3: 4 Turns #26 AWG Wire wound on top of and at dc supply end of L2
C1: Johanson Capacitor Type 3908 or equivalent
C2, C3: Johanson Capacitor Type 2950 or equivalent

CIRCUIT PERFORMANCE

FIGURE 7 – POWER GAIN versus SOURCE RESISTANCE

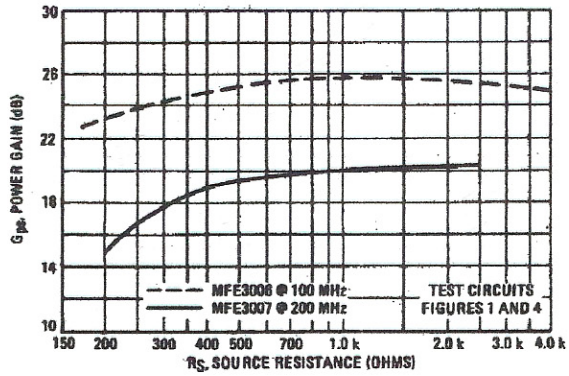


FIGURE 8 – NOISE FIGURE versus SOURCE RESISTANCE

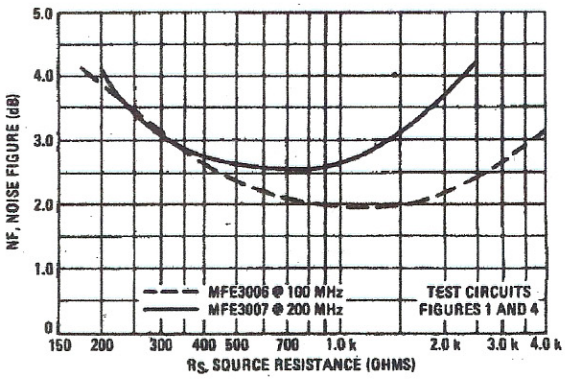


FIGURE 9 – GAIN REDUCTION

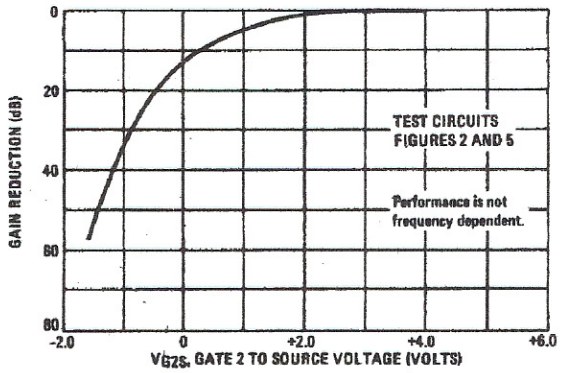


FIGURE 10 – COMMON SOURCE NOISE FIGURE versus GAIN REDUCTION

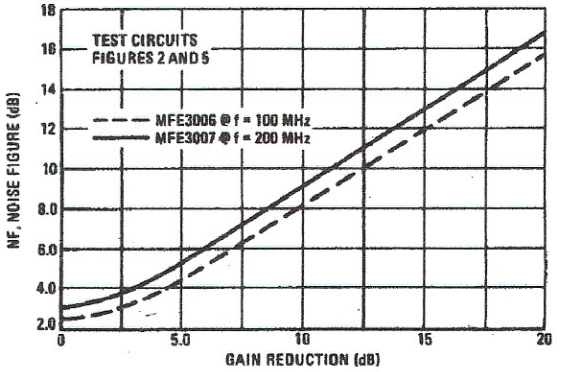


FIGURE 11 – CONVERSION POWER GAIN

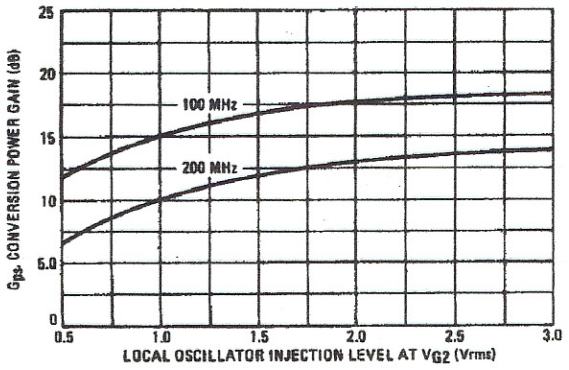
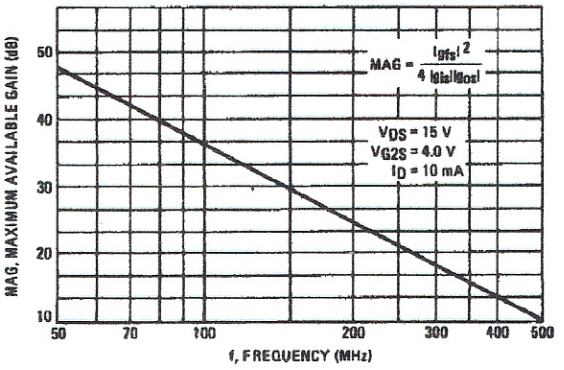


FIGURE 12 – MAXIMUM AVAILABLE POWER GAIN



COMMON-SOURCE ADMITTANCE PARAMETERS

(V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 10 mAdc)

FIGURE 13 – INPUT ADMITTANCE

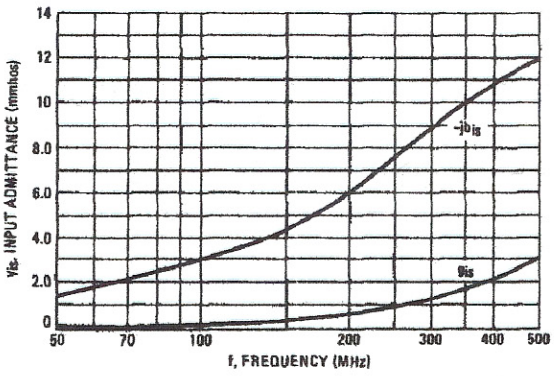


FIGURE 14 – REVERSE TRANSFER ADMITTANCE

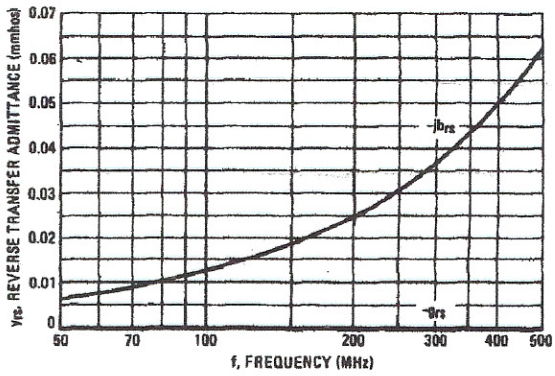


FIGURE 15 – FORWARD TRANSFER ADMITTANCE

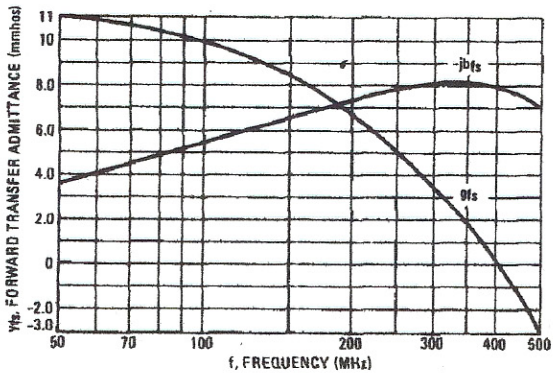
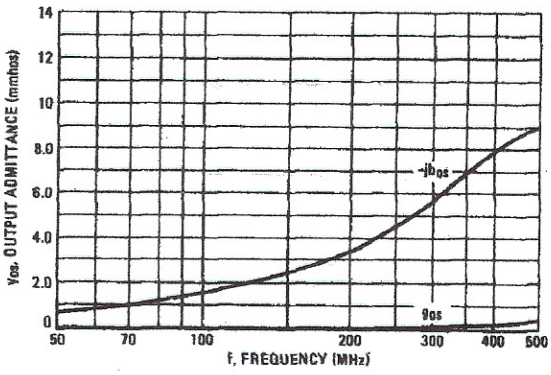


FIGURE 16 – OUTPUT ADMITTANCE



COMMON-SOURCE CIRCUIT DESIGN DATA AS A FUNCTION OF THE STERN "K" FACTOR

(V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 10 mAdc)

FIGURE 17 – TRANSDUCER POWER GAIN

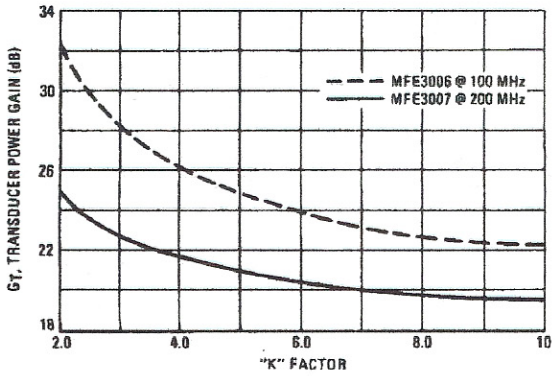


FIGURE 18 – SOURCE ADMITTANCE

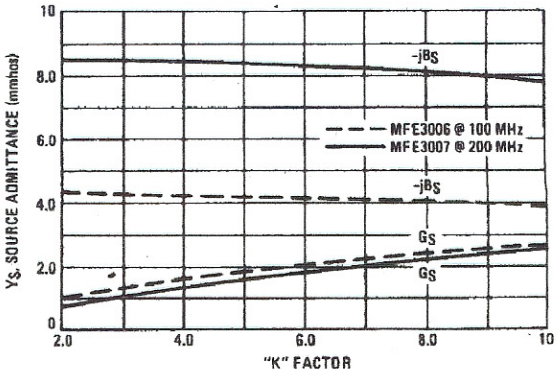
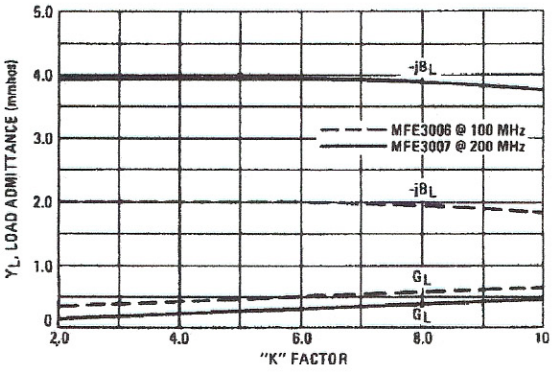


FIGURE 19 – LOAD ADMITTANCE



DESIGN NOTE

Figures 17-19 are included to assist the circuit designer in determining the transducer gain and the proper source and load admittances required for a given stability (Stern "K" factor*).

The Stern "K" factor has been defined to determine the stability of a practical amplifier terminated in finite load and source admittances. If "K" is greater than 1.0, the circuit will be stable. If less than 1.0, the circuit will be unstable. For further details, see Application Note AN-215.

As the C_{rss} of the MFE3006-7 is comparable to the distributed capacitance of the circuit where it is used, a feedback capacitance of 0.1 pF has been used throughout these calculations.

*"Stability and Power Gain of Tuned Transistor Amplifiers," Arthur P. Stern, Proc. I.R.E., March 1967.