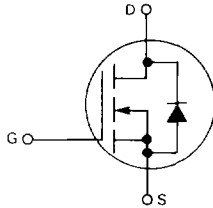


MFE910
MPF910

**N-CHANNEL ENHANCEMENT-MODE
 TMOS FIELD-EFFECT TRANSISTOR**

This TMOS FET is designed for high-voltage, high-speed switching applications such as line drivers, relay drivers, CMOS logic, microprocessor of TTL-to-high voltage interface and high voltage display drivers.

- Fast Switching Speed — $t_{on} = t_{off} = 6.0$ ns Typ
- Low On-Resistance — 2.0 Ohms Typ
- Low Drive Requirement, $V_{GS(th)} = 2.5$ V Max
- Inherent Current Sharing Capability Permits Easy Paralleling of Many Devices

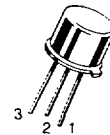


60 VOLTS

**N-CHANNEL TMOS
 FET**

3

MFE910



CASE 79-04
 TO-205AD

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	60	Vdc
Gate-Source Voltage	V_{GS}	± 15	Vdc
Drain Current — Continuous (1)	I_D	0.5	Adc
Pulsed (2)	I_{DM}	1.0	
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	6.25 50	Watts mW/°C
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	1.0 8.0	Watts mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to +150	°C

(1) The Power Dissipation of the package may result in a lower continuous drain current.
 (2) Pulse Width ≤ 300 μs , Duty Cycle $\leq 2.0\%$.

MPF910



CASE 29-03
 TO-226AE

MFE/MPF910

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V _{GS} = 0, I _D = 100 μA)	V _{(BR)DSS}	60	90	—	V _{dc}
Zero Gate Voltage Drain Current (V _{DS} = 40 V, V _{GS} = 0)	I _{DSS}	—	0.1	10	μA _{dc}
Gate-Body Leakage Current (V _{GS} = 10 V, V _{DS} = 0)	I _{GSS}	—	0.01	10	nA _{dc}
ON CHARACTERISTICS					
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 1.0 mA)	V _{GS(th)}	0.3	1.5	2.5	V _{dc}
Drain-Source On-Voltage (V _{GS} = 10 V, I _D = 500 mA)	V _{DS(on)}	—	—	2.5	V _{dc}
On-State Drain Current (V _{DS} = 25 V, V _{GS} = 10 V)	I _{D(on)}	500	—	—	mA
Forward Transconductance (V _{DS} = 15 V, I _D = 500 mA)	g _{FS}	100	—	—	mmhos

FIGURE 1 — V_{GS(th)} NORMALIZED versus TEMPERATURE

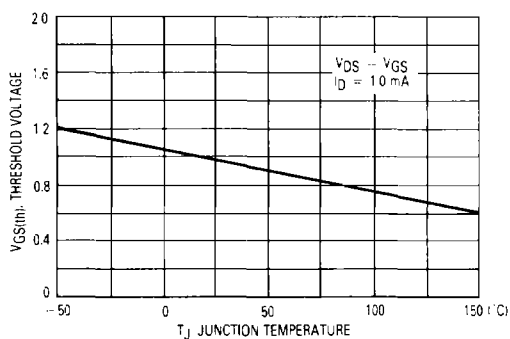


FIGURE 2 — ON-REGION CHARACTERISTICS

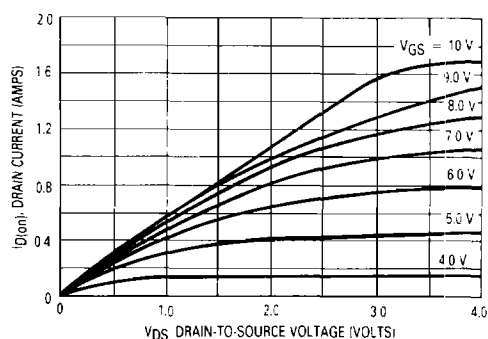


FIGURE 3 — OUTPUT CHARACTERISTICS

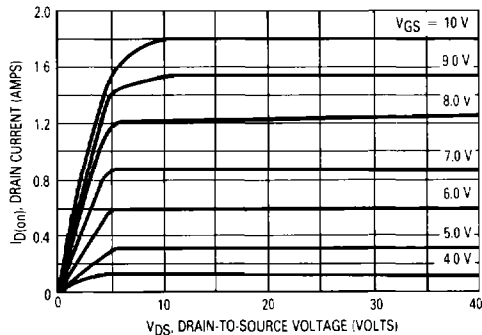
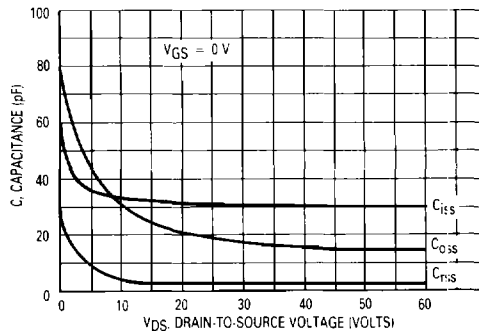


FIGURE 4 — CAPACITANCE versus DRAIN-TO-SOURCE VOLTAGE



OUTLINE DIMENSIONS

