Version: 0.15

MG20L021A

Data Sheet

8-bit I/O type MCU with LED driver

Version 0.15

Table of Contents

1 Features

- Single Chip 8-bit CPU
- Memory
  - Program ROM : 64K Bytes
  - Data RAM : 256 Bytes
- Operating voltage: 1.8V to 3.6V
- 4 general input/output pins (P0.0 to P0.3).
- 16 high sink I/O for LED display.
- Two AUD output pins with 8-bit resolution for audio output.
- Built-in RTC (Real Time Clock).
- One 10-bit PWM output.
- Watchdog timer built-in.
- Built-in two programmable timers and one 16-bit capture timer

  – Timer0, Timer1, Timer 2
- Built-in low voltage reset (typical voltage: below 1.8V).
- HALT mode and STOP mode for power saving.
- Oscillator:

  – Main oscillator (Crystal, Ceramic and RC up to 4MHz @ 2.0V) operation at crystal or RC mode is selected by code option.

  – Sub-oscillator (Crystal and Ceramic up to 100KHz @ 2.0V) operation at crystal mode only.

1.1 Application Field

LED Calendar, LED Name Badge, Toy Controller

2 General Description

MG20L021 is a cost effective, high performance 8-bit micro-controller of MEGAWIN. It integrates an 8-bit CPU core, ROM, RAM, timers, RTC, I/O ports, and system control circuits into a single chip. It is suitable for LED calendar and other products.

3 Pin Configurations

3.1 Pad Assignment

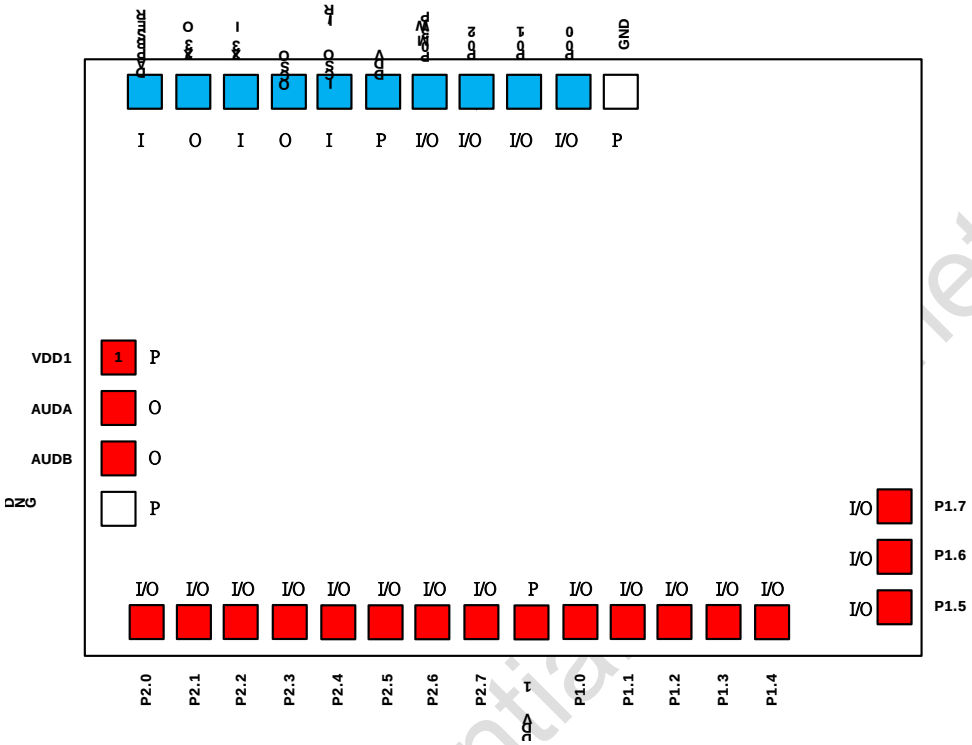


Figure 3-1 Pad Assignment

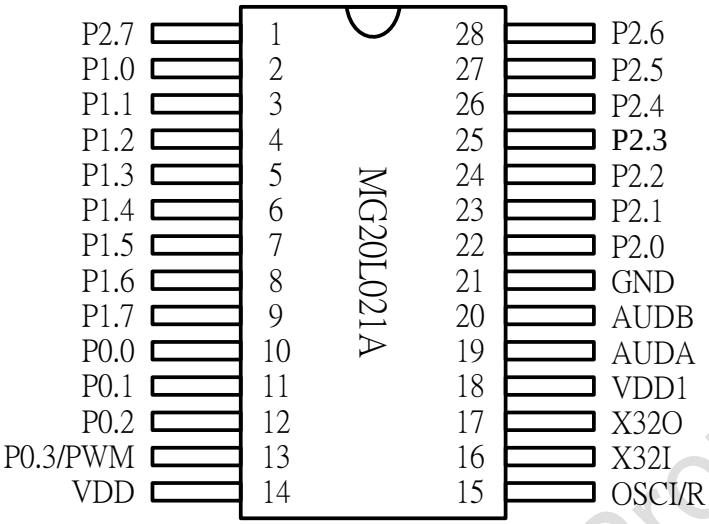
3.2 Pin Description

Table 3-1 Pin Description

Pad No.	Pad Name	I/O	Description
23 ~ 25	P0.0 ~ P0.2	B	General input/output function.
26	P0.3/PWM	B	General input/output function. The P0.3 can be I/O or PWM output pin.
14 ~ 21, 5 ~ 12	P1.0 ~ P1.7 P2.0 ~ P2.7	B	High sink current I/O for LED display.
2, 3	AUDA, AUDB	O	Audio output for direct drive speaker.
1, 13	VDD1	P	Positive power pin for high drive/sink I/O port
32	PAD_RESB	I	System reset pin (low active)
28, 29	OSCI/RI, OSCO	I, O	RC or crystal oscillator pins
30, 31	X32I, X32O	I, O	32.768KHz crystal oscillator pins
4, 22	GND	G	Ground pin
27	VDD	P	Positive power pin for CPU and RTC

Note: In the “Type” field,
“I” means input only.
“O” means output only.
“B” means bi-direction.
“P” means Power, “G” means Ground.

3.3 Package SOP28



4 Block Diagram

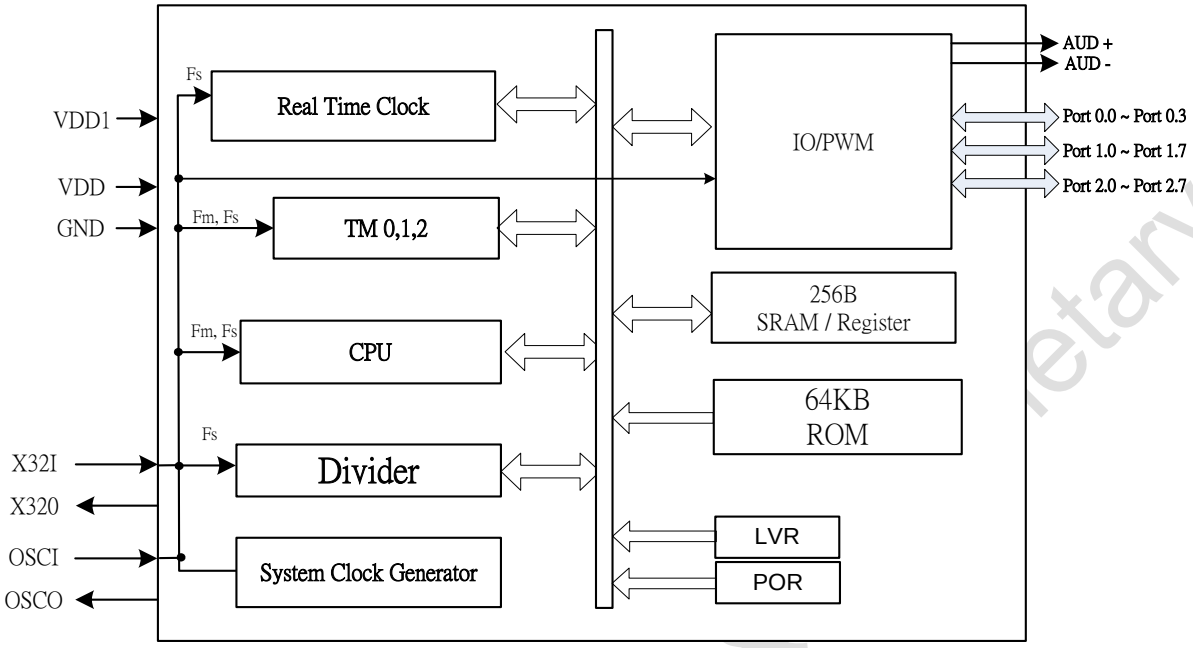


Figure 4-1 Block Diagram

5 Function Description

5.1 Registers

	A
	Y
	X
	P
PCH	PCL
1	S

5.2 Accumulator

The accumulator is a general-purpose 8-bit register, which stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of two data words used in these operations.

5.3 Index Register(X,Y)

There are two 8-bit index registers (X and Y), which may be used to count program steps or to provide an index value to be used in generating an effective address. When executing an instruction, which specifies indexed addressing, the CPU fetches the OP Code and the base address, and modifies the address by adding the index register to it prior to performing the desired operation. Pre- or post-index of index address is possible.

5.4 Processor Status Register

The 8-bit processor status register contains seven status flags. Some of the flags are controlled by the program, others may be controlled both the program and the CPU.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N	V	1	B	D	I	Z	C

N: Signed flag, 1 = negative, 0 = positive
V: Overflow flag, 1 = true, 0 = false
B: BRK interrupt command, 1 = BRK, 0 = IRQB
D: Decimal mode, 1 = true, 0 = false
I: IRQB disable flag, 1 = disable, 0 = enable
Z: Zero flag, 1 = true, 0 = false
C: Carry flag, 1 = true, 0 = false

5.5 Program Counter(PC)

The 16-bit program counter register provides the addresses, which step the micro-controller through sequential program instructions. Each time the micro-controller fetch an instruction from program memory, the lower byte of the program counter (PCL) is placed on the low-order 8 bits of the address bus and the higher byte of the program counter (PCH) is placed on the high-order 8 bits. The counter is incremented each time an instruction or data is fetched from program memory.

5.6 Stack Point(S)

The stack pointer is an 8-bit register, which is used to control the addressing of the variable-length stack. The stack pointer is automatically incremented and decremented under control of the micro-controller to perform stack manipulations under direction of either the program or interrupts (/NMI or /IRQ). The stack allows simple implementation of nested subroutines and multiple level interrupts. The stack pointer is initialized by the user's firmware.

6 Memory Organization

There are 256 bytes SRAM, located in address 0000H to 01FFH, in the MG20L021A . They could be used as either working RAM or stacks according to application programs. For the purpose above, the location 0000H to 007FH and 0100H to 017FH are overlaps. In other words, accessing any locations inside the range 0000H to 007FH is equivalent to access the corresponding ones in the range 0100 to 017FH. All special function registers, SFRs, are located at the region 00C0H to 00FFH. Such an arrangement could benefit from the faster access time of zero-page.

There are 64K bytes program/data ROM in MG20L021A . It is combined with 32K program/data ROM and bank switching data ROM. The ROM address from 8000H to FFFFH can store program and other data. There are two banks in MG20L021A that is index by SFR. The default bank number is 00H after power on or reset. The bank select function, ranged from 4000H to 7FFFH (16Kbyte/bank), is used for extending memories if the ROM size is more than 32K bytes in MG20L021A . The address mapping of MG20L021A is shown as below.

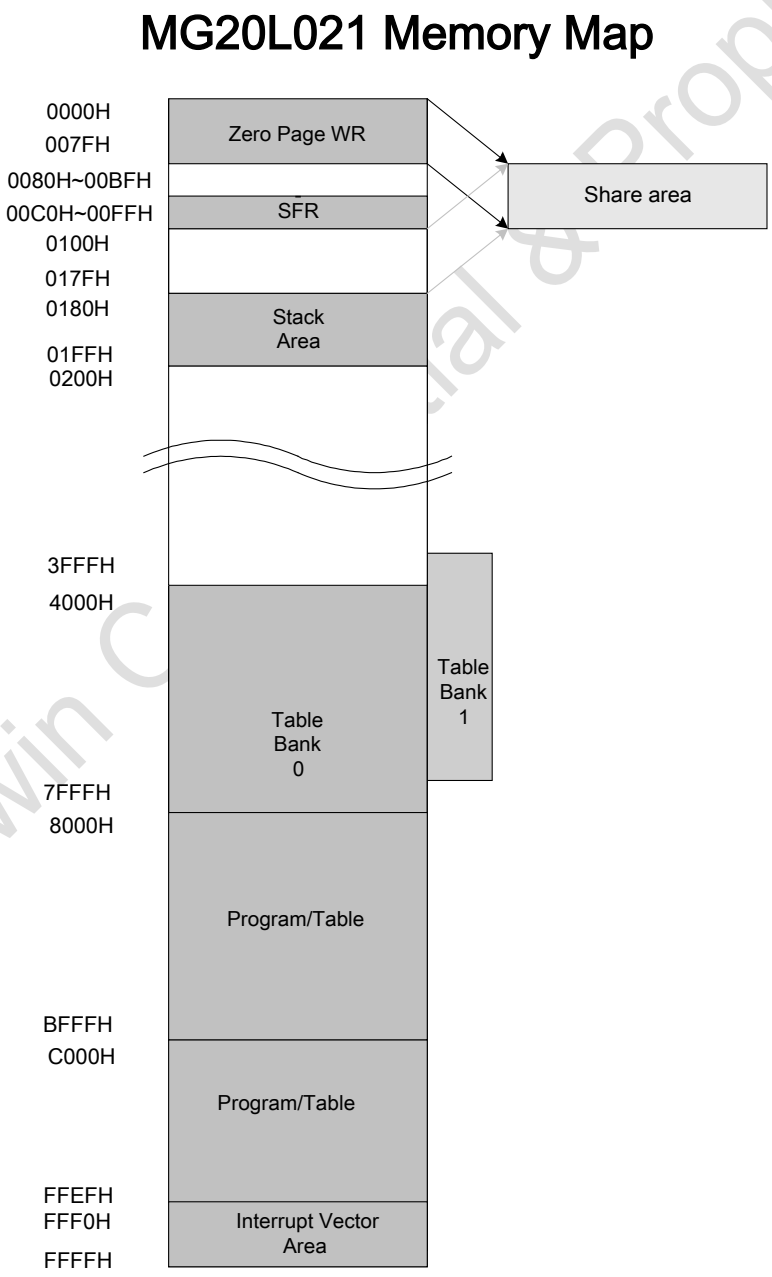


Figure 6-1 Memory Map

6.1 SFR Mapping

The address 00C0H to 00FFH is reserved for special function registers (SFR). The SFR is used to control or store the status of I/O, timers, system clock and other peripheral.

Table 6-1 SFR Table

SFR (special function register): 00C0H~00FFH

Address	Content	Default		Address	Content	Default
00C0	MCLKmgr(W)	0-0--000		00D0	IO_MFR(W)	---0000
00C1	SYS_STS(R)/SYS_CSTS(W)	xx-------		00D1		
00C2	IRQ_EN(R/W)	00000000		00D2	P0buf(W)/ P0pad(R)	----0000
00C3	IRQ_ST(R)/IRQ_CLR(W)	00000000		00D3	P0dir(W)	----0000
00C4	RLH_EN(W)	00000000		00D4	P0puhl(W)	---00000
00C5				00D5	P0opd(W)	----0000
00C6				00D6		
00C7				00D7	P1buf(W)/ P1pad(R)	00000000
00C8	TM0(R/W)	11111111		00D8	P1dir(W)	00000000
00C9	TM0_CTL(W)	00---000		00D9	P1plh(W)	00000000
00CA	TM1(R/W)	11111111		00DA	P1opd(W)	00000000
00CB	TM1_CTL(W)	00---000		00DB		
00CC	TM2L(R/W)	11111111		00DC	P2buf(W)/ P2pad(R)	00000000
00CD	TM2H(R/W)	11111111		00DD	P2dir(W)	00000000
00CE	TM2_CTL(W)	000--000		00DE	P2plh(R/W)	00000000
00CF	DIV_STL(R) / DIV_SEL(W)	-------0		00DF	P2opd(R/W)	00000000

Address	Content	Default		Address	Content	Default
00E0	RTC00(R/W)	00000000		00F0	PWML(R/W)	00000000
00E1				00F1	PWMH(R/W)	------10
00E2				00F2	BANK(R/W)	-------0
00E3				00F3	CWPR(W)	xxxxxxxx
00E4				00F4		--------
00E5				00F5		--------
00E6				00F6		--------
00E7				00F7	CH1/ENV1(W)	00000000
00E8				00F8	CH2/ENV2(W)	00000000
00E9				00F9	AB_TC(R/W)	0000-000
00EA				00FA		
00EB				00FB		
00EC				00FC		
00ED				00FD		
00EE				00FE		
00EF				00FF		

6.2 Write Protect Function Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00F3H	CWPR	PT7	PT6	PT5	PT4	PT3	PT2	PT1	PT0	-	√

PT7 ~ PT0: Conditional Write Protect Pattern
The CWPR is used to be the SYSCSTS.6 (WDT) and MCLKmgr write protector.
To unlock the write protector, it must write pattern 58H to CWPR SFR firstly.

PT7~PT0: Write Protect Pattern. In MG20L021A write protect pattern is “58H”
Note:

1. *When CWPR is written by firmware, it would be automatically cleared by hardware after the “next write action” of firmware.*

※ Bit-manipulation instructions are not available on this register.

6.3 Bank select

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00F2H	BANK	-	-	-	-	-	-	-	BK0	√	√

Program can switch the memory bank through this register. After power on reset, this register in initialized as 00H.

7 Interrupt

There are four kinds interrupt source is provided in MG20L021A . The flag IRQ_EN and IRQ_ST are used to control the interrupts. When flag IRQ_ST is set to '1' by hardware and the corresponding bits of flag IRQ_EN has been set by software, an interrupt is generated. When an interrupt occurs, all of the interrupts are inhibited until the CLI or STA IRQ_EN, # I instruction is invoked. Executing the SEI instruction can also disable the interrupts.

Table 7-1 Interrupt Vector Table

Vector Address	Item	Flag	Properties	Memo
FFFEH, FFFFH	RTC.IRQ	IRQ_ST.0	Int.	RTC 0.5S interrupt
	VD1.IRQ	IRQ_ST.1	Ext.	VDD1 toggle interrupt
	P0 IRQ	IRQ_ST.2	Ext.	P0.0 ~ P0.3 interrupt vector
	TM0 IRQ	IRQ_ST.3	Int.	TM0 underflow interrupt
	DIV1 IRQ	IRQ_ST.4	Int.	Divider 1 carry out interrupt
	TM1 IRQ	IRQ_ST.5	Int.	TM1 underflow interrupt
	TM2.IRQ	IRQ_ST.6	Int.	TM2 underflow interrupt
	DIV2.IRQ	IRQ_ST.7	Int.	Divider 2 carry out interrupt
FFFCH, FFFDH	RESET	None	Ext.	Initial reset
	WDT	SYS_STS.6	Int.	Watch dog timer reset
	LVR	None	Int.	Low voltage reset

7.1 Interrupt Register

IRQ enable flag

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C2H	IRQ_EN	DIV2	TM2	TM1	DIV1	TM0	P0	VD1	RTC	√	√

Program can enable or disable the ability of triggering IRQ through this register.
0: Disable (default "0" at initialization)
1: Enable
P0: Pull-High Falling edge or Pull–Low Rise edge occurs at port 0 input mode.
TM0, TM1, TM2: Timer 0, 1, 2 underflow occurs.
DIV1: Divider selected (DIV/4=8192 Hz) interrupt frequency occurred.
DIV2: Divider selected (DIV/16=2048 Hz or DIV/32=1024 Hz) interrupt frequency occurred.
VD1: Rising or falling edge occurs at VDD1 (both edge could generate interrupt).
RTC: RTC 0.5S interrupt.

IRQ status flag

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C3H	IRQ_ST	DIV2	TM2	TM1	DIV1	TM0	P0	VD1	RTC	√	-
00C1H	SYS_STS	VD1S	WDT	-	-	-	-	-		√	-

When IRQ occurs, program can read this register to know which source triggering IRQ. If the interrupt triggering is enabled and the interrupt event is accepted, the correspond IRQ status flag should be cleared by program after the interrupt vector is loaded into program counter. All the interrupt behavior is same as above description
VD1S: VDD1 high/low status flag (external pull low should be added between VDD1 pin and GND pin if the VD1 interrupt is used in your application)
WDT: Watch Dog time-out occurred

※ Bit-manipulation instructions not available on this register.

IRQ clear flag

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C3H	IRQ_CLR	DIV2	TM2	TM1	DIV1	TM0	P0	VD1	RTC-	-	√
00C1H	SYS_CSTS	-	WDT	-	-	-	-	-		-	√

Program can clear the interrupt event by writing '1' into the corresponding bit.
The SYS_CSTS.6 (WDT) is protected by CWPR.

※ Bit-manipulation instructions not available on this register.

7.2 Interrupt System

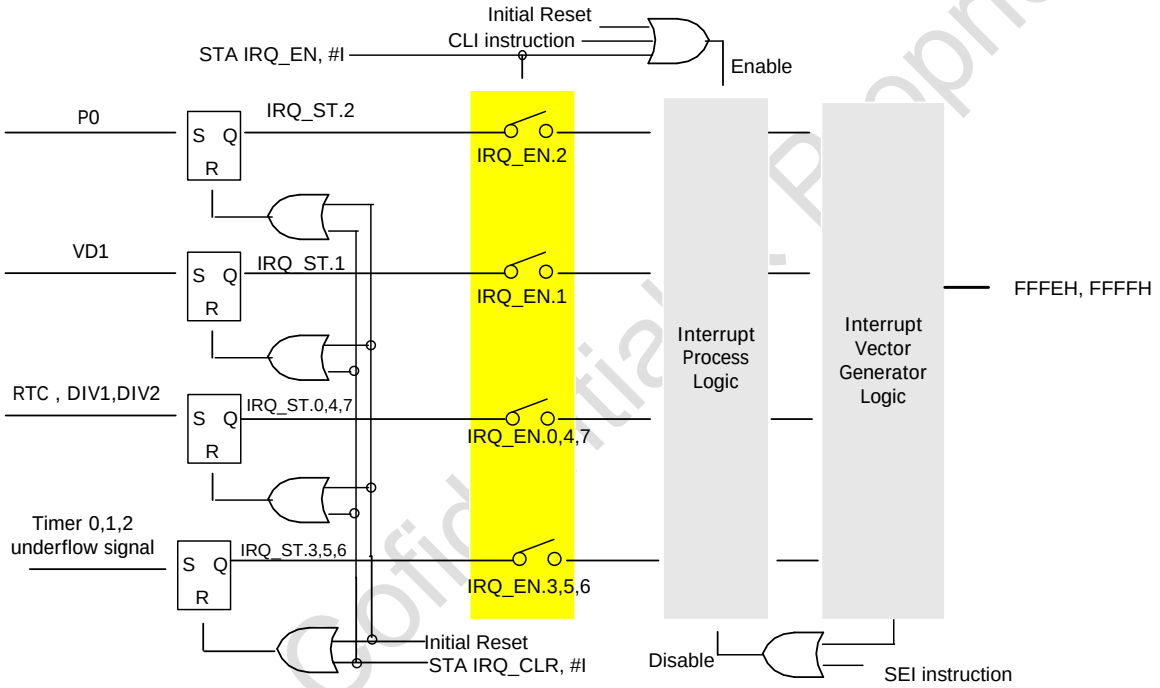


Figure 7-1 Interrupt System Diagram

8 Reset

8.1 Low Voltage Reset (LVR)

The MG20L021A provides low voltage reset circuit in order to monitor the supply voltage of the device. If the supply voltage of the device is within the range 0.9V ~ VLVR, such as changing a battery, the LVR will automatically reset the device internally.

The LVR includes the following specifications

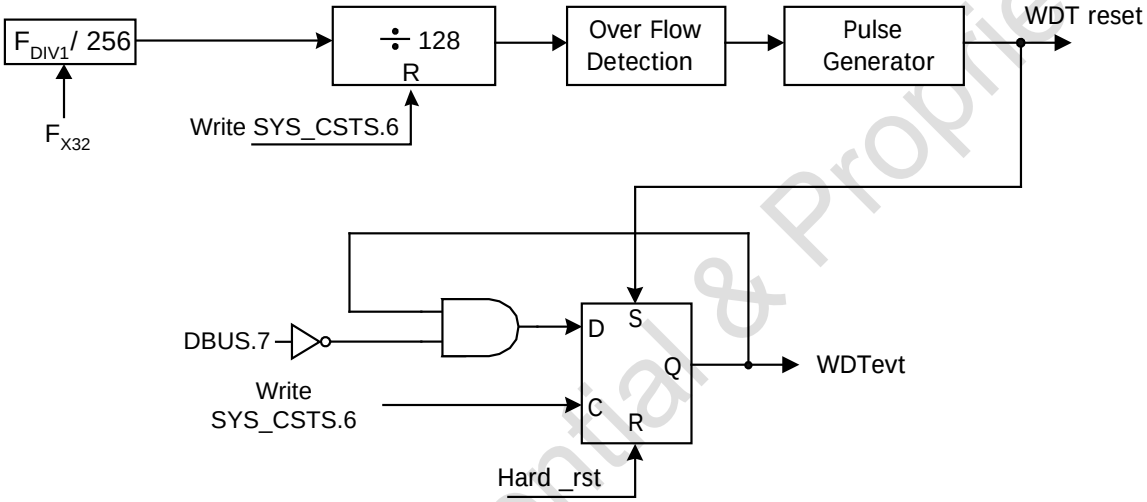
1. The low voltage (0.9V~VLVR) has to remain in their original state to exceed 1ms. If the low voltage state does not exceed 1ms, the LVR will ignore it and do not perform a reset function.
2. In the LVR mode, the clock source (INT./EXT. OSC) continuous oscillating and the IO status becomes default value.

8.2 Watchdog Timer (WDT)

(The example is base on 32.768KHz/ (256x128))

Name		/128	/64	/32	/16	/8	/4	/2	R	W
WDT		1Hz	2Hz	4Hz	8Hz	16Hz	32Hz	64Hz	-	-

The watchdog timer time-out period is obtained by the equation: F_{X32}/(256x128).
Before watchdog timer time-out occurs, the program must clear the 7-bit WDT timer by writing 1 to SYS_CSTS.6. WDT overflow will cause system reset and set SYS_CST.6 high. Before watchdog timer time-out occurs, the program must write 58H into CWPR then clear the 7-bit WDT timer by writing 1 to SYS_CSTS.6 at next write OP code. WDT overflow will cause system reset and set SYS_STS.6 to high. The WDT register contents will be reset by hardware reset, low voltage reset and power-on reset.



Watchdog Block Diagram

Figure 8-1 Watch Dog Diagram

The operation of clear WDT example is shown as below:

```
clear_WDT .macro
          SEI
          LDA      #58h
          STA      CWPR                    ;(F3h)
          LDA      #40H
          STA      C1H                     ; SYS_CSTS
          CLI
         .endm
```

9 Power Control

9.1 Main Clock Manager Control Register

Main Clock Manager

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C0H	MCLKmgr	CKS7	-	IORS	-	-	CKC1	CKC0	HALT	-	√

CKS7: F_{CPU} clock source select. 0: F_{OSC}, 1:F_{X32}
IORS: IO reset selector
0: Only WDT can not reset the I/O status
1: All reset sources (/RES pin, POR, LVR, WDT) can reset the I/O status

CKC1	CKC0	System clock control
0	0	F_{OSC} enable, F_{X32} enable (Dual mode)
0	1	F_{OSC} enable, F_{X32} disable (Single mode)
1	0	F_{OSC} disable, F_{X32} enable (Slow mode)
1	1	F_{OSC} disable, F_{X32} disable (Stop mode)

Note: MCLKmgr.CKC0 is inhibited when the code option NMO F_{X32} is enabled.

HALT: FCPU off-line control bit. 1: FCPU off-line, 0: FCPU on-line

Program can switch the normal operation mode to the power-saving mode for saving power consumption through this register. There are three power saving modes in this system.

Slow mode: *(MCLKmgr.CKC1 =1, MCLKmgr.CKC0 = 0)*
The main uC clock (F_{OSC}) stops oscillating. Only very low power is needed for uC to keep running.

Stop mode: *(MCLKmgr.CKC1 = 1, MCLKmgr.CKC0 = 1)*
All system clocks stop oscillating. The uC can be awakened from stop mode by 4-ways: port 0 interrupt, hardware reset, low voltage reset, or power-on reset. This mode is inhibited when the code option NMO F_{X32} is enabled.

Halt mode: (MCLKmgr.HALT = 1)
The F_{CPU} clock in off-line status. The oscillator(s) still oscillating if the MCLKmgr.CKC1, MCLKmgr.CKC0 keep low. The uC can be awakened from halt mode by 5-ways: all interrupt events (DIV1, DIV2, TM0, TM1, TM2, port 0, VDD1, RTC), hardware reset, low voltage reset, watchdog timer reset, or power-on reset. Before enter halt mode, the F_{CPU} must set to slow mode firstly to make the current consumption less than 10uA.

※ Bit-manipulation instructions not available on this register.

Note: Conditional Write Protect Register (CWPR) protects the contents of MCLKmgr register. When system change operation mode, the program must write 58H to CWPR and then set MCLKmgr at next write OP code.

For example, the operation of entry stop mode as below:

Example:

```
SEI
LDA   #58h
STA   CWPR                    ;(F3h)
LDA   #06H
STA   C0H                     ; MCLKmgr
CLI
```

9.2 Release halt mode enable flag

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C4H	RLH_EN	DIV2	TM2	TM1	DIV1	TM0	P0	VD1	RTC	-	√

Set IRQ_CLR register to clear the halt release event.
Release halt status flag is the IRQ_ST register.

※ Bit-manipulation instructions not available on this register.

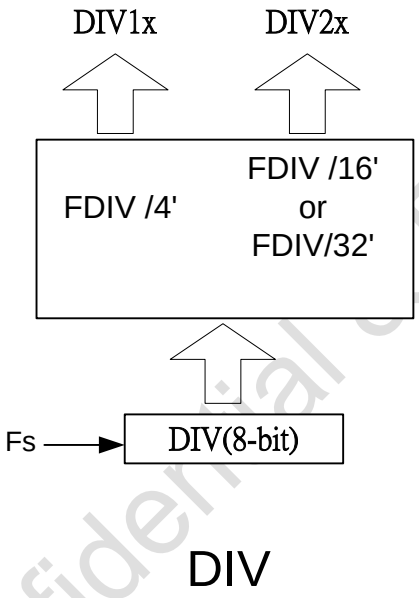
10 Divider

DIV interrupt selector (If the frequency of divider 1 clock source is 32.768KHz)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00CFH	DIV_STL	128 Hz	256 Hz	512 Hz	1024 Hz	2048 Hz	4096 Hz	8192 Hz	16384 Hz	√	-
00CFH	DIV_SEL	-	-	-	-	-	-	-	CKO0	-	√

The clock source of divider is fixed to F_{X32}. The divider contents can be reset to 00H by POR, LVR only.

CKO0	Selected DIV1 frequency		Selected DIV2 frequency	
0	F_{DIV} / 4	(8192 Hz)	F_{DIV} / 16	(2048 Hz)
1	F_{DIV} / 4	(8192 Hz)	F_{DIV} / 32	(1024 Hz)



DIV

※ Bit-manipulation instructions not available on this register.

11 RTC (Real Time Clock) register

(clock source is F_{X32}/256)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E0H	RTC00	S7	S6	S5	S4	S3	S2	S1	S0	√	√

The RTC part contains one 8-bit registers with an auto-incrementing address register, an on-chip 32.768kHz oscillator with an integrated capacitor, a frequency divider which provides the source clock for the Real-Time Clock (RTC). The RTC contents can be reset to 00H by POR only.
Program can enable or disable the ability of triggering RTC interrupt through IRQ_IEN.0 register. Programmer can clear the IRQ_ST.0 by writing '1' into the bit 0 of IRQ_CLR.

(The example frequency is 32.768KHz)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E0H	RTC00	2S	1S	2Hz	4Hz	8Hz	16Hz	32Hz	64Hz	√	√

12 Timer

12.1 Timer0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C8H	TM0	T7	T6	T5	T4	T3	T2	T1	T0	√	√
00C9H	TM0_CTL	STC	RL/S	-	-	-	TKI2	TKI1	TKI0		√

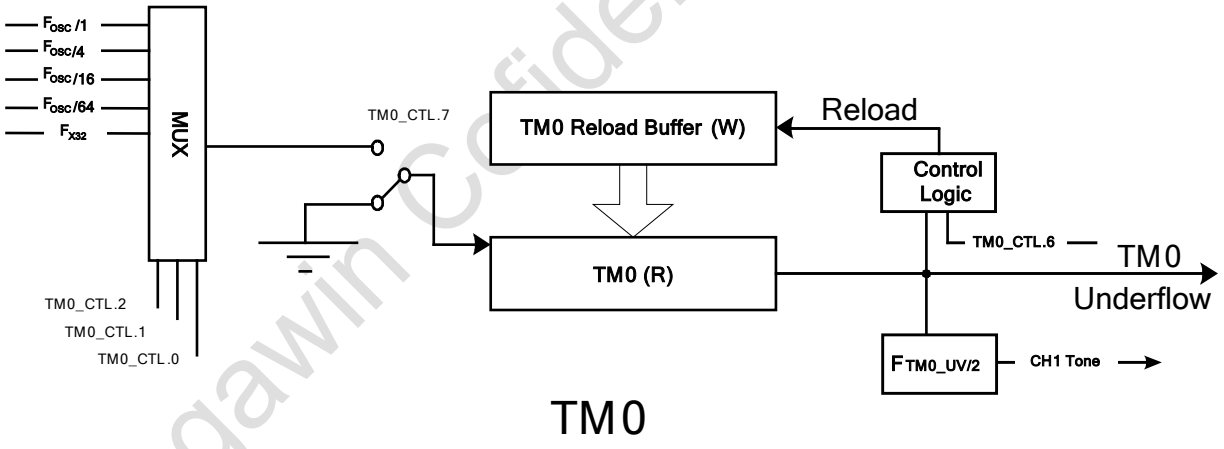
STC: Start/Stop counting. 1: start and pre-load the value to counter, 0: stop timer clock
RL/S: Auto-reload disable/enable. 1: disable auto-reload, 0: enable auto-reload

TKI2	TKI1	TKI0	Selected TM0 input frequency
0	0	0	F_{OSC} / 1
0	0	1	F_{OSC} / 4
0	1	0	F_{OSC} / 16
0	1	1	F_{OSC} / 64
1	X	X	F_{X32}

X: Don't care.
Timer 0 is an 8-bit down-count counter. The counter underflow frequency of timer 0, F_{TM0_UV}, can be calculated with the equation:
$F_{TM0\_UV} = F_{TM0} / (TM0+1)$, where the F_{TM0} is the timer input frequency set by TKI2, TKI1 and TKI0.

For example: (if F_{TM0} = 2.000MHz, TKI2=TKI1=TKI0=0)

TM0	Frequency
00H	Reserved
01H	1.000MHz
02H	667kHz
…	…
FFH	7.84kHz



12.2 Timer1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00CAH	TM1	T7	T6	T5	T4	T3	T2	T1	T0	√	√
00CBH	TM1_CTL	STC	RL/S	-	-	-	TKI2	TKI1	TKI0		√

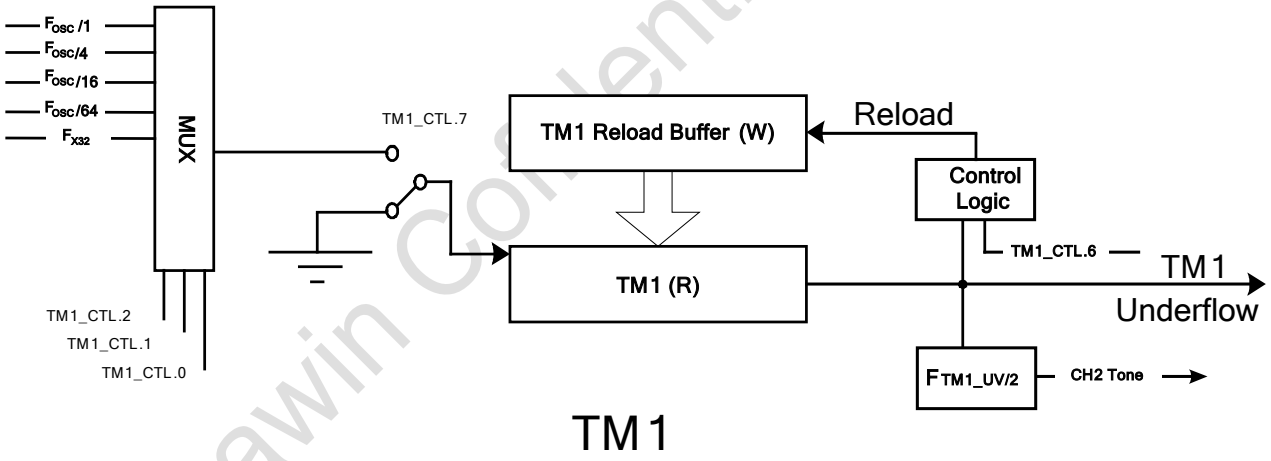
STC: Start/Stop counting. 1: start and pre-load the value to counter, 0: stop timer clock
RL/S: Auto-reload disable/enable. 1: disable auto-reload, 0: enable auto-reload

TKI2	TKI1	TKI0	Selected TM1 input frequency
0	0	0	F_{OSC} / 1
0	0	1	F_{OSC} / 4
0	1	0	F_{OSC} / 16
0	1	1	F_{OSC} / 64
1	X	X	F_{X32}

X: Don't care.
Timer 1 is an 8-bit down-count counter. The counter underflow frequency of timer 1, F_{TM1_UV}, can be calculated with the equation:
$F_{TM1\_UV} = F_{TM1} / (TM1+1)$, where the F_{TM1} is the timer input frequency set by TKI2, TKI1 and TKI0.

For example: (if F_{TM1} = 2.000MHz, TKI2=TKI1=TKI0=0)

TM1	Frequency
00H	Reserved
01H	1.000MHz
02H	667kHz
…	…
FFH	7.84kHz



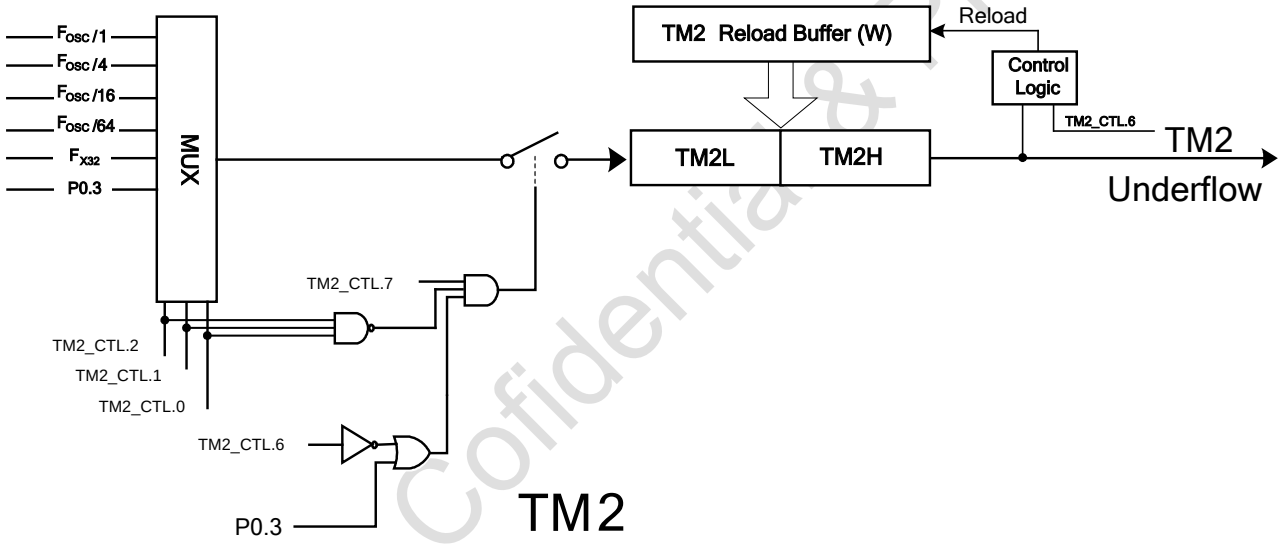
TM1

12.3 Timer2

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00CCH	TM2L	T7	T6	T5	T4	T3	T2	T1	T0	√	√
00CDH	TM2H	T7	T6	T5	T4	T3	T2	T1	T0	√	√
00CEH	TM2_CTL	STC	RL/S	GATE	-	-	TKI2	TKI1	TKI0		√

STC: Start/Stop counting. 1: start value to counter, 0: stop timer clock
RL/S: Auto-reload disable/enable. 1: disable auto-reload, 0: enable auto-reload
Gate: Gating control. 1: Timer2 is enabled only while P0.3 is high and STC control bit is set.
0: Timer2 is enabled whenever STC control bit is set. When TKI2 to TKI0 are set to "1", the gate function will be disabled.
TKI2, TKI1, TKI0:

TKI2	TKI1	TKI0	Selected TM2 input frequency
0	0	0	Fosc / 1
0	0	1	Fosc / 4
0	1	0	Fosc / 16
0	1	1	Fosc / 64
1	0	0	F_{X32}
1	1	1	P0.3 (capture disable)



13 Configurable I/O Ports

13.1 Port 0

Port 0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D2H	P0pad/ P0buf	P07	P06	P05	P04	P03	P02	P00	P00	√	√

Port 0 is an 4-bit I/O port; each pin can be programmed as input or output individually.
When the P0.n is configured as input pin, reading P0pad.n would always read the logic value from pad.
When the P0.n is configured as output pin, the P0.n pin would output the logic content of P0.n and reading the P0pad.n would always read logic '0'.

※ Bit-manipulation instructions not available on this register.

Port 0 Direction Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D3H	P0dir	-	-	-	-	DR3	DR2	DR1	DR0	-	√

P0dir (Port 0 Direction)
P0dir.n = 0: P0.n is configured as an input pin. (Default)
1: P0.n is configured as an output pin.

※ Bit-manipulation instructions are not available on this register.

Port 0 Pull-high(low) Control Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D4H	P0puhl	-	-	-	SHL	PHL3	PHL2	PHL1	PHL0	-	√

SHL: Pull High or Pull Low Select
0: Select internal pull-high (Default)
1: Select internal pull-low
P0puhl: PHL3~PHL0 Control bit is used to enable the pull-high(low) of port0.3~ port0.0 pin.
0: Disable internal pull-high (Default)
1: Enable internal pull-high (low) ; (Auto Disable at port0.n set output pin and output low)

※ Bit-manipulation instructions not available on this register.

Port 0 Open-Drain Control Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D5H	P0opd	-	-	-	-	OD3	OD2	OD1	OD0	-	√

P0opd: OD3~OD0 control bit is used to enable the open-drain of port0.3~ port0.0 pin.
0: Disable open-drain output(CMOS Output). (Default)
1: Enable open-drain output .

※ Bit-manipulation instructions not available on this register.

13.2 Port 1

Port 1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D7H	P1pad/ P1buf	P17	P16	P15	P14	P13	P12	P10	P10	√	√

Port 1 is an 8-bit I/O port; each pin can be programmed as input or output individually.
When the P1.n is configured as input pin, reading P1pad.n would always read the logic value from pad.
When the P1.n is configured as output pin, the P1.n pin would output the logic content of P1.n and reading the P1pad.n would always read logic '0'.

※ Bit-manipulation instructions not available on this register.

Port 1 Direction Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D8H	P1dir	DR7	DR6	DR5	DR4	DR3	DR2	DR1	DR0	-	√

P1dir (Port 1 Direction)
P1dir.n = 0: P1.n is configured as an input pin. (Default)
1: P1.n is configured as an output pin.

※ Bit-manipulation instructions not available on this register.

Port 1 Pull-high Control Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D9H	P1plh	PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0	-	√

PH0 ~ PH7: Control bit is used to enable the pull-high of P1.0 ~ P1.7pin.
0: Disable internal pull-high (default);
1: Enable internal pull-high, the pull-high will be disable automatically when P1.n is set to output mode low state;

※ Bit-manipulation instructions not available on this register.

Port 1 Open-Drain Control Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00DAH	P1opd	OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0	-	√

OD0 ~ OD7: Control bit is used to enable the open-drain of P1.0 ~ P1.7 pin.
0: Disable open-drain output (CMOS output);
1: Enable open-drain output

※ Bit-manipulation instructions not available on this register.

13.3 Port 2

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00DCH	P2pad/ P2buf	P27	P26	P25	P24	P23	P22	P21	P20	√	√

Port 2 is an 8-bit I/O port; each pin can be programmed as input or output individually.
When the P2.n is configured as input pin, reading P2pad.n would always read the logic value from pad.
When the P2.n is configured as output pin, the P2.n pin would output the logic content of P2.n and reading the P2pad.n would always read logic '0'.

※ Bit-manipulation instructions not available on this register.

Port 2 Direction Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00DDH	P2dir	DR7	DR6	DR5	DR4	DR3	DR2	DR1	DR0	-	√

P2dir (Port 2 Direction)
P2dir.n = 0: P2.n is configured as an input pin. (Default)
1: P2.n is configured as an output pin.

※ Bit-manipulation instructions not available on this register.

Port 2 Pull-high Control Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00DEH	P2plh	PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0	-	√

PH0 ~ PH7: Control bit is used to enable the pull-high of P2.0 ~ P2.7 pin.
0: Disable internal pull-high (default);
1: Enable internal pull-high, the pull-high will be disable automatically when P2.n is set to output mode low state;

※ Bit-manipulation instructions not available on this register.

Port 2 Open-Drain Control Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00DFH	P2opd	OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0	-	√

OD0 ~ OD7: Control bit is used to enable the open-drain of P2.0 ~ P2.7 pin.
0: Disable open-drain output (CMOS output);
1: Enable open-drain output

※ Bit-manipulation instructions not available on this register.

14 I/O multi-function selector

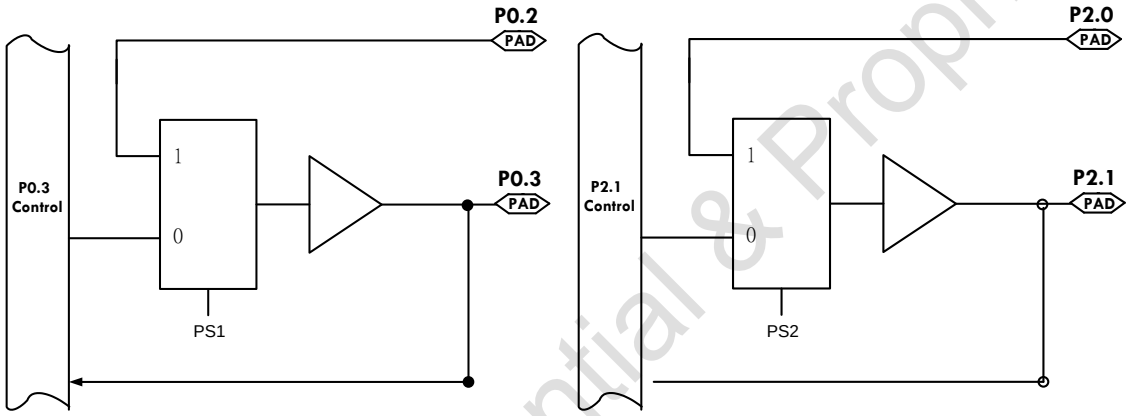
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D0H	IO_MFR	-	-	-	-	SVIH	PS2	PS1	PS0	-	√

The I/O can be programmed to special function via IO_MFR register.

PS0 = “0”: Port0.3 is a normal I/O (Default), “1”: Port0.3 is PWM output when Port0.3 is set to Output mode.

PS1= “0” : Port0.3 is a normal I/O (Default), “1”: Port0.3 will Output From Port0.2 Pad when Port0.3 is set to Output mode.
IO_MFR[1] = 0 : P0.3 normal I/O ◦
IO_MFR[1] = 1 : When P0.3 set to output mode and PS0=”0” , Port0.3 Output is Port0.2 Pad ◦

PS2= “0” : Port2.1 is a normal I/O (Default), “1”: Port2.1 will Output From Port2.0 Pad when Port2.1 is set to Output mode.
IO_MFR[2] = 0 : P2.1 normal I/O ◦
IO_MFR[2] = 1 : When P2.1 set to output mode , Port2.1 Output is Port2.0 Pad ◦



SVIH is Port 1,2 VIH Select (Input 0 →1) SFR :
IO_MFR[3]=”0”: Port1, 2 is a normal VIH (0.7VDD) (Default),
IO_MFR[3]=“1”: Port1, 2 is a special VIH (0.9VDD)

※ Bit-manipulation instructions not available on this register.

15 PWM Register

(PWML : Default 0000,0000) , (PWMH : Default ----,--10)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00F0H	PWML	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	√	√
00F1H	PWMH							PD9	PD8	√	√

The PWM clock source frequency is Fm. P0.3/PWM pins produce 10-bit resolution PWM output. The PWM output duty is proportional to the code value of data buffer. Default is 10 0000 0000B

16 CH1, CH2 Buffer

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00F7H	CH1/ENV1	EN7	EN 6	EN 5	EN 4	EN 3	EN 2	EN 1	EN 0	-	√
00F8H	CH2/ENV2	EN7	EN 6	EN 5	EN 4	EN 3	EN 2	EN 1	EN 0	-	√

```
LDA     Voice   ; Load 8-bit voice data to accumulator
STA     F7H     ;
```

※ Bit-manipulation instructions not available on this register.

17 AUD buffer transfer control

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00F9H	AB_TC	AEN	VTS6	TC5	TC4	-	VTS2	TC1	TC0	√	√

AB_TC is a voice or tone control register. When AEN is set as disable, the AUD+ and AUD- will be set to open drain high impendence. VTS6 and VTS2 are used to control the path of voice or tone. TC5~ TC3, TC2~TC0 are used to control the AUD buffer transfer method. Before disable all the AUD output, user must progress the fade out subroutine to avoid the noise burst.

AEN: AUD enable control. 0: disable, 1:enable
In STOP mode or halt mode, the AUD output must be turn off (set AEN to "0") to save power consumption.
VTS6: Ch 2 voice/tone control. 0: voice, 1:tone

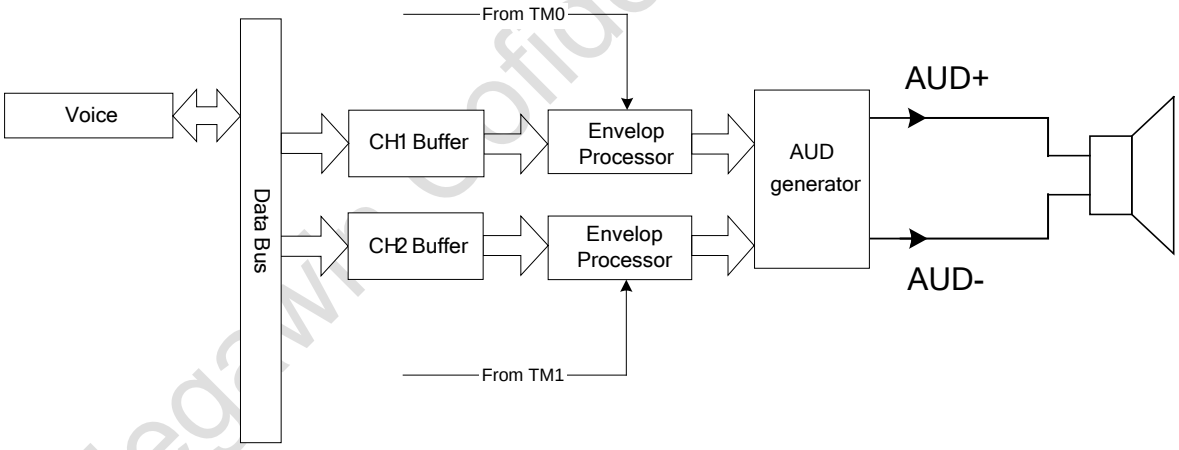
TC5	TC4	AUD buffer transfer control
0	0	Ch 2 buffer data transfer to AUD after TM0 underflow
0	1	Ch 2 buffer data transfer to AUD after TM1 underflow
1	0	Ch 2 buffer data transfer to AUD after TM2 underflow
1	1	Ch 2 buffer data transfer to AUD directly

VTS2: Ch 1 voice/tone control. 0: voice, 1:tone

TC1	TC0	AUD buffer transfer control
0	0	Ch 1 buffer data transfer to AUD after TM0 underflow
0	1	Ch 1 buffer data transfer to AUD after TM1 underflow
1	0	Ch 1 buffer data transfer to AUD after TM2 underflow
1	1	Ch 1 buffer data transfer to AUD directly

AUD output current

The drive current of AUD buffer is typically 180mA at V_{DD}=3volt. It is suit to direct drive a speaker or buzzer.



18 Option Register

Mask Option

Item	1 / 0
F_{OSC}	RC / Crystal
WDT	Enable / Disable
NMO F_{X32}	Enable / Disable

NMO F_{X32}: Non-Maskable Oscillator X32. The X32 cannot stop oscillating by MCLKmgr.CKC0 when it is enabled.

Typical Application (with RTC and with WDT)

Item	
F_{OSC}	RC
WDT	Enable
NMO F_{X32}	Enable

Application (without both RTC and WDT, connect X32I to GND)

Item	
F_{OSC}	RC or Crystal
WDT	Disable
NMO F_{X32}	Disable

Not Recommended Selection

Item	
F_{OSC}	RC or Crystal
WDT	Enable
NMO F_{X32}	Disable

19 Programming Notice

The status after different reset condition is listed below:

	Power on reset	CPU /RES pin reset
SRAM Data	Unknown	Unchanged
CPU Register	Unknown	Unknown
Special Function Register	Default value	Default value

20 Application Circuit

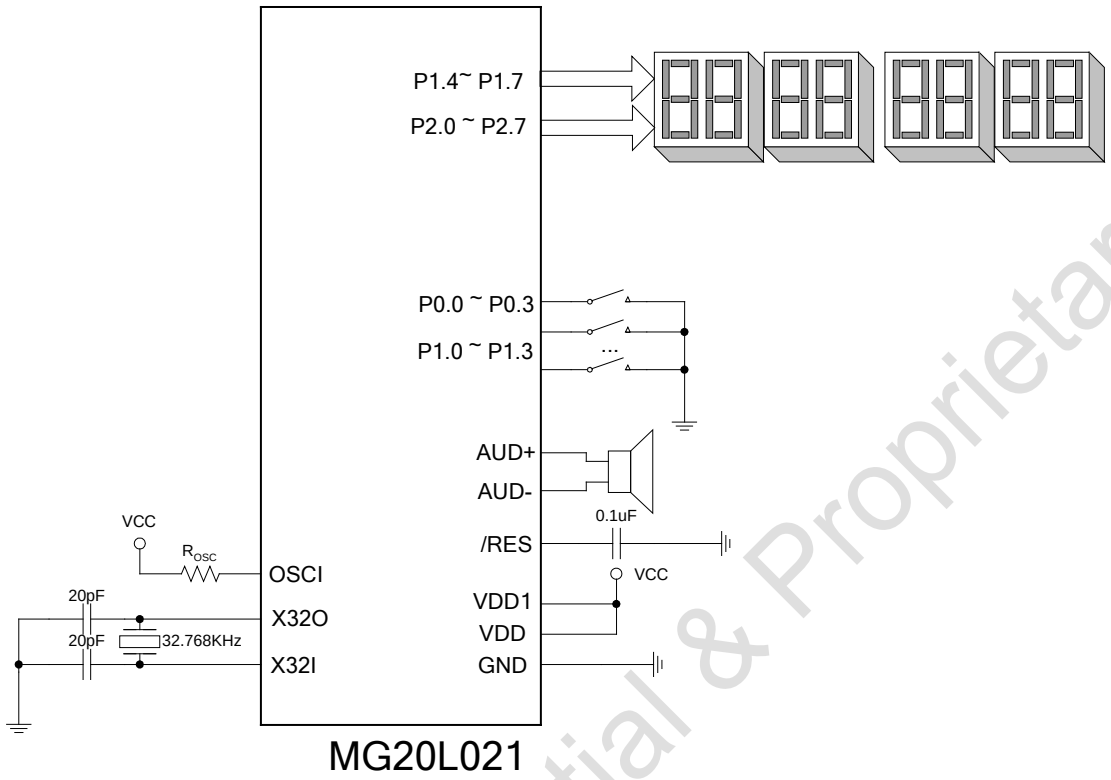


Figure 20-1 Application Circuit

21 Electrical Characteristics

21.1 Absolute Maximum Rating

PARAMETER	RATING	UNIT
Supply Voltage to Ground Potential	-0.3 to +4.0	V
Applied Input / Output Voltage	-0.3 to +4.0	V
Power Dissipation	800	mW
Ambient Operating Temperature	0 to +70	°C
Storage Temperature	-55 to +150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

21.2 DC Characteristics

(VDD-VSS = 3.0 V, F_{OSC} = 4MHz, Ta = 25° C; unless otherwise specified)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Op. Voltage	V_{DD}	-	1.8	-	3.6	V
Op. Current	I_{OP1}	No load (Ext.-V) In dual clock operation	-	2	5	mA
	I_{OP2}	No load (Ext.-V) In Slow mode operation	-	60	-	μA
Standby Current	I_{STB1}	Halt mode, No load, F_{CPU}=32768Hz, RTC INT off, NMO F_{X32} Disabled	-	5		μA
	I_{STB2}	Halt mode, No load, F_{CPU}=32768Hz, RTC INT ON, NMO F_{X32} Disabled	-	10		μA
	I_{STB3}	Stop mode, No load, NMO F_{X32} Disabled	-	1	3	μA
AUD+ buffer driving current	I_{AUD+}	R load = 8 Ω	-	180	-	mA
AUD- buffer driving current	I_{AUD-}	R load = 8 Ω	-	180	-	mA
Port 0 Input High Voltage	V_{IH1}	-	0.7 V_{DD}	-	V_{DD}	V
Port 1,2 Input High Voltage	V_{IH2}	Normal mode(SVIH=0)	0.7 V_{DD}	-	V_{DD}	V
		Special mode(SVIH=1)	0.9 V_{DD}	-	V_{DD}	V
Input Low Voltage	V_{IL}	-	0	-	0.3V_{DD}	V
Port 0 drive current	I_{OH0}	V_{OH} = 2.4V, V_{DD} = 3.0V	-	7	-	mA
Port 0 sink current	I_{OL0}	V_{OL} = 0.4V, V_{DD} = 3.0V	-	10	-	mA
Port 1, 2 drive current	I_{OH1}	V_{OH} = 2.4V, V_{DD} = 3.0V	-	7	-	mA
Port 1, 2 sink current	I_{OL1}	V_{OL} = 0.4V, V_{DD} = 3.0V	-	50	-	mA
Internal Pull-high Resistor	R_{PH}	V_{IL} = 0V	25K	50K	100K	Ω
Internal Pull-low Resistor	R_{PL}	V_{IH} = 3V	25K	50K	100K	Ω
/RES Pull-high Resistor	R_{RES}	V_{IL} = 0V	-	30K	-	Ω
Low Voltage Reset	V_{LVR}	-	-	1.8	-	V

21.3 AC Characteristics

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CPU OP. Frequency	F_{CPU}	V_{DD} = 3.0V	0.4	4	6	MHz
System Start-Up Time	T_{SST1}	Power-up, reset or wake-up from STOP mode ($F_{CPU} = F_{OSC}$)	-	16384	-	1/ F_{CPU}
	T_{SST2}	Wake-up from STOP mode ($F_{CPU} = F_{X32}$)	-	2048	-	1/ F_{CPU}

22 Revision History

Revision	Page	Descriptions	Date
V0.11		Original	2012/09/26
V0.12		Add Pin Configurations and SOP28 Package P.6	2012/09/28
V0.13		Modify IO_MFR[2] spec. description. P.27	2012/10/08
V0.14		Modify CWPR protect item. Delete BANK write protection. P.12	2012/10/19
V0.15		Modify Main Page Version 0.13->0.15	2012/10/20