AMERICAN MICROSYSTEMS, INC.

MG29C01
4-Bit Microprocessor

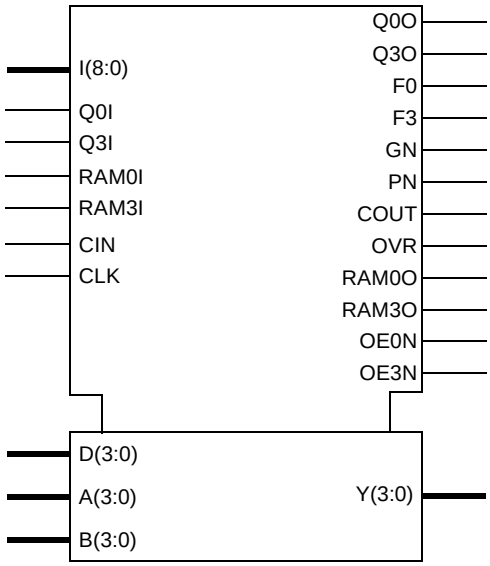
Digital Soft Megacells

Features

- A high-performance, low-power CMOS megacell featuring functional compatibility with the industry standard 2901
- 4-Bit cascadable bit-slice
- Eight function ALU including addition, two subtraction and five logic operations on two operands
- Microprogrammable with three groups of three bits each for ALU function, destination control and source operand
- Two address architecture provides independent access to two working registers
- Five source ports for data selection
- Four status flags including carry, zero, overflow and sign
- Equivalent gates:
  Standard Cell - 810; Gate Array - 1000

LOGIC SYMBOL

MG29C01



Description

MG29C01 is a high-performance 4-bit cascadable microprocessor.

The MG29C01 offers the designer a simple and methodical approach to designing bit-slice microprocessors, high-speed ALUs and boolean machines.

The MG29C01 consists of a fast ALU, a 16-word by 4-bit two port RAM and the required decoding, multiplexing and shifting circuits. The microinstruction word consists of nine bits divided into three groups. Bits 0-2 select the ALU source operads. Bits 3-5 select the ALU function and bits 6-8 select the destination register.

The ALU allows for several arithmetic functions which include: unsigned addition and subtraction, two's complement and one's complement addition and subtraction, and decrementing. The ALU also produces the status bits: overflow, carry-out, F0. Boolean functions offered include: AND, OR, XOR, XNOR, INVERT, PASS, ZERO, and MASK.

The MG29C01 also includes a 16-word by 4-bit register, a 4-bit Q register, and various sources for the ALU.

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS
I(8:0)	Input	The nine instruction lines.
CIN	Input	Carry in to the ALU.
CLK	Input	The clock input.
D(3:0)	Input	Data inputs. These data may be selected as one of the ALU sources. D(0) is the LSB.
A(3:0)	Input	The address inputs to the register stack, used to select which register's contents are available through the A port. A(0) is the LSB.
B(3:0)	Input	The address inputs to the register stack used to select which registers contents are available through the B port. B(0) is the LSB.
Q0O, Q3O Q0I, Q3I	I/O	The input and output shift lines for the LSB and MSB of the Q register, allow for shift up and shift down operations. Q3 is the MSB. Q0O is valid when OE0N is low and Q3O is valid when OE3N is low.
F0	Output	Becomes active when all four ALU outputs are low.
F3	Output	The most significant ALU output bit.
GN, PN	Output	The generate and propagate outputs of the ALU, can be used to for carry look-ahead.
COUT	Output	Carry out of the ALU.
OVR	Output	Overflow. Indicates the result of an arithmetic two's complement operation has overflowed into the sign bit.
OE0N	Output	A low on this pin indicates Q0O and RAM0O are valid.
OE3N	Output	A low on this pin indicates Q3O and RAM3O are valid.
RAM0O, RAM3O RAM0I, RAM3I	I/O	The input and output shift lines for the LSB and MSB of the register stack, allow for shift up and shift down operations. RAM3 is the MSB. RAM0O is valid when OE0N is low and RAM3O is valid when OE3N is low.
Y(3:0)	Output	Data outputs. These outputs are connected to either ALU or A port of the register stack.