AMERICAN MICROSYSTEMS, INC.

MG29C10
12-Bit Microprogram Controller

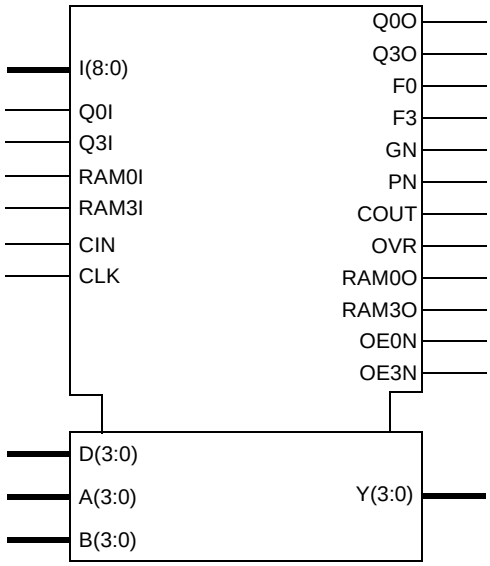
Digital Soft Megacells

Features

- A high-performance, low-power CMOS megacell featuring functional compatibility with the industry standard 2901
- 4-Bit cascadable bit-slice
- Eight function ALU including addition, two subtraction and five logic operations on two operands
- Microprogrammable with three groups of three bits each for ALU function, destination control and source operand
- Two address architecture provides independent access to two working registers
- Five source ports for data selection
- Four status flags including carry, zero, overflow and sign
- Equivalent gates:
  Standard Cell - 810; Gate Array - 1000

LOGIC SYMBOL

MG29C01



Description

MG29C10 is a high-performance 12-bit microprogram controller. It functions as an address sequencer for controlling the execution of microinstructions in microprogram memory.

It also controls conditional branching to any microinstruction within its 4096 word range. There are nine levels of subroutine nesting with return linkage and looping capability provided by a last-in, first-out stack.

The MG29C10 has four sources for providing the 12-bit address during each microinstruction. These four sources are as follows:

1. A direct external input.
2. A register/counter (R) which retains data loaded during an earlier microinstruction.
3. The last-in, first-out stack/file (F).
4. The address counter/register which usually increments the addresses.

The MG29C10 consists of six functional blocks: an instruction PLA, a multiplexer, a register/counter, a zero detector, a 9-word by 12-bit stack, a microprogram counter register, and an incrementer.

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS
CCN	Input	Used as test input criterion. Active low.
CCENN	Input	Enables CCN. Active low.
CI	Input	Carry input to the low order of the microprogram counter.
RLDN	Input	Forces loading of register/counter regardless of instruction or condition. Active low.
CLK	Input	Master input clock.
D(11:0)	Input	Direct data input to register/counter and multiplexer. D(0) is the LSB.
I(3:0)	Input	Instruction inputs. I(0) is the LSB.
FULLN	Output	Goes low when the internal stack is full. Active low.
PLN	Output	Used to select #1 source (usually a pipeline register) as the direct input source.
MAPN	Output	Used to select #2 source (usually a mapping ROM or PLA) as the direct input source.
VECTN	Output	Used to select #3 source (usually an interrupt starting address) as the direct input source.
Y(11:0)	Output	Address to microprogram memory. Y(0) is the LSB.