



**(Preliminary) MG39U301**

*Universal PWM Type LED Driver*

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# **MG39U301**

## **Data Sheet**

**Version: V1.03**

## **Features**

- Operation voltage, 7.0V ~ 500V
- Provide constant frequency or constant off-time control
- Open loop current peak detector
- Linear or PWM dimming control

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## 1 Description

The MG39U301 is a current feedback control, buck type LED driver IC. It achieves good output current regulation without the need of external compensation components.

The MG39U301 integrates a HV start-up circuit, 7.0V ~ 500V linear regulator, precision comparator, PWM control and ring oscillator into one chip. With those building circuits, a precision current output buck mode converter with dimming control (linear or PWM type) can be easily achieved with only few external components. The linear dimming control input is 0~0.25V & the PWM dimming range is 0~100% duty at a frequency of up to 10KHz.

The chip is available in 8-pin or 16-pin SOP package.

## 2 Order Information

	MG39U301ASC1	MG39U301ASC2
Package	SOP8	SOP16

## 3 Application Field

DC-DC or AC-DC LED driver application

Backlighting LED driver

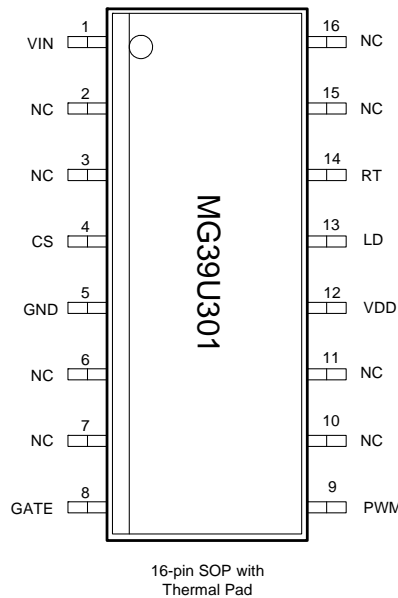
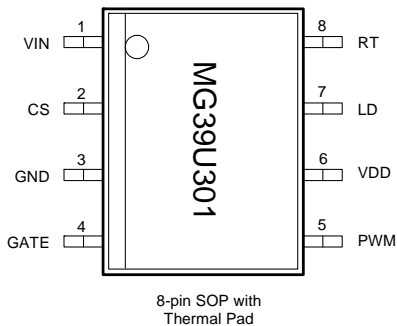
General-purpose constant current source

## 4 Pin Description

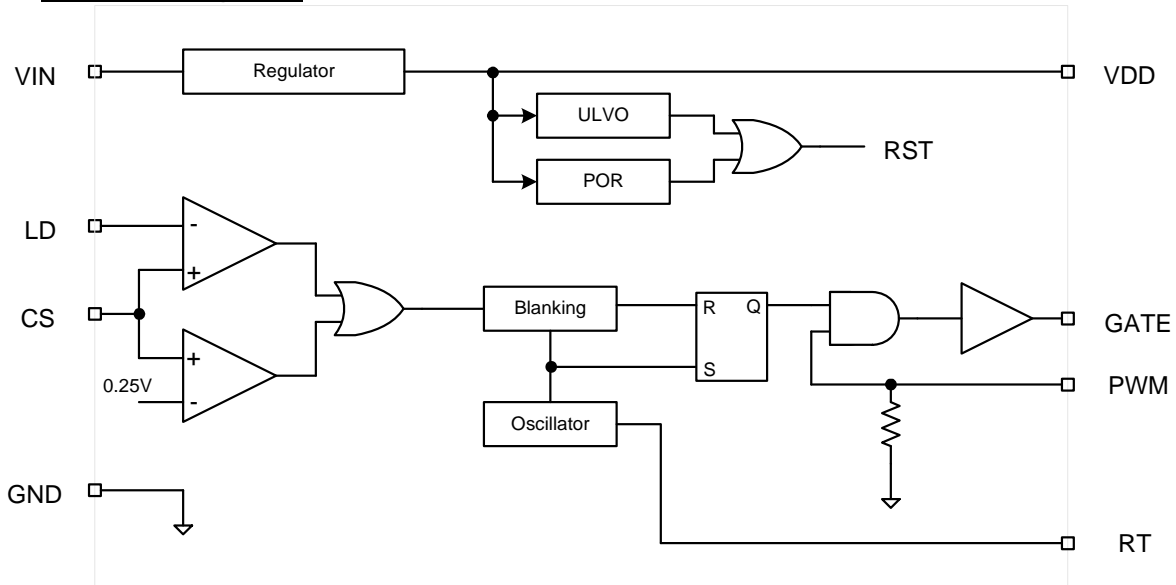
### 4.1 Pin Definition

SOP8	SOP16	Pin Name	Description
1	1	VIN	7.0~500V high voltage input.
2	4	CS	Current sense input pin.
3	5	GND	Ground pin.
4	8	GATE	Driver for external power MOS.
5	9	PWM	PWM dimming input.
6	12	VDD	Regulated core supply.
7	13	LD	Linear dimming input. If current sense threshold is required less than 0.25V, an external voltage can be applied to this pin.
8	14	RT	Ring oscillator bias input. When RT is connected to ground via a resistor, the MG39U301 operates in constant frequency mode. When the resistor is connected between RT & GATE, the MG39U301 operates in constant off-time mode.
-	2, 3, 6, 7, 10, 11, 15, 16	NC	No connection.

### 4.2 Pin Configuration

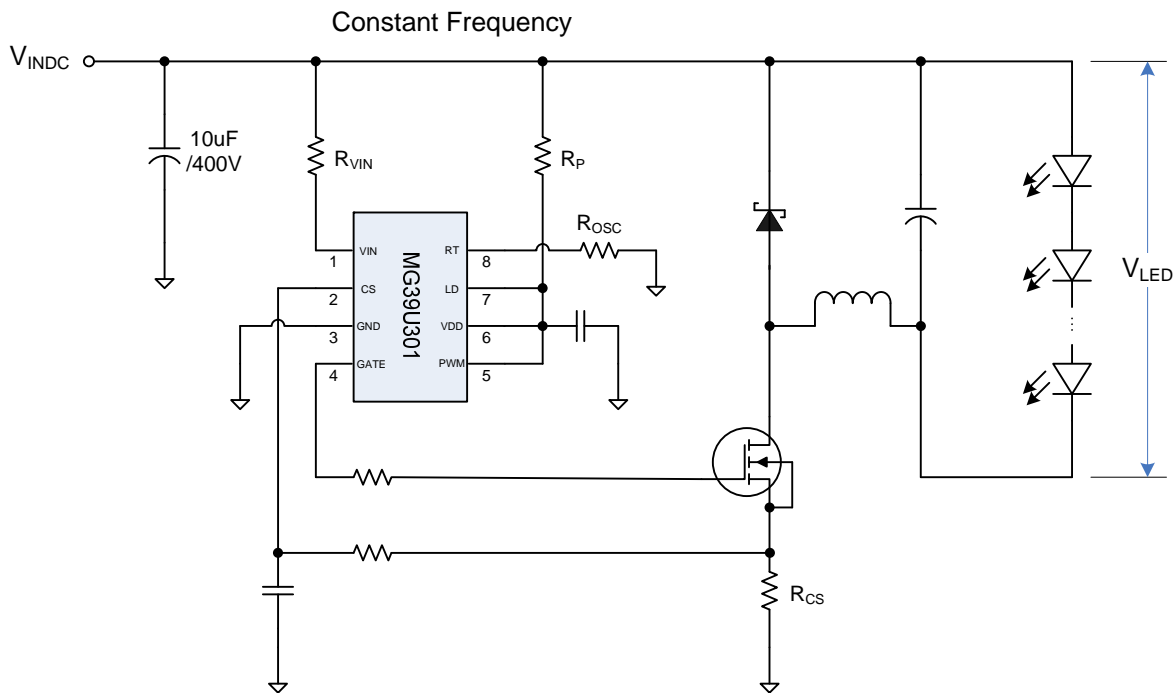


## 5 Block Diagram

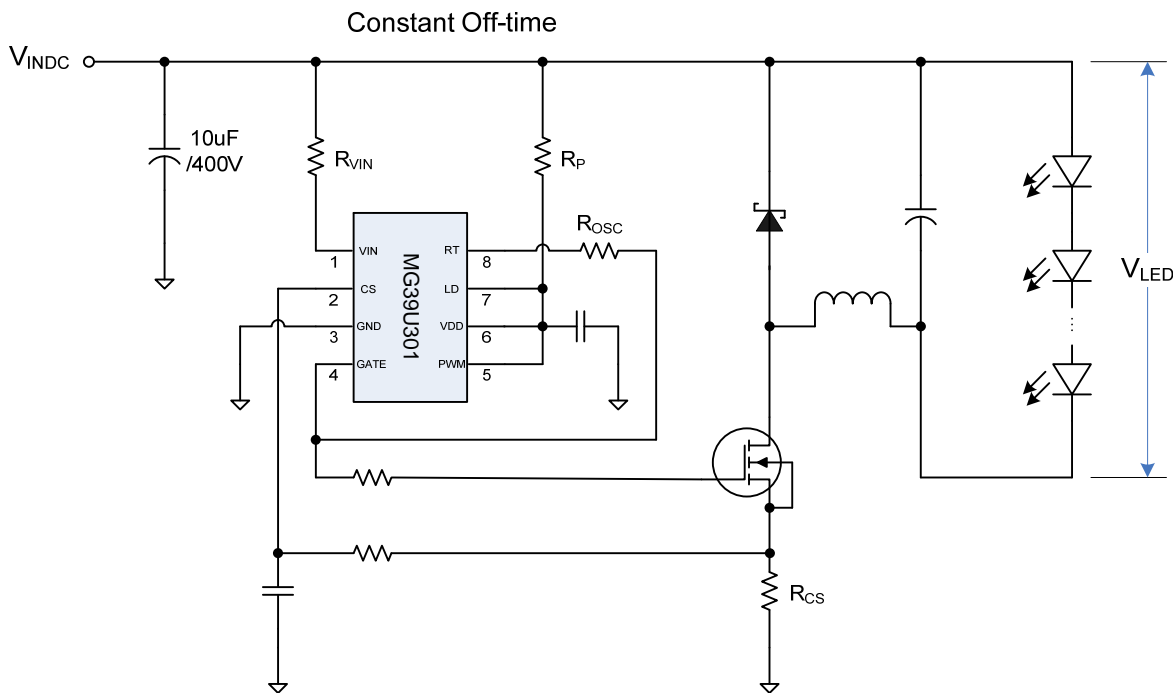


## 6 Application Circuit

Buck Driver Example 1



## Buck Driver Example 2



## 7 Application Information

### Input Voltage Regulator

The MG39U301 integrates one high voltage regulator to generate the power for internal core logic. The internal power is taken from the AC line directly. Extra auxiliary transformer is not needed for the supply. When a voltage (7~500V) is applied at the VIN pin, the regulator maintains a constant 5.6V at the VDD pin. The VDD pin must be bypassed by a low ESR capacitor to provide a low impedance path for the high frequency current of the output date driver.

Since the current driving capability of the regulator is limited to around 0.7mA. It's not suitable for driving the external components. User must make sure the switching frequency should not be too high and the load at the GATE pin should not be too heavy.

It's recommended to add a series resistor between  $V_{INDC}$  and VIN pin to protect the IC. Basically, several ten K to 100K ohms are recommended. The voltage drop on the resistor can be calculated as  $V_{RDROP} = I_{OP} \times R_{VIN}$ .

For large  $I_{LED}$  application, it's recommended to add a pull-high resistor ( $R_P$ ) between  $V_{INDC}$  and VDD pin to provide more driving current.

### Selection of the Switching Control Scheme

The MG39U301 provides two control schemes, constant frequency and constant off time. For a buck converter, the duty of PWM control signal is determined as  $D = V_O / V_{IN}$ , where  $V_O$  is the voltage drop on LED strings ( $V_{LED}$ ). For a heavy load application (large  $V_{LED}$  drop,  $D > 0.45$ ), user should select the constant off time mode.

### Selection of the Switching Frequency ( $F_s$ )

Rule of thumb, the range of 20KHz ~ 100KHz is recommended.

For detail frequency setting, please check application note "AN\_MG39U301\_ROSC SEL".

### GATE Output

The GATE output of the MG39U301 is used to drive an external MOSFET. It is recommended that the gate charge  $Q_G$  of the external MOSFET should satisfy the equation as below:

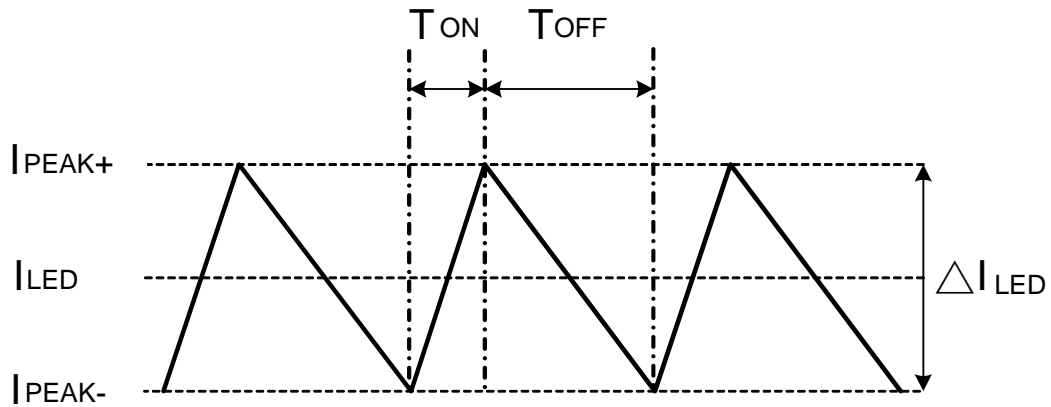
$$(V_{INDC} - 5.6V)/R_P + 0.7mA \geq F_s * Q_G$$

In the above equation,  $Q_G$  is the GATE charge of the external FET obtained from the manufacturer's datasheet.

### Selection of the Sense Resistor ( $R_{CS}$ )

The MG39U301 is an open loop buck converter with peak current control. The peak current is decided by the equation  $I_{PEAK+} = V_{CSTH} / R_{CS}$ , where  $V_{CSTH}$  is around 0.27V. The average current ( $I_{LED}$ ) is described as follow:

The  $\Delta I_{LED}$  is determined by  $T_{OFF}$ , L value and  $V_{LED}$  load.





## 8 Absolute Maximum Rating

Parameter	Rating	Unit
VIN to GND	-0.5 to +525	V
VDD to GND	7	V
CS, LD, PWM, GATE, RT to GND	-0.3 to (V <sub>DD</sub> + 0.3)	V
Junction Temperature	-40 to +125	°C
Storage temperature	-55 to +155	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

## 9 Electrical Characteristics

All typical numbers are at Ta=25°C and VIN=12V, unless otherwise noted.

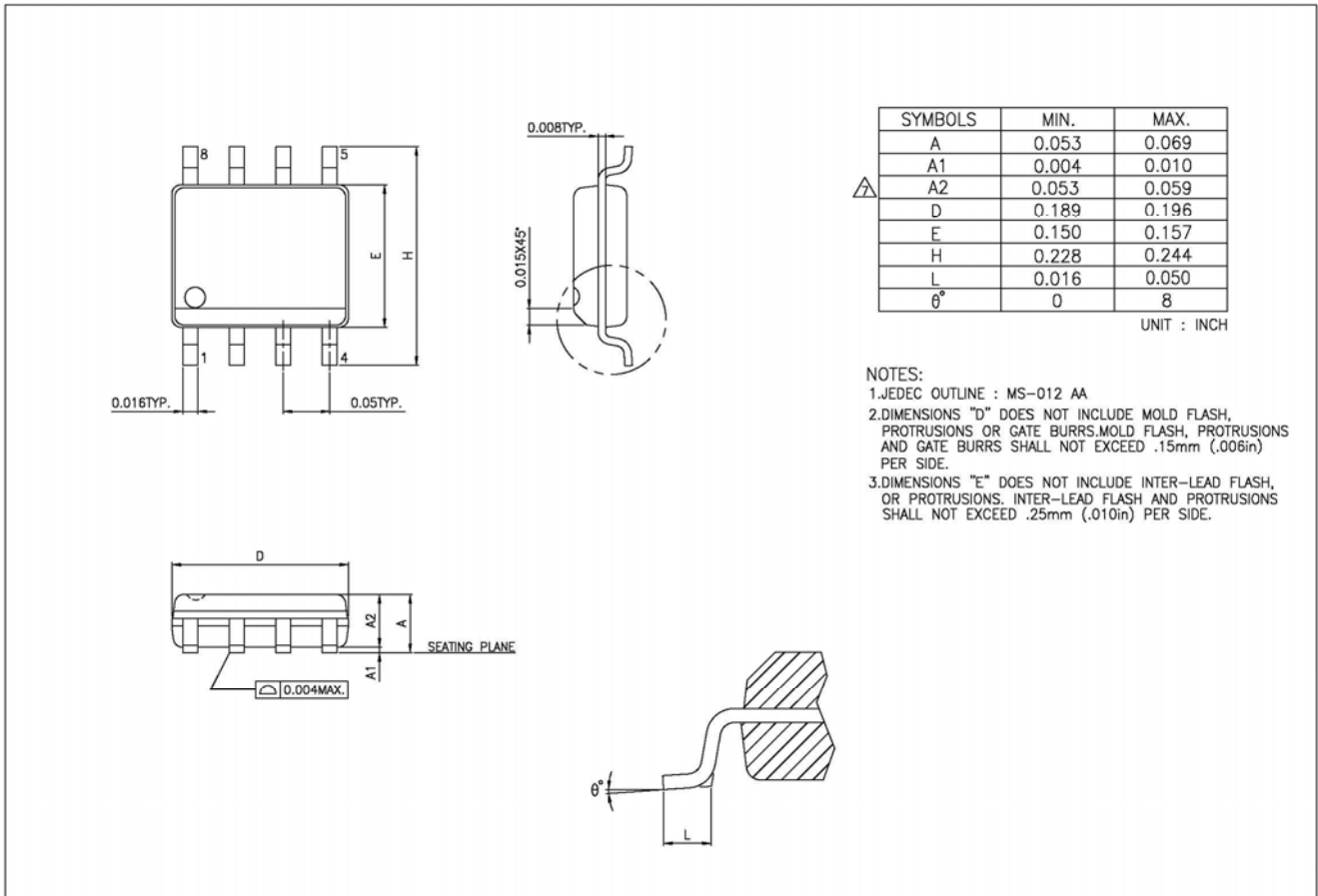
Parameter	Sym.	Conditions	Min.	Typ.	Max.	Unit
Input DC supply voltage range	V <sub>INDC</sub>	DC input voltage	7.0	-	500	V
Shut down mode supply current	I <sub>INSD</sub>	PWM=0, V <sub>IN</sub> =7.5V	-	0.5	0.7	mA
Operating Current	I <sub>OP</sub>	V <sub>IN</sub> > 7.5V, R <sub>OSC</sub> =226K and C <sub>GATE</sub> =500P	-	0.8	1.2	mA
<b>Internal Regulator</b>						
Internally regulated Voltage	V <sub>DD</sub>	V <sub>IN</sub> =7.5V ~ 200V, R <sub>OSC</sub> =226K, C <sub>GATE</sub> = 500pF, No load in pin VDD	5.0	5.6	6.0	V
Maximal pin VDD voltage	V <sub>DDMAX</sub>	When an external voltage applied to pin VDD	-	-	7.0	V
Output current of the regulator	I <sub>SOURCE</sub>	V <sub>DD</sub> = 5.6V	-	0.7	-	mA
VDD under-voltage lockout threshold	V <sub>UVLO</sub>	V <sub>IN</sub> rising	-	5.30	-	V
VDD under-voltage lockout hysteresis	ΔUVLO	V <sub>IN</sub> falling	100	300	500	mV
<b>PWM Dimming</b>						
Pin PWM input high voltage	V <sub>PWM(H)</sub>	V <sub>IN</sub> =7.5V ~ 500V	2.0	-	-	V
Pin PWM input low voltage	V <sub>PWM(L)</sub>	V <sub>IN</sub> =7.5V ~ 500V	-	-	0.8	V
Pin PWM pull-down resistance	R <sub>PWM</sub>	V <sub>DD</sub> =5.5V	50	100	150	KΩ
PWM signal duty	D <sub>PWM</sub>		0	-	100	%
<b>Current Sense Input</b>						
Current sense pull-in threshold voltage	V <sub>CSTH</sub>	Ta= 0°C to +125°C, V <sub>DD</sub> = 5.6V	255	275	285	mV
		Ta= -40°C, V <sub>DD</sub> = 5.6V	200	-	-	mV
Offset voltage of comparator	V <sub>OS</sub>		-20	-	20	mV
Linear dimming pin voltage range	V <sub>LD</sub>		0	-	V <sub>CSTH</sub>	mV

## Electrical Characteristics (continued)

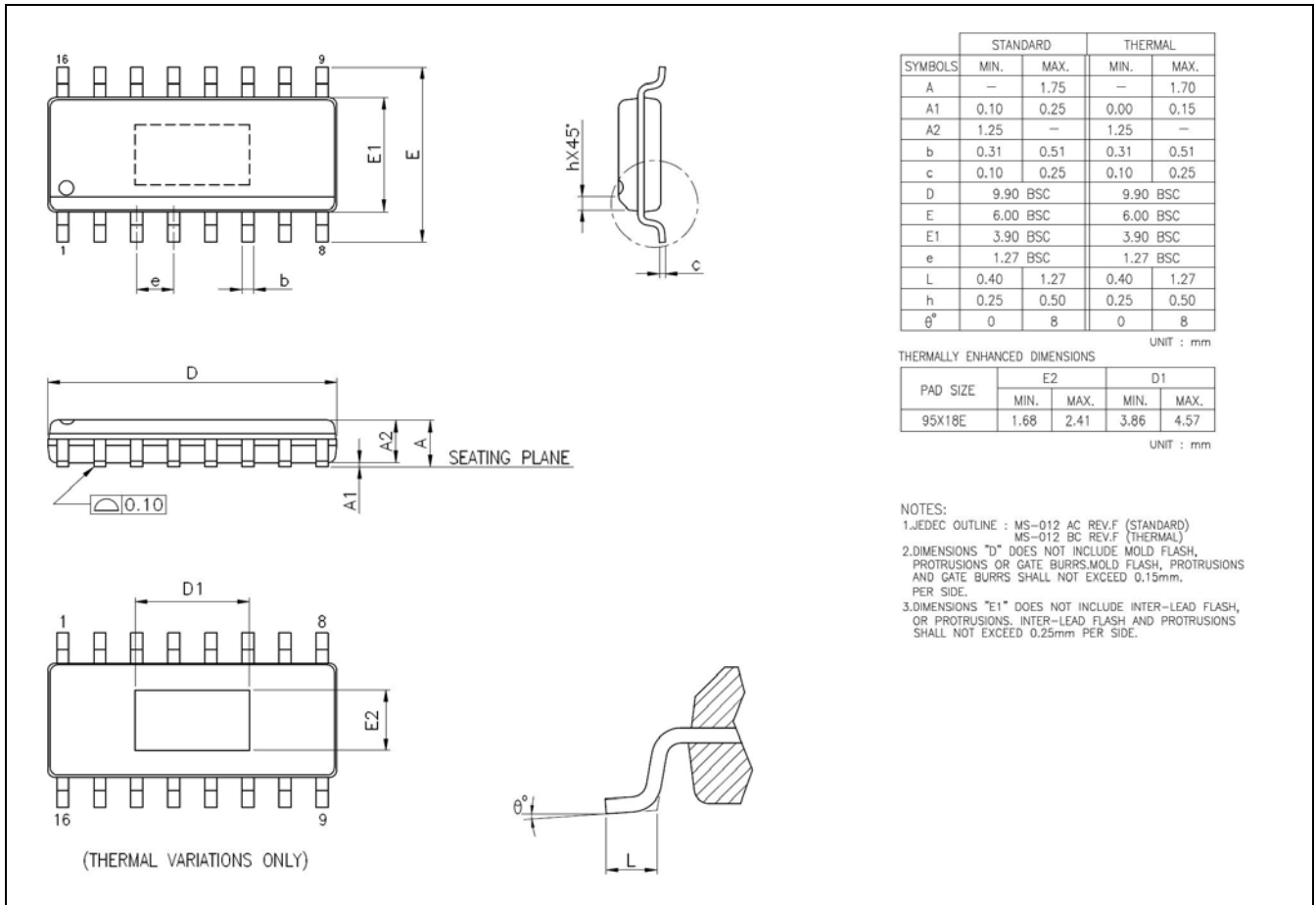
Current sense blanking interval	$t_{\text{BLANK}}$	$V_{\text{CS}}=0.55 V_{\text{LD}}, V_{\text{LD}}=V_{\text{DD}}$	150	215	285	nS
Delay from CS trip to GATE IO	$t_{\text{DELAY}}$	$V_{\text{LD}}=V_{\text{DD}}, V_{\text{CS}}= V_{\text{CSTH}} +50\text{mV}$ after $t_{\text{BLANK}}$	-	-	300	nS
<b>Gate Driver</b>						
GATE output high voltage	$V_{\text{GATE (H)}}$		$V_{\text{DD}} -0.4$	-	-	V
GATE output low voltage	$V_{\text{GATE (L)}}$		-	-	0.4	V
GATE output high driving current	$I_{\text{GATE (H)}}$	$V_{\text{GATE}}= V_{\text{DD}}-0.4\text{V}$	-	10	-	mA
GATE output low sinking current	$I_{\text{GATE (L)}}$	$V_{\text{GATE}}= 0.4\text{V}$	-	25	-	mA
GATE output rise time	$t_{\text{RISE}}$	$C_{\text{GATE}} = 500\text{pF}$	-	30	50	nS
GATE output fall time	$t_{\text{FALL}}$	$C_{\text{GATE}} = 500\text{pF}$	-	30	50	nS
<b>Oscillator</b>						
Oscillator frequency	$F_{\text{OSC}}$	$R_{\text{OSC}}= 1.0\text{M}\Omega$	22K	27K	32K	Hz
		$R_{\text{OSC}}= 226\text{K}\Omega$	90K	110K	120K	

# 10 Package Dimension

## 10.1 SOP8 Package Dimension



## 10.2 SOP16 Package Dimension



## 11 Revision History

Rev	Descriptions	Date
V0.10	Initial release.	2013/01/05
V0.20	Modify the supply voltage range.	2013/03/05
V0.30	Modify the application circuit and add gate output notification.	2013/06/14