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1 Features

- Operation voltage, 8.0V ~ 500V
- Fast average current control
- Programmable constant off-time switching
- Output short circuit protection with skip mode
- Linear and PWM dimming input
- Ambient operating temperature: -40°C to+125°C
- Pin-to-pin compatible with the MG39U301

2 Description

The MG39U302 is an average current mode control LED driver IC operating in a constant off-time mode. Unlike MG39U301, this control IC does not produce a peak-to-average error, and therefore greatly improves accuracy, line and load regulation of the LED current without any need for loop compensation or high-side current sensing. The output LED current accuracy is ±3%.

The MG39U302 is equipped with a current limit comparator for hiccup mode output short circuit protection.

The MG39U302 can be powered from an 8.0V ~ 500V supply. A PWM dimming input is provided that accepts an external control TTL compatible signal. The output current can be programmed by an internal 272mV reference, or controlled externally through a 0 ~ 1.5V dimming input.

MG39U302 is pin-to-pin compatible with MG39U301 and it can be used as a drop-in replacement for many applications to improve the LED current accuracy and regulation.

The chip is available in 8-pin or 16-pin SOP package.

3 Order Information

	MG39U302ASC1	MG39U302ASC2
Package	SOP8	SOP16

4 Application Field

DC-DC or AC-DC LED driver applications

Backlight driver for LCD displays

General-purpose constant current source

LED signage and displays

Architectural and decorative LED lighting

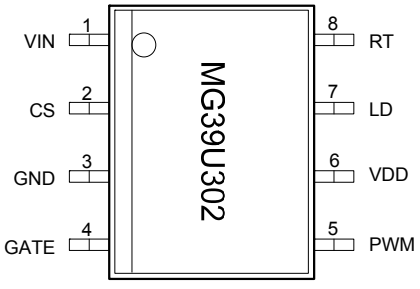
LED street lighting

5 Pin Description

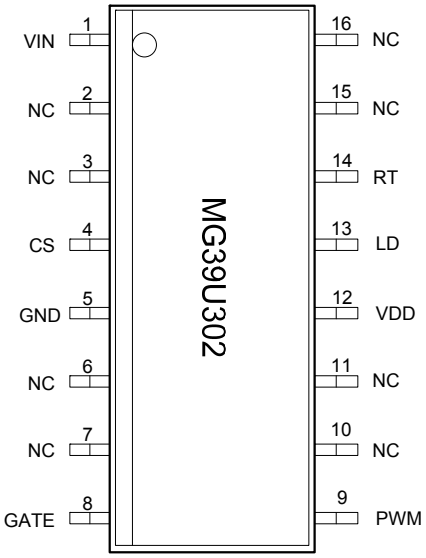
5.1 Pin Definition

SOP8	SOP16	Pin Name	Description
1	1	VIN	8.0V~500V linear regulator input.
2	4	CS	The current sense input pin used to sense the FET current by means of an external sense resistor.
3	5	GND	Ground pin. Ground return for all internal circuitry. This pin must be electrically connected to the ground of the power train.
4	8	GATE	This pin is the output GATE driver for an external N-channel power MOSFET.
5	9	PWM	This is the PWM dimming input of the IC. When this pin is pulled to GND, the gate driver is turned off. When the pin is pulled high, the gate driver operates normally.
6	12	VDD	This is the power supply pin for all internal circuits. It must be bypassed with a low ESR capacitor to GND (at least 0.1μF).
7	13	LD	This pin is the linear dimming input, and it sets the current sense threshold as long as the voltage at this pin is less than 1.5V. If voltage at LD falls below 150mV, the GATE output is disabled. The GATE signal recovers at 200mV at LD.
8	14	RT	A resistor connected between this pin and GND programs the GATE off-time.
-	2, 3, 6, 7, 10, 11, 15, 16	NC	No connection.

5.2 Pin Configuration

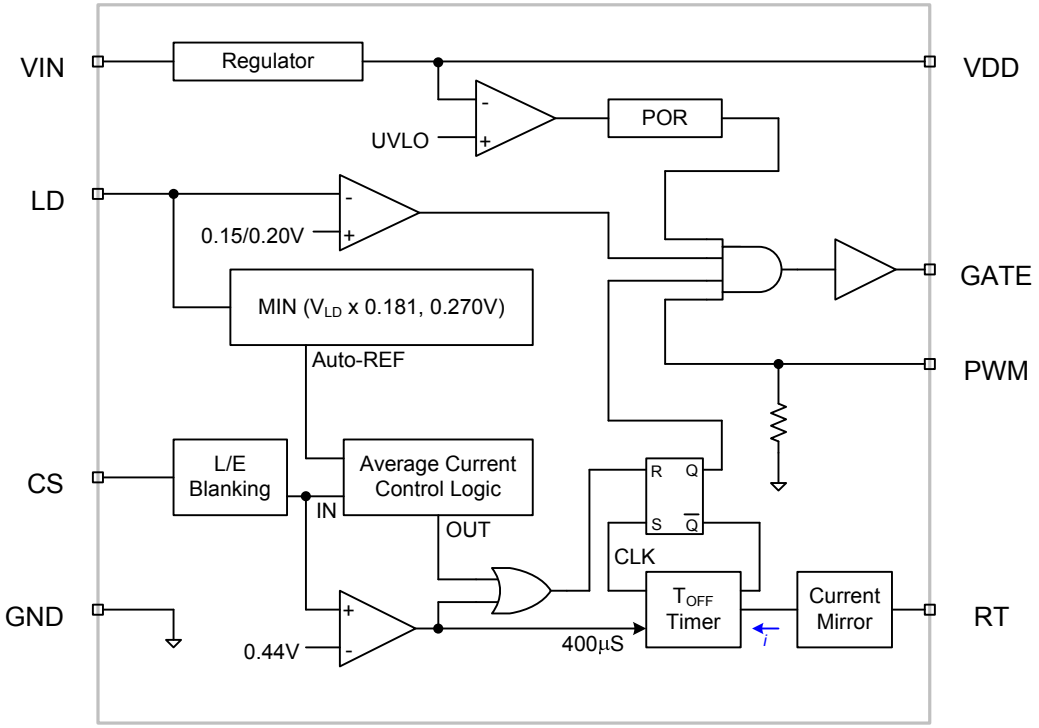


8-pin SOP with Thermal Pad



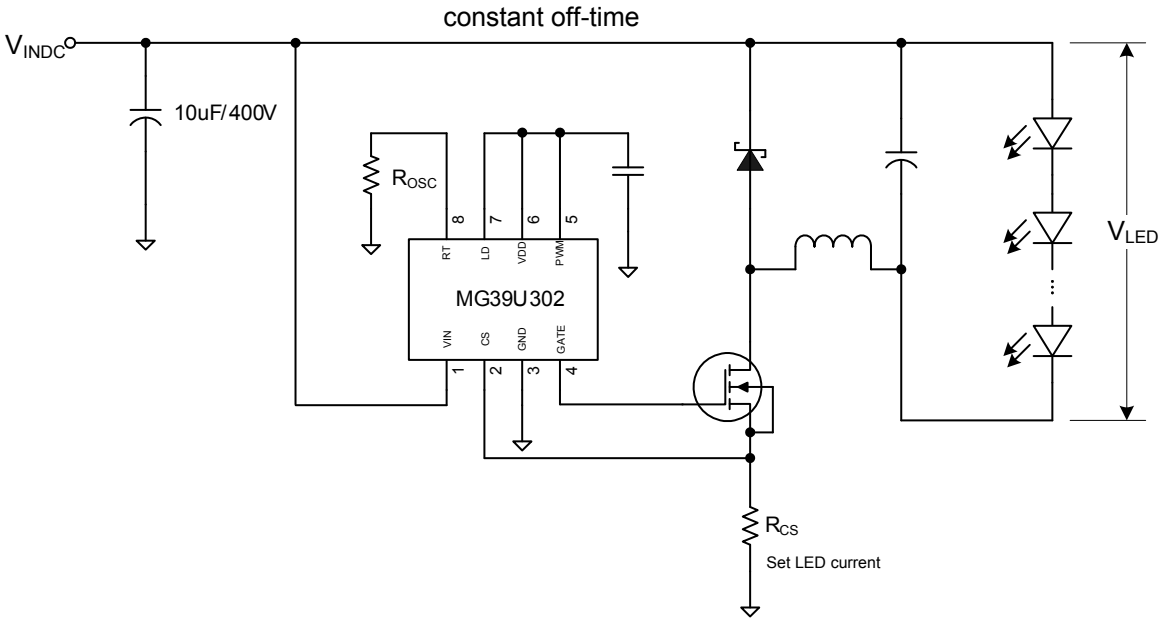
16-pin SOP with Thermal Pad

6 Block Diagram



7 Application Circuit

Buck Driver Example



8 Absolute Maximum Rating

Parameter	Rating	Unit
VIN to GND	-0.5 to +525	V
VDD to GND	12	V
CS, LD, PWM, GATE, RT to GND	-0.3 to (V_{DD} + 0.3)	V
Junction Temperature	-40 to +125	°C
Storage temperature	-55 to +155	°C
Continuous power dissipation (Ta=25°C) 8-pin SOP 16-pin SOP	 650 1000	 mW mW

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

9 Electrical Characteristics

All typical numbers are at Ta=25°C, V_{IN}=12V, V_{LD} = VDD and PWM = VDD, unless otherwise noted.

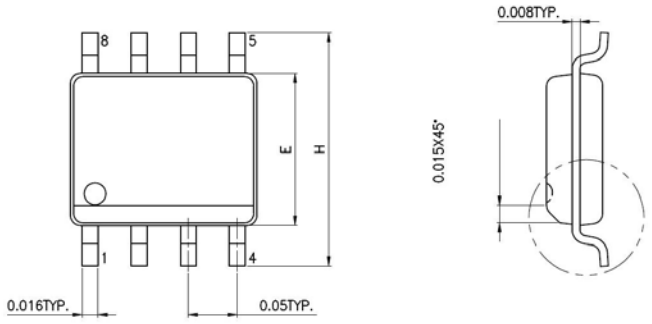
Parameter	Sym.	Conditions	Min.	Typ.	Max.	Unit
Input						
Input DC supply voltage range	V_{INDC}	DC input voltage	8	-	500	V
Shut down mode supply current	I_{INSD}	PWM=0, V_{IN}=8V	-	0.5	1.0	mA
Internal Regulator						
Internally regulated Voltage	VDD	V_{IN}=8V, R_{OSC}=226K, C_{GATE} = 500pF, No load in pin VDD	7.25	7.5	7.75	V
Line regulation of VDD	$\Delta V_{DD,LINE}$	V_{IN}=8V ~ 500V, R_{OSC}=226K, C_{GATE} = 500pF, No load in pin VDD	0	-	1.0	V
Line regulation of VDD	$\Delta V_{DD,LOAD}$	R_{OSC}=226K, C_{GATE} = 500pF, $I_{DD(EXT)}$ = 0~ 1.0mA	0	-	100	mV
VDD under-voltage lockout threshold	V_{UVLO}	V_{IN} rising	6.45	6.70	6.95	V
VDD under-voltage lockout hysteresis	ΔUVLO	V_{IN} falling	-	500	-	mV
Maximum input current (limited by UVLO)	$I_{IN,MAX}$	V_{IN}=8V, Ta=25°C	3.5	-	-	mA
		V_{IN}=8V, Ta=125°C	1.5	-	-	mA
PWM Dimming						
Pin PWM input high voltage	$V_{PWM\ (H)}$	V_{IN}=8V ~ 500V	2.0	-	-	V
Pin PWM input low voltage	$V_{PWM\ (L)}$	V_{IN}=8V ~ 500V	-	-	0.8	V
Pin PWM pull-down resistance	R_{PWM}	V_{PWM}=5.0V	50	100	150	KΩ

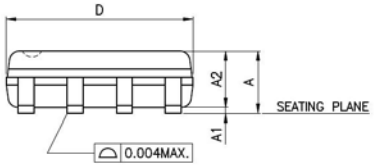
Electrical Characteristics (continued)

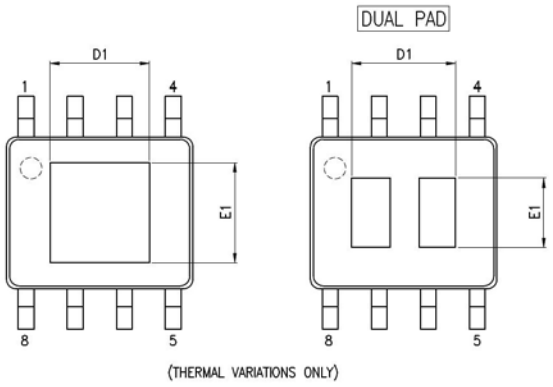
Average Current Sense Logic						
Current sense reference voltage	V_{CS}	-	264	-	280	mV
LD-to-CS voltage ratio	$A_{V(LD)}$	-	0.176	-	0.187	-
LD input voltage, shutdown	$V_{LD(OFF)}$	V_{LD} falling	-	150	-	mV
LD input voltage, enable	$\Delta V_{LD(OFF)}$	V_{LD} rising	-	200	-	mV
Current sense blanking interval	t_{BLANK}	-	150	-	320	nS
Minimum on-time	$t_{ON(MIN)}$	CS = V_{CS} + 30mV	-	-	1000	nS
Maximum steady-state duty cycle	D_{MAX}	Reduction in output LED current may occur beyond this duty cycle	75	-	-	%
Short Circuit Protection						
Hiccup threshold voltage	$V_{CS\ (HIC)}$	-	410	-	470	mV
Current limit delay CS-to-Gate	t_{DELAY}	CS = V_{CS} + 30mV	-	-	150	nS
Short circuit hiccup time	t_{HICCUP}	-	350	-	550	µS
Minimum on-time (short circuit)	$t_{ONS(MIN)}$	CS = V_{DD}	-	-	430	nS
T_{OFF} Timer						
Off time	t_{OFF}	R_{OSC} = 1.00MΩ	32	40	48	µS
		R_{OSC} = 226KΩ	8	10	12	µS
Gate Driver						
GATE source current	$I_{GATE\ (H)}$	V_{GATE}= V_{DD}-0.4V, V_{DD}= 7.5V	165	-	-	mA
GATE sinking current	$I_{GATE\ (L)}$	V_{GATE}= 0.4V, V_{DD}= 7.5V	165	-	-	mA
GATE output rise time	t_{RISE}	C_{GATE} = 500pF, V_{DD}= 7.5V	-	30	50	nS
GATE output fall time	t_{FALL}	C_{GATE} = 500pF, V_{DD}= 7.5V	-	30	50	nS

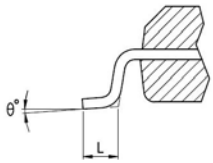
10 Package Dimension

10.1 SOP8 Package Dimension









	STANDARD		THERMAL	
SYMBOLS	MIN.	MAX.	MIN.	MAX.
A	0.053	0.069	0.053	0.067
A1	0.004	0.010	0.000	0.006
A2	0.053	0.059	0.049	0.059
D	0.189	0.196	0.189	0.196
E	0.150	0.157	0.150	0.157
H	0.228	0.244	0.228	0.244
L	0.016	0.050	0.016	0.050
θ°	0	8	0	8

UNIT : INCH

THERMALLY ENHANCED DIMENSIONS

PAD SIZE	E1		D1	
	MIN.	MAX.	MIN.	MAX.
90X90E	0.077	0.090	0.077	0.090
95X13E	0.081	0.095	0.111	0.130
96X65E(DUAL PAD)	0.070	0.096	0.114	0.140

UNIT : INCH

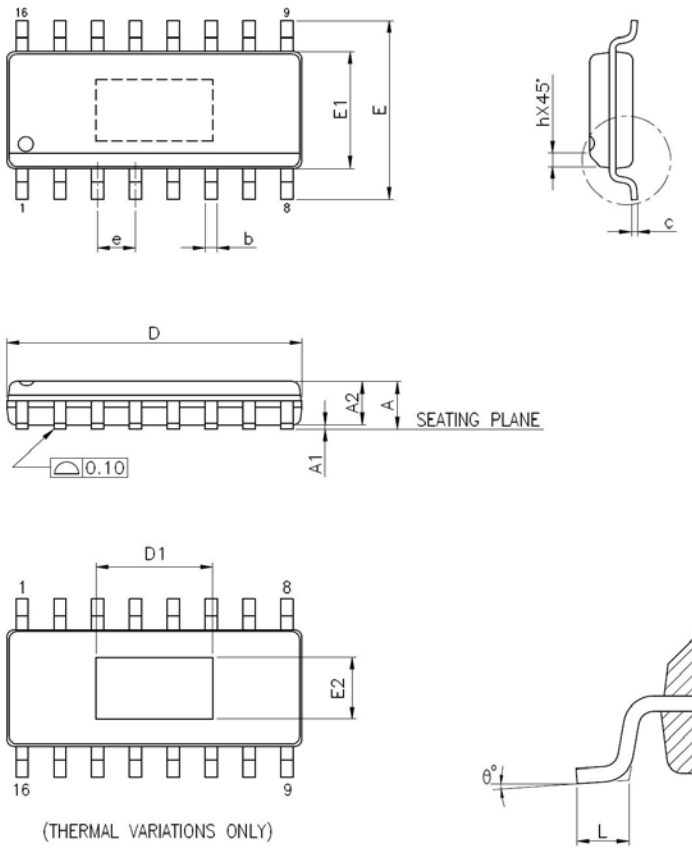
NOTES:

1.JEDEC OUTLINE : MS-012 AA(STANDARD)
MS-012 BA(THERMAL)

2.DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.006in) PER SIDE.

3.DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.

10.2 SOP16 Package Dimension



SYMBOLS	STANDARD MIN.	STANDARD MAX.	THERMAL MIN.	THERMAL MAX.
A	–	1.75	–	1.70
A1	0.10	0.25	0.00	0.15
A2	1.25	–	1.25	–
b	0.31	0.51	0.31	0.51
c	0.10	0.25	0.10	0.25
D	9.90 BSC		9.90 BSC	
E	6.00 BSC		6.00 BSC	
E1	3.90 BSC		3.90 BSC	
e	1.27 BSC		1.27 BSC	
L	0.40	1.27	0.40	1.27
h	0.25	0.50	0.25	0.50
θ°	0	8	0	8

UNIT : mm

THERMALLY ENHANCED DIMENSIONS

PAD SIZE	E2 MIN.	E2 MAX.	D1 MIN.	D1 MAX.
95X18E	1.68	2.41	3.86	4.57

UNIT : mm

NOTES:
1.JEDEC OUTLINE : MS-012 AC REV.F (STANDARD)
MS-012 BC REV.F (THERMAL)
2.DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15mm. PER SIDE.
3.DIMENSIONS "E1" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25mm PER SIDE.

11 Revision History

Version	Date	Page	Description
V1.01	2011/10/03		Initial release.
V1.02	2012/10/01	2, 3, 5	Modify the operation voltage range.