AMERICAN MICROSYSTEMS, INC.

MG65C02
8-Bit Core Microprocessor

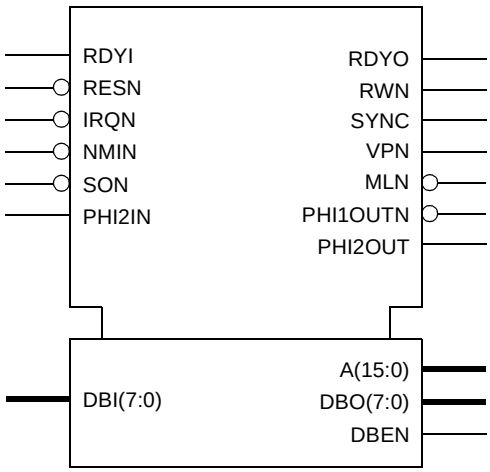
Digital Soft Megacells

Features

- High-performance, schematic-based megacell
- Functional compatibility with the industry standard 6502
- 8-Bit Microprocessor
- Fully Static Design
- 0-33 MHz Operation
- 64 kbytes Program Address Space
- Enhanced Instruction Set
- Supports Bit Manipulation
- 72 instructions and 212 opcodes
- 15 address modes
- Interrupt Capability
- Equivalent gates:
  Standard Cell - 2,950; Gate Array - 3,850

LOGIC SYMBOL

MG65C02



Description

MG65C02 is an 8-bit microprocessor which is compatible with the industry standard W65C02S. It has been designed to be compatible with both the original NMOS 6502 and the newer CMOS variations from various vendors.

The MG65C02 runs all 6502 opcodes as well as the new Enhanced Instruction set which include the new bit manipulation opcodes - RMB, SMB, BBR, BBS, and WAI and STP instructions. The latest functions are also incorporated in the MG65C02 such as Bus Enable, Vector-Pull, and Memory Lock. It accesses 65 kbytes of addressable Memory. It is fully static allowing the external clock to stop in either state. Operation frequency follows a range of 0 MHz, for low power or standby modes, to more than 25 MHz for high speed applications.

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS
A0-A15	O	Address to memory.
DBO0-DBO7	O	Data bus output. Valid when DBEN is high.
DBI0-DBI7	I	Data bus Input. Should be valid when DBEN is low.
DBEN	O	Data Bus Enable.
RDYI	I	Ready Input, active low. Stops the internal clock.
RDYO	O	Ready Output. The WAI instruction uses this pin to bring RDYI low.
RESN	I	Active low Reset.
IRQN	I	Active low Interrupt.
NMIN	I	Active low Non-maskable interrupt.
SON	I	Active low sets the overflow bit in the status word.
RWN	O	Read/Write. Active low for write.
SYNC	O	Synchronize. Active during opcode fetch cycle.
VPN	O	Vector Pull, active low. Low during interrupt vector access.
MLN	O	Memory Lock, active low. Low during Read-Modify-Write (RMW) portion of RMW instructions.
PHI2IN	I	Clock.
PHI1OUTN	O	Clock. Out of phase with C2IN.
PHI2OUT	O	Clock. In phase with PHI2IN. It also goes high with the STP instruction.