Version: 2.1

MG65L566A

Data Sheet

8-Bit Micro-Controller with 120 dots LCD driver

Version 2.1

Table of Contents

1 Features

- Single Chip 8-bit CPU
- Memory
  - Program ROM : 64K Bytes
  - Data RAM : 128 Bytes
  - LCD display RAM : 16 Bytes
- Operating voltage: 1.8V to 3.6V
- 17 Programmable GPIO
  - Direct IR output
  - Input/output pins P0[7:0]
  - Shared output pins:
    - ✧ Open Drain Output P1[7:0] / Segmen29 ~ Segmen22
- LCD driver output
  - 30 segment, 4 common
  - 1/4 duty 1/3 bias driving mode
- Watchdog timer built-in
- Two re-loadable 8-bit timers
- HALT mode and STOP mode for power saving
- Build-in dual oscillation circuit:
  - RC type main oscillator
  - X32 for sub-oscillator
  - Dual clock operation
- Build-in low voltage detector (typical voltage: below 2.3V) and low voltage reset (typical voltage: below 1.8V)

1.1 Application Field

General IR Controller, Hand-held Game, Toy

2 General Description

MG65L566A is a cost effective, high performance 8-bit micro-controller of MEGAWIN. It integrates an 8-bit CPU core, ROM, RAM, timers, LCD driver, I/O ports and system control circuits into a single chip. The MG65L566A provides a build-in oscillator as clock source. It is suitable for general IR controller, hand-held game, toy controllers, and other products.

3 Pin Configurations

3.1 Pad Assignment

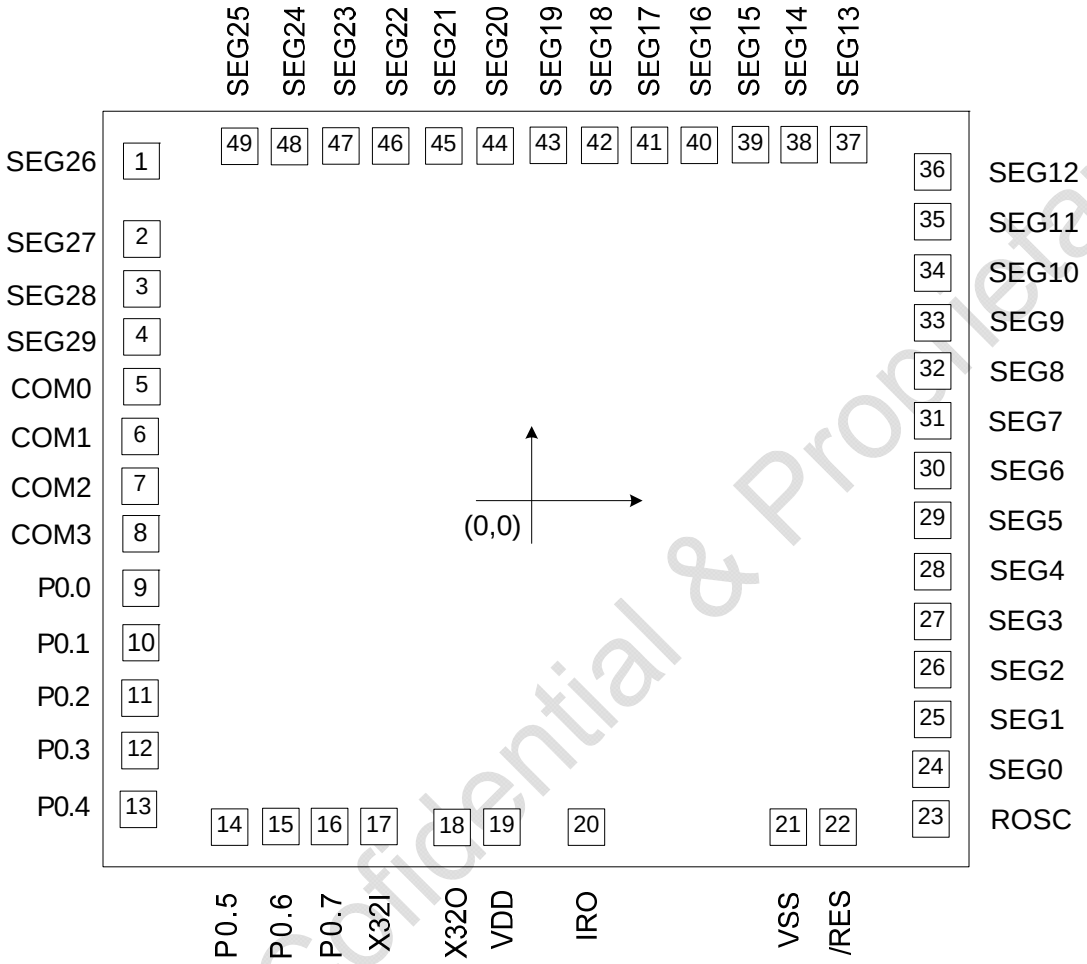


Figure 3-1 Pad Assignment

3.2 Pin Description

Table 3-1 Pin Description

Pad	Name	Type	Description
13 ~ 16	P0.4 ~ P0.7	I/O	Programmable I/O ports with interrupt and wake up function.
17,18	X32I, X32O	I/O	32.768KHz crystal oscillator pins.
19	VDD	P	Positive power pins (need to connect together)
20	IRO	O	IR carrier output. Direct sink (sink current: 250mA) for IR LED. Default value is high after reset.
21	VSS	P	Ground pins (need to connect together)
22	/RES	I	System reset pin (low active).
23	ROSC	I	RC oscillator input pin.
24 ~ 45	SEG0 ~ SEG21	O	LCD segment signal output pins.
46 ~ 49 1 ~ 4	SEG22 ~ SEG29	O	LCD segment signal output pins. SEG29~SEG22 share pads with P1 [7:0] Open Drain Output pin.
5 ~ 8	COM0 ~ COM3	O	LCD common signal output pins.
9 ~ 12	P0.0 ~ P0.3	I/O	Programmable I/O ports with interrupt and wake up function.

Note: In the “Type” field,
“I” means input only.
“O” means output only.
“B” means bi-direction.
“P” means Power, “G” means Ground.

4 Block Diagram

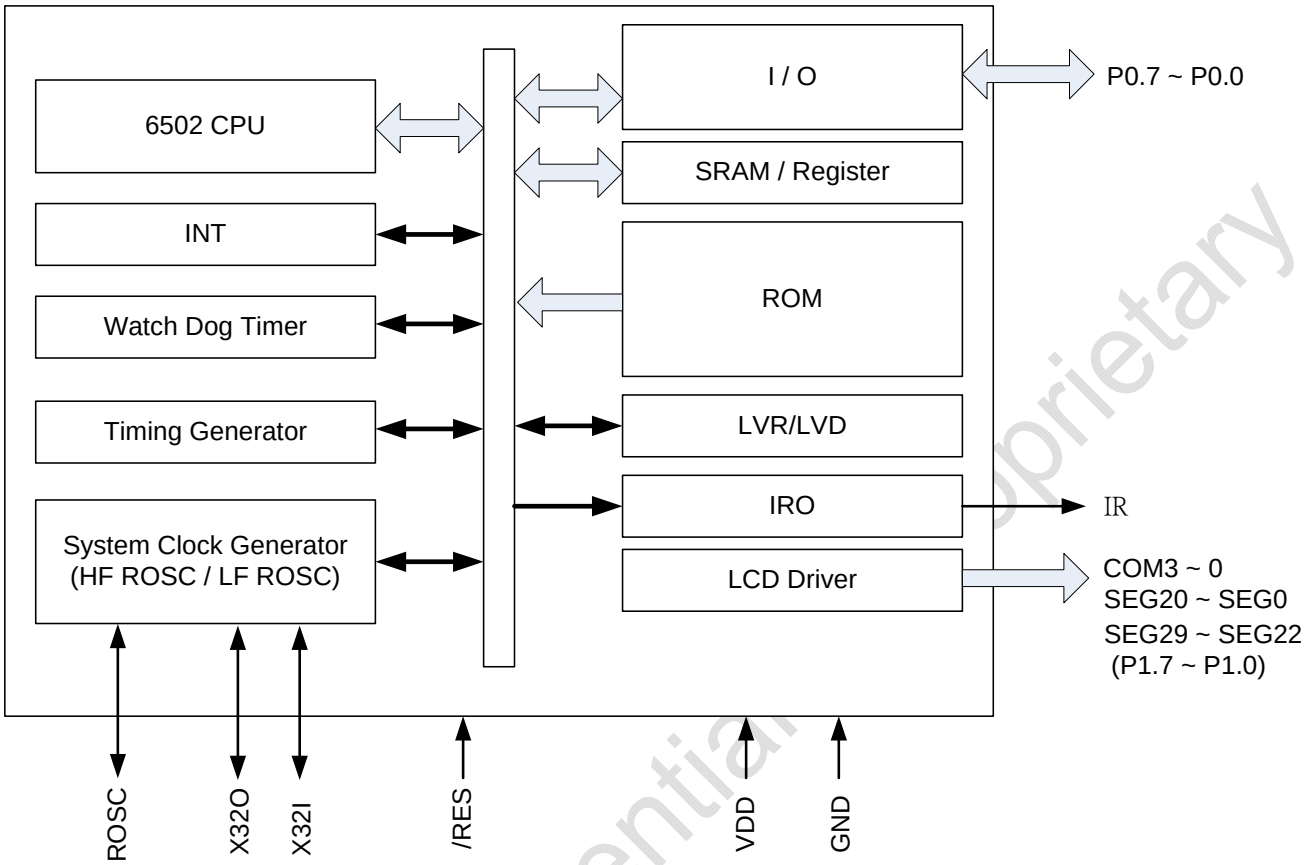


Figure 4-1 Block Diagram

5 Function Description

5.1 Registers

	A
	Y
	X
	P
PCH	PCL
1	S

5.2 Accumulator

The accumulator is a general-purpose 8-bit register, which stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of two data words used in these operations.

5.3 Index Register(X,Y)

There are two 8-bit index registers (X and Y), which may be used to count program steps or to provide an index value to be used in generating an effective address. When executing an instruction, which specifies indexed addressing, the CPU fetches the OP Code and the base address, and modifies the address by adding the index register to it prior to performing the desired operation. Pre- or post-index of index address is possible.

5.4 Processor Status Register

The 8-bit processor status register contains seven status flags. Some of the flags are controlled by the program, others may be controlled both the program and the CPU.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N	V	1	B	D	I	Z	C

N: Signed flag, 1 = negative, 0 = positive
V: Overflow flag, 1 = true, 0 = false
B: BRK interrupt command, 1 = BRK, 0 = IRQB
D: Decimal mode, 1 = true, 0 = false
I: IRQB disable flag, 1 = disable, 0 = enable
Z: Zero flag, 1 = true, 0 = false
C: Carry flag, 1 = true, 0 = false

5.5 Program Counter(PC)

The 16-bit program counter register provides the addresses, which step the micro-controller through sequential program instructions. Each time the micro-controller fetch an instruction from program memory, the lower byte of the program counter (PCL) is placed on the low-order 8 bits of the address bus and the higher byte of the program counter (PCH) is placed on the high-order 8 bits. The counter is incremented each time an instruction or data is fetched from program memory.

5.6 Stack Point(S)

The stack pointer is an 8-bit register, which is used to control the addressing of the variable-length stack. The stack pointer is automatically incremented and decremented under control of the micro-controller to perform stack manipulations under direction of either the program or interrupts (/NMI or /IRQ). The stack allows simple implementation of nested subroutines and multiple level interrupts. The stack pointer is initialized by the user's firmware.

6 Memory Organization

There are 128 bytes SRAM, located in address 0000H to 007FH, in the MG65L566A . They could be used as either working RAM or stacks according to application programs. For the purpose above, the location 0000H to 007FH and 0100H to 017FH are overlaps. In other words, accessing any locations inside the range 0000H to 007FH is equivalent to access the corresponding ones in the range 0100 to 017FH. All special function registers, SFRs, are located at the region 00C0H to 00FFH. Such an arrangement could benefit from the faster access time of zero-page.

For LCD function, there are 16 bytes LCD RAM (1000H to 100FH) in MG65L566A . They can also be used as a general purpose RAM when LCD function is unused. There are 64K bytes program/data ROM in MG65L566A . It is combined with 32K program/data ROM and bank switching data ROM. The ROM address from 8000H to FFFFH can store program and other data. There are two banks in MG65L566A that is index by SFR. The default bank number is 00H after power on or reset. The bank select function, ranged from 4000H to 7FFFH (16Kbyte/bank), is used for extending memories if the ROM size is more than 32K bytes in MG65L566A . The address mapping of MG65L566A is shown as below.

MG65L566A Memory Map

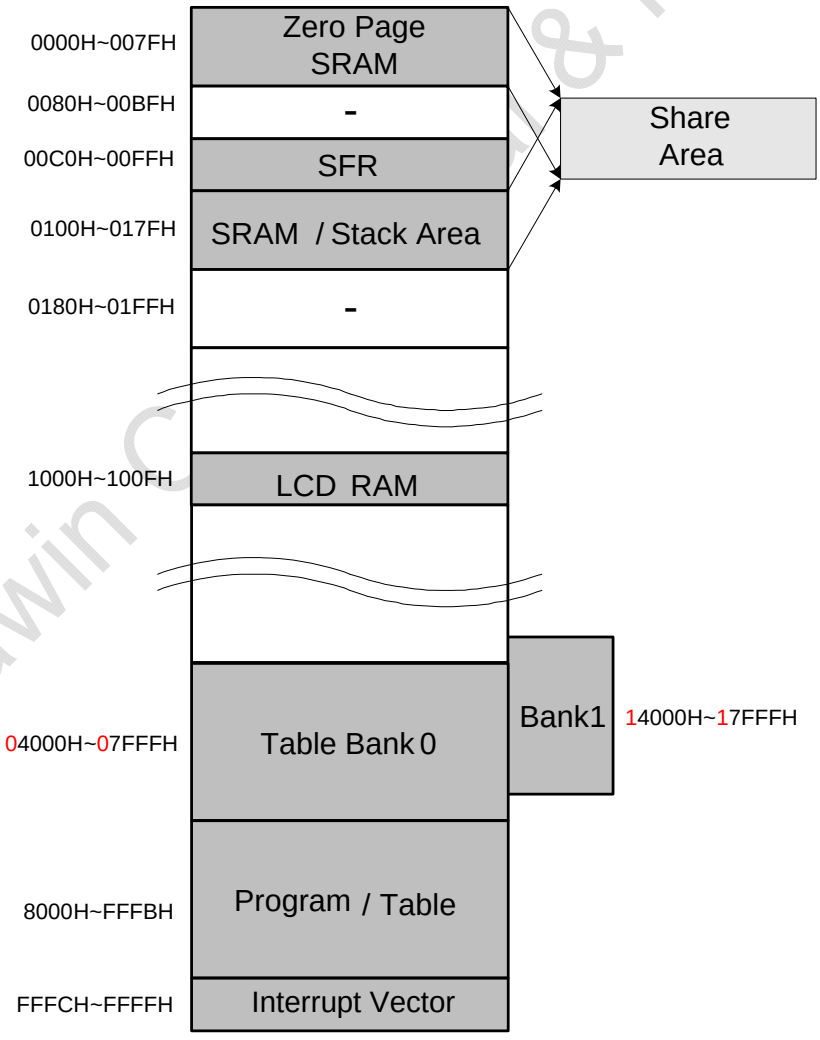


Figure 6-1 Memory Map

6.1 SFR Mapping

The address 00C0H to 00FFH is reserved for special function registers (SFR). The SFR is used to control or store the status of I/O, timers, system clock and other peripheral.

Table 6-1 SFR Table

SFR (special function register): 00C0H~00FFH

Address	Content	Default	Address	Content	Default
00C0		--------	00D0		--------
00C1		--------	00D1		--------
00C2	IRQ_EN / IRQ_ST	--0000-- /000000--	00D2	P0	00000000
00C3	IRQ_CLR	XXXXXX--	00D3	P0dir	00000000
00C4		--------	00D4	P0plh	11111111
00C5	RESOK	XXXX---0	00D5	P0opd	00000000
00C6		--------	00D6	P1	11111111
00C7		--------	00D7	SEG_SEL	-1010000
00C8	TM0	11111111	00D8		--------
00C9		--------	00D9		--------
00CA	TM0_CTL	00---000	00DA	IRO	1------0
00CB		--------	00DB		--------
00CC	DIV_SEL	------00	00DC		--------
00CD	TM1	11111111	00DD		--------
00CE		--------	00DE	LCD_CR	0-----00
00CF	TM1_CTL	00---000	00DF		--------

Address	Content	Default	Address	Content	Default
00E0	BANK	-------0	00F0	SCK_SEL	0----000
00E1		--------	00F1		--------
00E2		--------	00F2		--------
00E3		--------	00F3		--------
00E4		--------	00F4		--------
00E5		--------	00F5		--------
00E6		--------	00F6		--------
00E7		--------	00F7		--------
00E8		--------	00F8		--------
00E9		--------	00F9	CWPR	XXXXXXXX
00EA		--------	00FA		--------
00EB		--------	00FB		--------
00EC		--------	00FC	PWR_CR	-----000
00ED		--------	00FD		--------
00EE		--------	00FE		--------
00EF		--------	00FF		--------

6.2 Write Protect Function Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00F9H	CWPR	PT7	PT6	PT5	PT4	PT3	PT2	PT1	PT0	-	√

Condition Write Protect flag register (CWPR) is used to protect BANK, IRQ_CLR.7 (WDT), PWR_CR and SCK_SEL. If want to change BANK, IRQ_CLR.7 (WDT), PWR_CR and SCK_SEL, it must write "78H" to CWPR first.

PT7~PT0: Write Protect Pattern. In MG65L566A write protect pattern is "78H"

Note:

1. *When CWPR is written by firmware, it would be automatically cleared by hardware after the "next write action" of firmware.*

※ Bit-manipulation instructions are not available on this register.

7 Interrupt

There are four kinds interrupt source is provided in MG65L566A . The flag IRQ_EN and IRQ_ST are used to control the interrupts. When flag IRQ_ST is set to '1' by hardware and the corresponding bits of flag IRQ_EN has been set by software, an interrupt is generated. When an interrupt occurs, all of the interrupts are inhibited until the CLI or STA IRQ_EN, # I instruction is invoked. Executing the SEI instruction can also disable the interrupts.

Table 7-1 Interrupt Vector Table

Vector Address	Item	Flag	Properties	Memo
FFFEH, FFFFH	P0 IRQ	IRQ_ST.2	Ext.	P0.0 ~ P0.7 interrupt vector
	TM0 IRQ	IRQ_ST.3	Int.	TM0 underflow interrupt
	TM1 IRQ	IRQ_ST.4	Int.	TM1 underflow interrupt
	DIV IRQ	IRQ_ST.5	Int.	Divider carry out interrupt
FFFCH, FFFDH	RESET	None	Ext.	Initial reset
	WDT	IRQ_ST.7	Int.	Watch dog timer reset
	LVR	None	Int.	Low voltage reset

7.1 Interrupt Register

IRQ enable flag

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C2H	IRQ_EN	-	-	DIVx	TM1	TM0	P0	-	-	-	√

Program can enable or disable the ability of triggering IRQ through this register.
0: Disable (default "0" at initialization)
1: Enable
P0: Falling edge occurs at port 0 input mode.
TM0: Timer 0 underflow.
TM1: Timer 1 underflow.
DIVx: Divider selected interrupt frequency occurred.

※ Bit-manipulation instructions not available on this register.

IRQ status flag

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C2H	IRQ_ST	WDT	LVD	DIVx	TM1	TM0	P0	-	-	√	-

When IRQ occurs, program can read this register to know which source triggering IRQ. If the interrupt triggering is enabled and the interrupt event is accepted, the correspond IRQ status flag should be cleared by program after the interrupt vector is loaded into program counter.

LVD: Low voltage detected. 1:VDD is under 2.3V. 0:VDD is above 2.3V. It is set by hardware and read only.

※ Bit-manipulation instructions not available on this register.

IRQ clear flag

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C3H	IRQ_CLR	WDT	LVD	DIVx	TM1	TM0	P0	-	-	-	√

Program can clear the interrupt event by writing '1' into the corresponding bit.
The IRQ_CLR.7 (WDT) is protected by CWPR.

※ Bit-manipulation instructions not available on this register.

7.2 Interrupt System

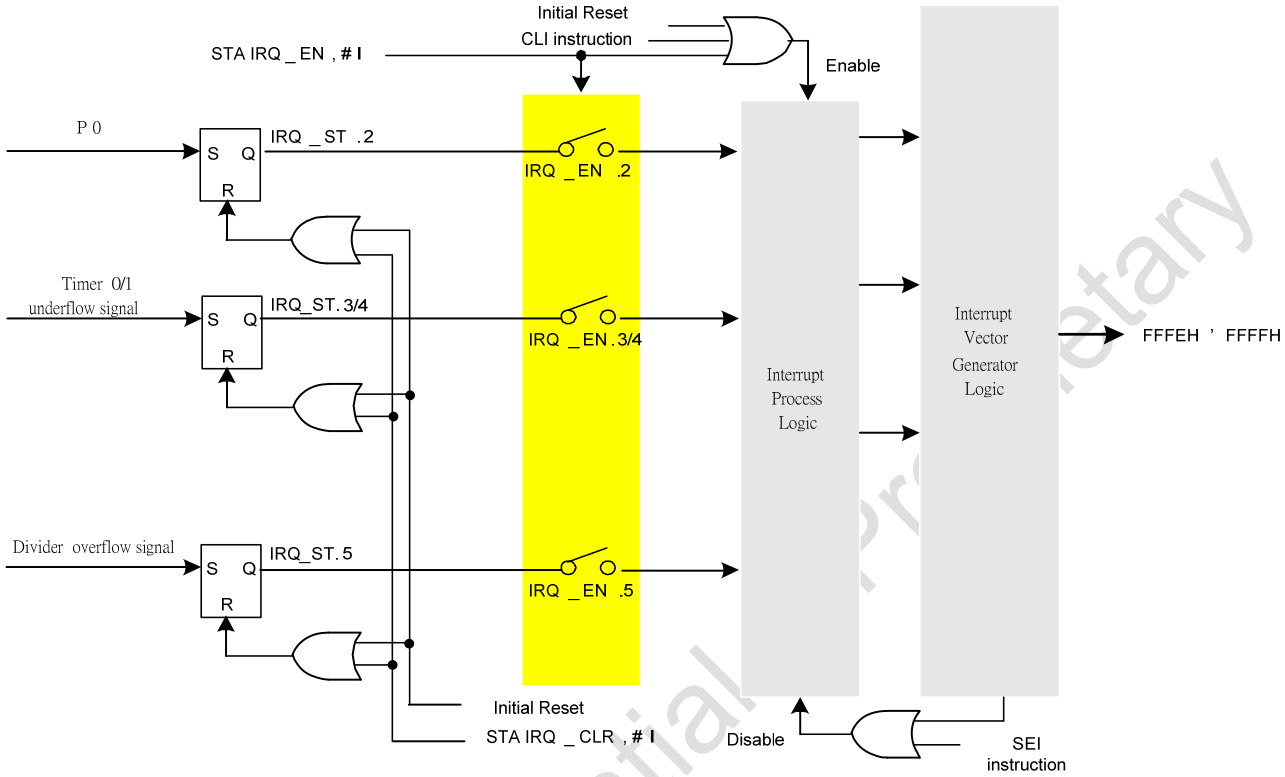


Figure 7-1 Interrupt System Diagram

8 Reset

8.1 Low Voltage Reset (LVR)

The MG65P515 provides low voltage reset circuit in order to monitor the supply voltage of the device. If the supply voltage of the device is within the range 0.9V ~ VLVR, such as changing a battery, the LVR will automatically reset the device internally.

The LVR includes the following specifications

1. The low voltage (0.9V~VLVR) has to remain in their original state to exceed 1ms. If the low voltage state does not exceed 1ms, the LVR will ignore it and do not perform a reset function.
2. In the LVR mode, the clock source (INT./EXT. OSC) continuous oscillating and the IO status becomes default value.

8.2 Watchdog Timer (WDT)

(The example is base on 4MHz and SCK_SEL.1 = 0)

Name								Bit 8	R	W
WDT								1.9 (Hz)	-	-

The watchdog timer time-out period is obtained by the equation: (F_{DIV} /512)/512 or (F_{DIV} /4096)/512 select by SCK_SEL.1 (CKS1).
Before watchdog timer time-out occurs, the program must clear the 9-bit WDT timer by writing 1 to IRQ_CLR.7.
WDT overflow will cause system reset and set IRQ_CLR.7 to high.

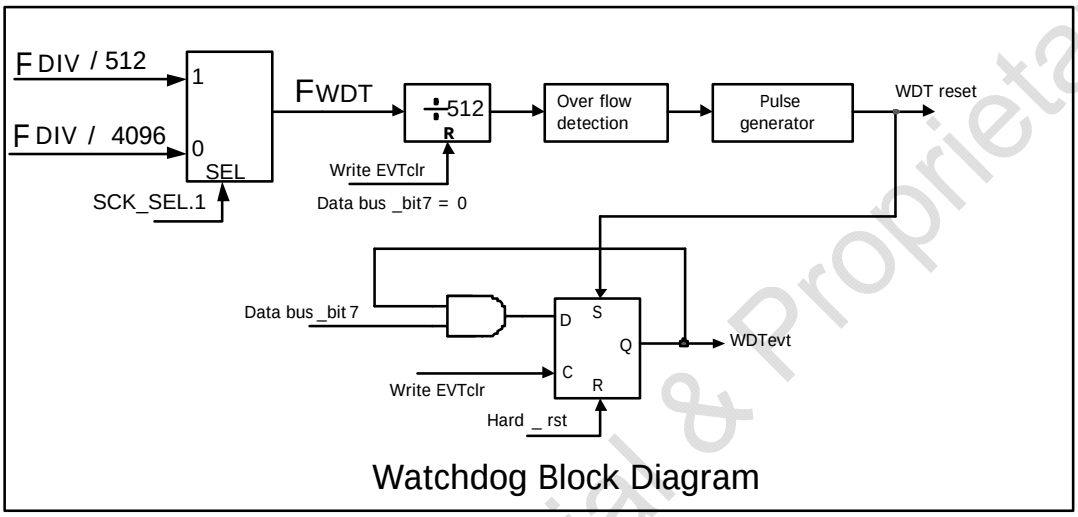


Figure 8-1 Watch Dog Diagram

8.3 Reset OK

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C5H	RESOK	RK7	RK6	RK5	RK4	-	-	-	RSEL	-	√

RESOK (Reset OK): If the device reset OK and work well, **must** write #$90 into this register.
For example:

```
Program_start:   LDA   #10010000b
                 STA   $C5
```

RSEL: Reset selector.
0: IO status reset by All Reset WDT, LVR, POR, BOR and EXT_RESET (Default)
1: IO status reset by LVR, BOR, EXT_RESET and POR
※ Bit-manipulation instructions not available on this register.

9 Power Control

9.1 Power Control Register

System clock selector (※The Clock Control Register is protected by CWPR.)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00F0H	SCK_SEL	CKS7	-	-	-	-	CKS2	CKS1	CKS0	-	√

CKS0: F_{CPU} clock source select. 0: F_{OSC}, 1: F_{X32}
CKS1: Watchdog clock source select. 0: F_{DIV}/4096, 1: F_{DIV}/512
CKS2: De-bounce (awakened from stop mode) time selector. 0: F_{OSC}/16384, 1: F_{OSC}/4096
CKS7: Select the input clock source of divider. 0: F_{OSC}, 1: F_{X32}

Power saving control

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00FCH	PWR_CR	-	-	-	-	-	CKC1	CKC0	HALT	-	√

※ PWR_CR is protected by CWPR.
※ Bit-manipulation instructions not available on this register.

CKC1	CKC0	System clock control
0	0	F_{OSC} enable, F_{X32} enable (Dual mode)
0	1	F_{OSC} enable, F_{X32} disable (Single mode)
1	0	F_{OSC} disable, F_{X32} enable (Slow mode)
1	1	F_{OSC} disable, F_{X32} disable (Stop mode)

HALT: F_{CPU} off-line control bit. 1: F_{CPU} off-line, 0: F_{CPU} on-line

Program can switch the normal operation mode to the power-saving mode for saving power consumption through this register. There are three power saving modes in this system.

Slow mode: *(PWR_CR.CKC1 = 1, PWR_CR.CKC0 = 0)*
The main uC clock (F_{OSC}) stops oscillating. Only very low power is needed for uC to keep running.

Stop mode: *(PWR_CR.CKC1 = 1, PWR_CR.CKC0 = 1)*
Both system clocks stop oscillating. The uC can be awakened from stop mode by 3-ways: port 0 interrupt (IRQ_EN.2=1 and IRQ_ST.2=1), hardware reset, or power-on reset. When the stop mode is released, only the oscillator, which is providing the uC clock, will be enabled again.
If uC clock source is F_{X32} and system into STOP mode (set PWR_CR [2:1] = 11). The F_{X32} will be enabled and F_{OSC} still keep same status, when uC waken up by port0.

Halt mode: *(PWR_CR.HALT = 1)*
The F_{CPU} clock in off-line status. The oscillator(s) still keep same status. The uC can be awakened from halt mode by 4-ways: the interrupt events, hardware reset, LVR, or power-on reset.

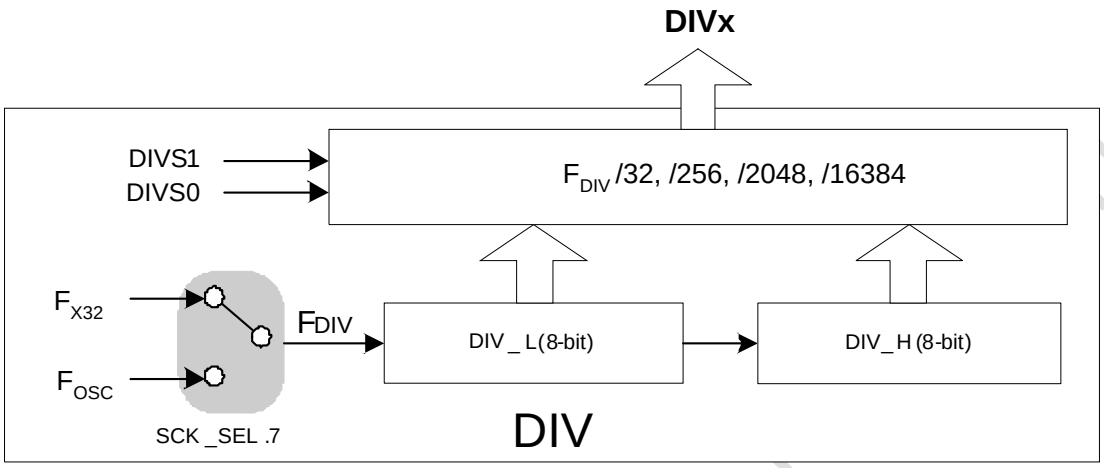
10 Divider

10.1 Divider

DIV interrupt selector

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00CCH	DIV_SEL	-	-	-	-	-	-	DIVS1	DIVS0	-	√

The divider clock source comes from F_{X32} (sub-main clock) or F_{OSC} (main clock).
Program can select divider interrupt frequency by DIV_SEL register.



DIVS1	DIVS0	DIV interrupt occurs status
0	0	F_{DIV} / 16384
0	1	F_{DIV} / 2048
1	0	F_{DIV} / 256
1	1	F_{DIV} / 32

※ Bit-manipulation instructions not available on this register.

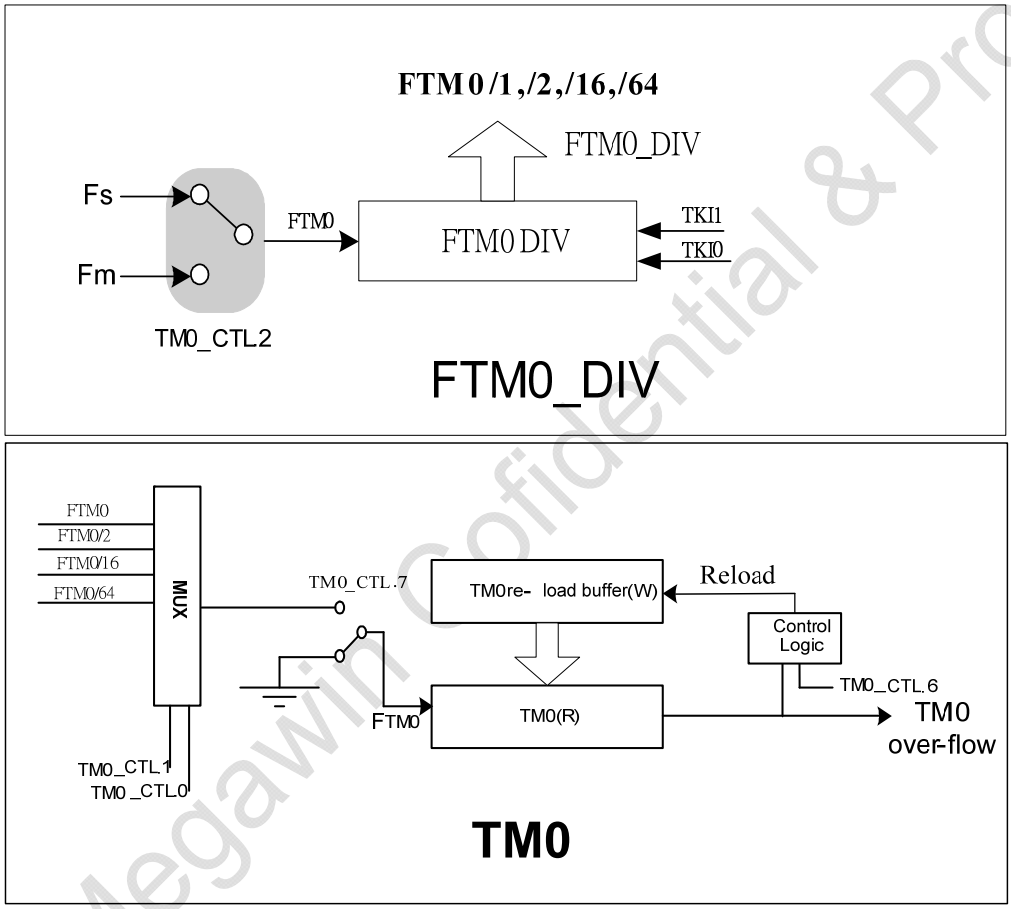
11 Timer

11.1 Timer0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C8H	TM0	T7	T6	T5	T4	T3	T2	T1	T0	√	√
00CAH	TM0_CTL	STC	RL/S	-	-	-	TCS0	TKI1	TKI0		√

Timer 0 is an 8-bit down-count counter.
STC: Start/Stop counting. 1: start and pre-load the value to counter, 0: stop timer clock
RL/S: Auto-reload disable/enable. 1: disable auto-reload, 0: enable auto-reload
TCS0: select the input clock source of timer0. 0:F_{OSC}, 1: F_{X32}

TKI1	TKI0	Selected TM0 input frequency (F_{TM0_DIV})
0	0	F_{TM0} / 1
0	1	F_{TM0} / 2
1	0	F_{TM0} / 16
1	1	F_{TM0} / 64



F_{TM0_UV}, can be calculated with the equation:
$F_{TM0\_UV} = F_{TM0} / (TM0+1)$, where the F_{TM0} is the timer input frequency set by TKI1 and TKI0.

For example: (if F_{TM0} = 2.000MHz, TKI1=TKI0=0)

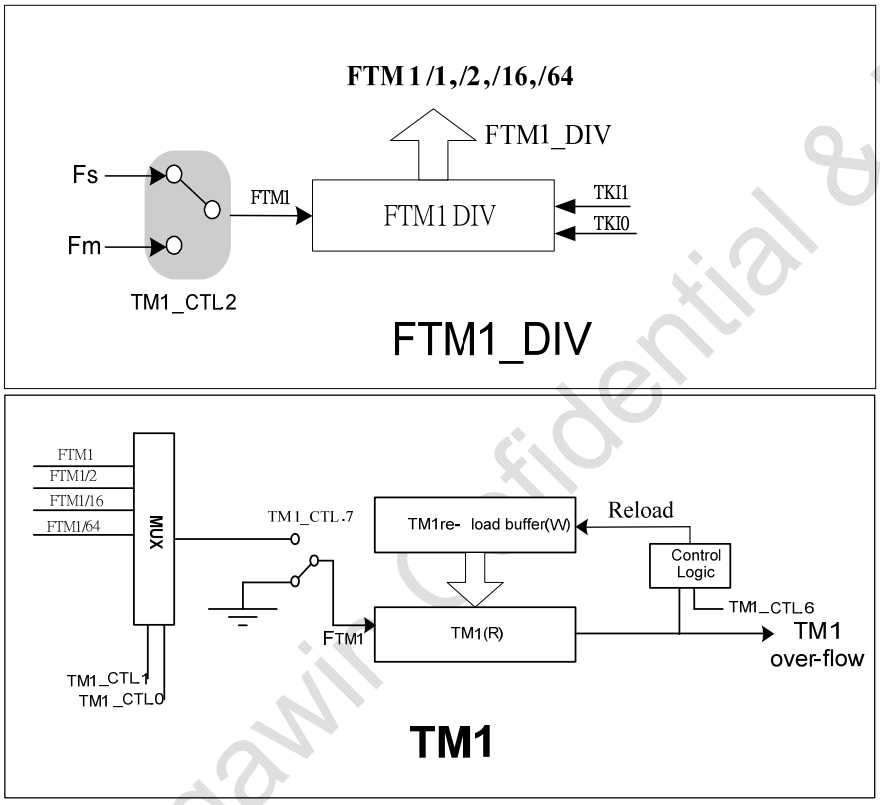
TM0	Frequency
00H	Reserved
01H	1.000MHz
02H	667kHz
…	…
FFH	7.84kHz

11.2 Timer1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00CDH	TM1	T7	T6	T5	T4	T3	T2	T1	T0	√	√
00CFH	TM1_CTL	STC	RL/S	-	-	-	TCS1	TKI1	TKI0		√

Timer 1 is an 8-bit down-count counter.
STC: Start/Stop counting. 1: start and pre-load the value to counter, 0: stop timer clock
RL/S: Auto-reload disable/enable. 1: disable auto-reload, 0: enable auto-reload
TCS1: select the input clock source of timer1. 0: F_{OSC}, 1: F_{X32}

TKI1	TKI0	Selected TM1 input frequency (F_{TM1_DIV})
0	0	F_{TM1} / 1
0	1	F_{TM1} / 2
1	0	F_{TM1} / 16
1	1	F_{TM1} / 64



F_{TM1_UV}, can be calculated with the equation:
$F_{TM1\_UV} = F_{TM1}$ / (TM1+1), where the F_{TM1} is the timer input frequency set by TKI1 and TKI0.

For example: (if F_{TM1} = 2.000MHz,TKI1=TKI0=0)

TM1	Frequency
00H	Reserved
01H	1.000MHz
02H	667kHz
…	…
FFH	7.84kHz

12 Configurable I/O Ports

12.1 Port 0

Port 0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D2H	P0	P07	P06	P05	P04	P03	P02	P01	P00	√	√

Port 0 is an 8-bit I/O port; each pin can be programmed as input or output individually. When P0.n is configured as an output pin, the P0.n pin would output the logic content of P0obuf.n.
When the P0.n is configured as output mode, reading P0pad.n would always read logic '0'.
When the P0.n is configured as input mode, reading P0pad.n would always read the logic value from pad.

※ Bit-manipulation instructions not available on this register.

Port 0 Direction Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D3H	P0dir	DR7	DR6	DR5	DR4	DR3	DR2	DR1	DR0	-	√

P0dir (Port 0 Direction)

DR.n = 0: P0.n is configured as an input pin. (Default)
1: P0.n is configured as an output pin.

※ Bit-manipulation instructions are not available on this register.

Port 0 Pull-high Control Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D4H	P0plh	PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0	-	√

0: Disable internal pull-high.
1: Enable internal pull-high. (Default)
PHn: Control bit is used to enable the pull-high of P0.n pin.

※ Bit-manipulation instructions not available on this register.

Port 0 Open-Drain Control Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D5H	P0opd	OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0	-	√

0: Disable open-drain output (CMOS output). (Default)
1: Enable open-drain output.
OD.n: Control bit is used to enable the open-drain of P0.n pin.

※ Bit-manipulation instructions not available on this register.

12.2 Port 1

Port 1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D6H	P1	P17	P16	P15	P14	P13	P12	P11	P10	-	√

Port 1 is an 8-bit open drain type output port without pull high resistor; When SEG_SEL register option is selected to LCD segment output. The P1.0 to P1.7 pins can be set as SEG22 to SEG29.

※ Bit-manipulation instructions not available on this register.

Segment/Open Drain Select

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D7H	SEG_SEL	-	OSCR2	OSCR1	OSCR0	SSEL3	SSEL2	SSEL1	SSEL0	-	√

SEG_SEL is the P1 or LCD segment output selector. The default value is open drain output without pull-high resistors.
SEG29~28: LCD Segment29~Segment28 (SSEL3=1): P1.7~P1.6 (SSEL3 = 0) Default: SSEL3=0
SEG27~26: LCD Segment27~Segment26 (SSEL2=1): P1.5~P1.4 (SSEL2 = 0) Default: SSEL2=0
SEG25~24: LCD Segment25~Segment24 (SSEL1=1): P1.3~P1.2 (SSEL1 = 0) Default: SSEL1=0
SEG23~22: LCD Segment23~Segment22 (SSEL0=1): P1.1~P1.0 (SSEL0 = 0) Default: SSEL0=0

OSCR [2:0]: It used to select RC oscillator resistor value.
Set Different OSCR value to change system clock “Fm” frequency.
(default : 101 <about 4MHz>)

※ Bit-manipulation instructions not available on this register.

12.3 IRO

IRO Buffer

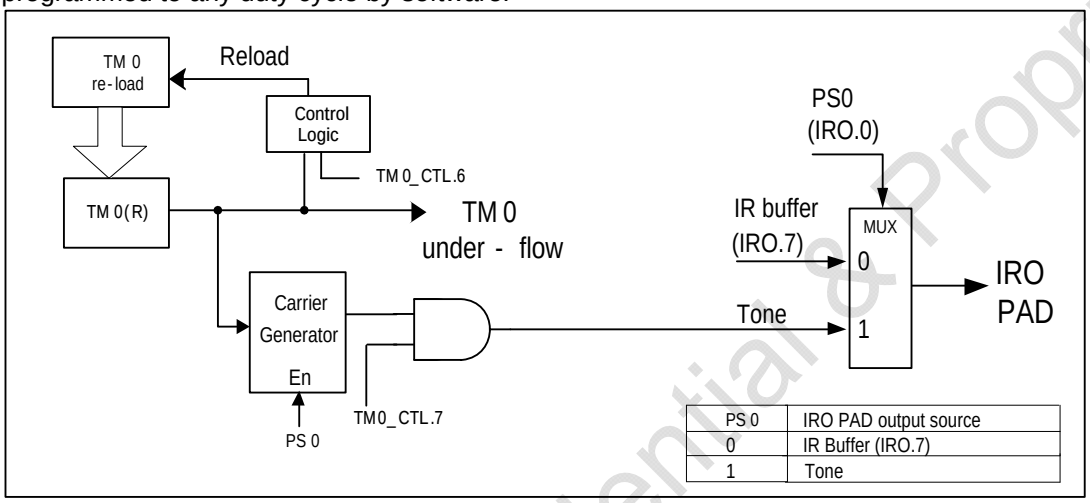
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00DAH	IRO	IR	-	-	-	-	-	-	PS0	-	√

IRO pad is a high sink current output pin. The IRO output pin would output the logic content from IR buffer or Tone (select by PS0).

PS0 = 0: IRO is configured as IR buffer. (Default)
1: IRO is configured as Tone output.

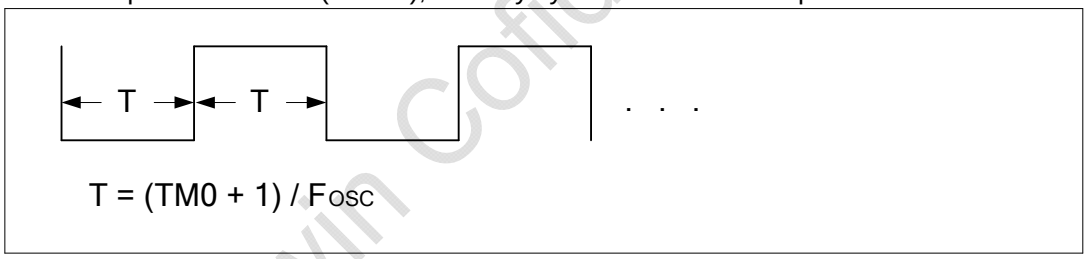
※ Bit-manipulation instructions are not available on this register.

PS0 (IRO.0) can set the IRO pad output source as IR buffer or tone generator. The IRO output waveform can be programmed to any duty cycle by software.



PS 0	IRO PAD output source
0	IR Buffer (IRO.7)
1	Tone

If the tone path is selected (PS0=1), the duty cycle of the carrier output is fixed to 50%.



The counter underflow frequency of timer0 can be calculated with the equation:
$F_{TM0\_UV} = F_{TM0} / (TM0reg+1)$. The F_{TM0} is Timer0 clock input.
For example: F_{TM0} = 455KHz,TM0reg = 0BH
$F_{TM0\_UV} = F_{TM0} / (TM0reg+1) = 455K/(0BH+1) = 37.92KHz$.

13 LCD Controller/Driver

The MG65L566A can directly drive an LCD with 30 segment output pins and 4 common output pins for a total of 30 × 4 dots. LCD control register can be used to select LCD display configuration. LCD driving mode is 1/3 bias and 1/4 duty and frame frequency is about 81.38Hz. When CPU access the LCD RAM area, the access path of the LCD RAM will be transferred from LCD driver to CPU automatically.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00DEH	LCD_CR	LCDON	-	-	-	-	-	CKS1	CKS0	-	√

LCDON: LCD on/off control bit. 0: off (default), 1:on
LCD scan rate, F_{COM}, is derived from the clock source of divider. The relation between the CKS1, CKS0, F_{COM} and F_{DIV} is shown as below.

CKS1	CKS0	Selected F_{COM} frequency
0	0	F_{DIV} / 96
0	1	F_{DIV} / 6144
1	0	F_{DIV} / 12288
1	1	F_{DIV} / 24576

The LCD frame rate can be calculated with the equation:

$F_{FRAME} = F_{COM}$ / COM No.

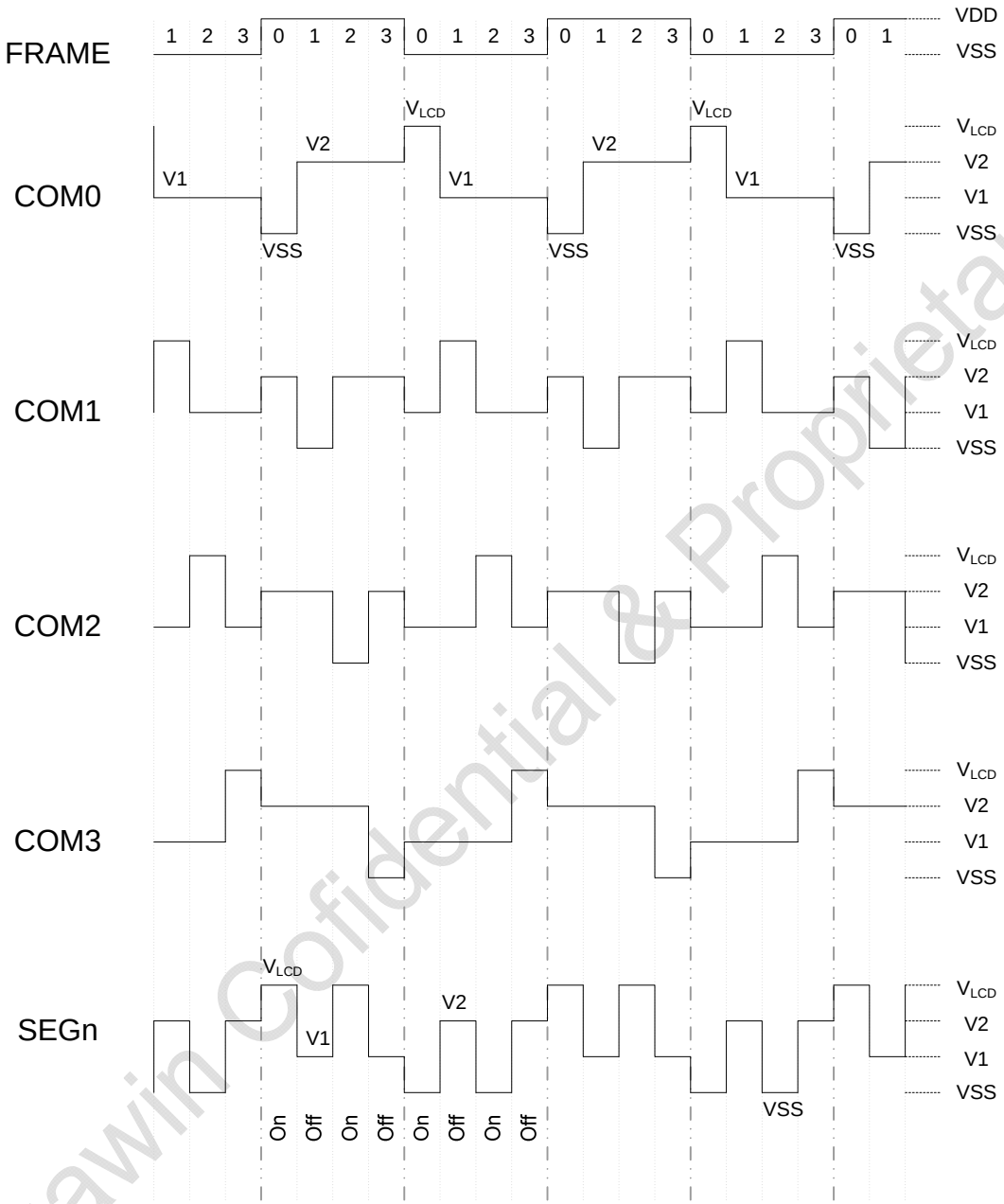
Typical selection combination for 1/4 duty are shown below:

COM No.	F_{DIV_IN}	Selected F_{COM} frequency	F_{FRAME}
4	6M	F_{DIV} / 24576	61.04
4	4M	F_{DIV} / 12288	81.38
4	2M	F_{DIV} / 6144	81.38
4	32K	F_{DIV} / 96	85.33

There are 16 LCD data RAM in MG65L566A. When the bit value of LCD data RAM is “1”, the LCD is turned on. When the bit value of LCD data RAM is “0”, the LCD is turned off. The contents of the LCD data RAM are sent out through the SEG0 to SEG29 pins by a direct memory access. The relationship between the LCD data RAM and SEG/COM pins is shown below.

LCD Data RAM	COM_X	Bit 7 SEG	Bit 6 SEG	Bit 5 SEG	Bit 4 SEG	Bit 3 SEG	Bit 2 SEG	Bit 1 SEG	Bit 0 SEG
1000H	COM 0	07	06	05	04	03	02	01	00
1001H		15	14	13	12	11	10	09	08
1002H		23	22	21	20	19	18	17	16
1003H		RAM	RAM	29	28	27	26	25	24
1004H	COM 1	07	06	05	04	03	02	01	00
1005H		15	14	13	12	11	10	09	08
1006H		23	22	21	20	19	18	17	16
1007H		RAM	RAM	29	28	27	26	25	24
1008H	COM 2	07	06	05	04	03	02	01	00
1009H		15	14	13	12	11	10	09	08
100AH		23	22	21	20	19	18	17	16
100BH		RAM	RAM	29	28	27	26	25	24
100CH	COM 3	07	06	05	04	03	02	01	00
100DH		15	14	13	12	11	10	09	08
100EH		23	22	21	20	19	18	17	16
100FH		RAM	RAM	29	28	27	26	25	24

1/4 duty 1/3 bias



14 Option Register

Mask Option

Item	1	0
WDT	Enable (default)	Disable
Fm (F_{CPU} = F_{OSC}/2)	Disable (default)	Enable

15 Programming Notice

The status after different reset condition is listed below:

Item	Power on reset	CPU /RES pin reset
SRAM Data	Unknown	Unchanged
CPU Register	Unknown	Unknown
Special Function Register	Default value	Default value

16 Application Circuit

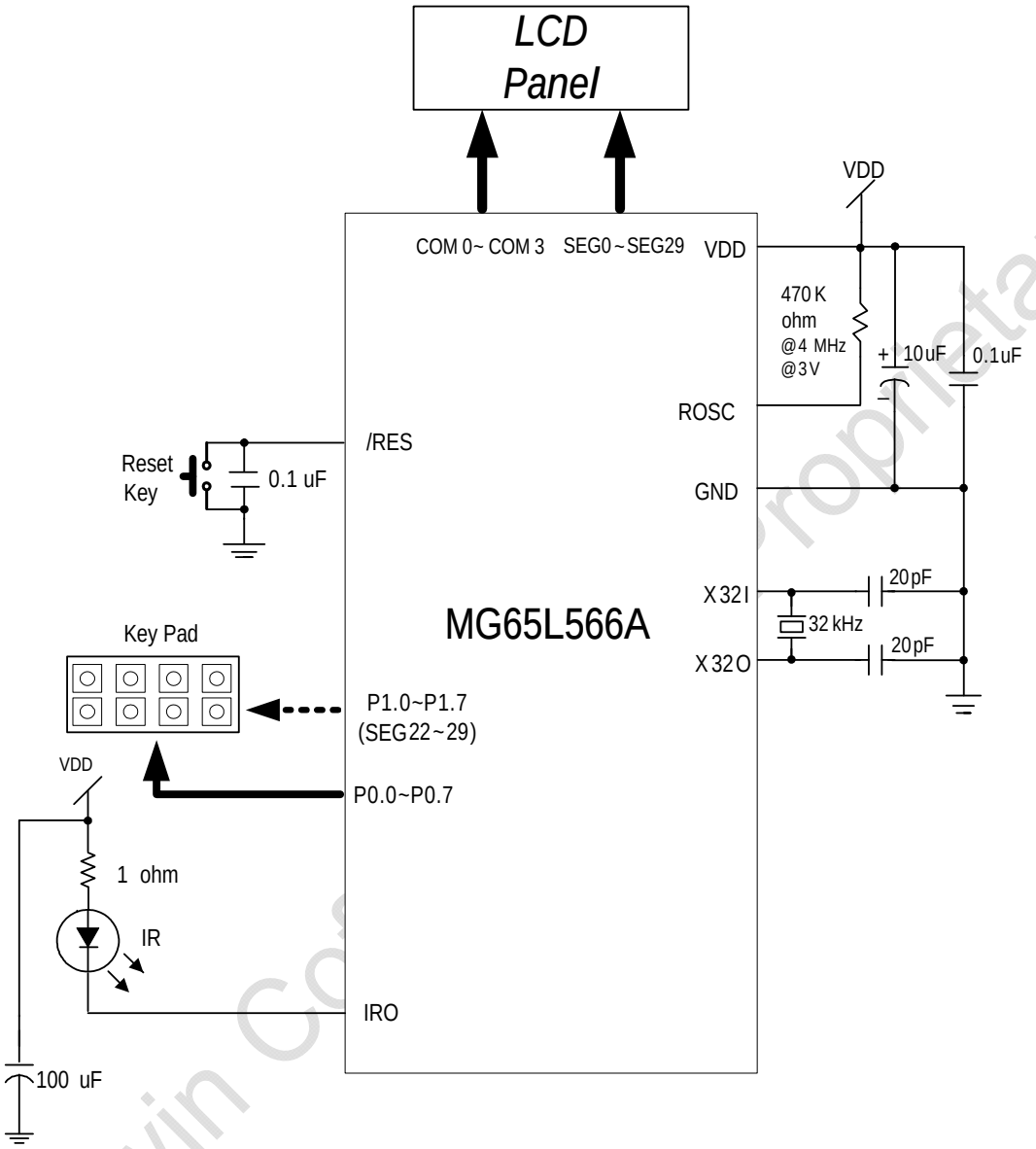


Figure 166-1 Application Circuit - LCD Remote Controller

17 Electrical Characteristics

17.1 Absolute Maximum Rating

PARAMETER	RATING	UNIT
Supply Voltage to Ground Potential	-0.3 to +5.0	V
Applied Input / Output Voltage	-0.3 to +5.0	V
Power Dissipation	60	mW
Ambient Operating Temperature	0 to +70	°C
Storage Temperature	-55 to +150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

17.2 DC Characteristics

(VDD-VSS = 3.0 V, FOSC = 4MHz, Ta = 25° C; unless otherwise specified)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input High Voltage	V_{IH}	-	0.7 V_{DD}	-	V_{DD}	V
Input Low Voltage	V_{IL}	-	0	-	0.3 V_{DD}	V
Op. Current 1	I_{OP}	Dual mode, No load, LCD on Fcpu=4Mhz		1.8	5.6	mA
Halt Current 2	I_{STB2}	Slow mode, HALT, No load, LCD on , Fcpu=32768Hz ,DIVx INT on		15	20	μA
Halt Current 3	I_{STB3}	Slow mode, No load, LCD off , Fcpu=32768Hz ,DIVx INT off		10		μA
Stop Current	I_{STB1}	STOP mode, No load,LCD off	-		1	μA
Port 0 drive current	I_{OH1}	V_{OH} = 2.7V, V_{DD} = 3.0V	2	4	-	mA
Port 0 sink current	I_{OL1}	V_{OL} = 0.4V, V_{DD} = 3.0V	8	10	-	mA
COM,SEG drive current	I_{OH2}	V_{OH} = 2.7V, V_{LCD} = 3.0V	0.1	2	-	mA
COM,SEG sink current	I_{OL2}	V_{OL} = 0.4V, V_{LCD} = 3.0V	0.3	3	-	mA
SEG24~SEG31(P10~P17) sink current	I_{OL3}	V_{OL} = 0.4V, V_{DD} = 3.0V	8	10	-	mA
P0 Internal Pull-high Resistor	R_{PH1}	V_{IL} = 0V	75K	100K	125K	Ω
IRO Drive Current	IOH4	VOH = 2.7V, VDD = 3.0V	10	-	-	mA
IRO Sink Current	IOL4	VOL = 0.4V, VDD = 3.0V	100.0	-	-	mA
		VOL = 1.0V, VDD = 3.0V	250.0			mA
/RES Pull-high Resistor	RRES	VIL = 0V	-	30K	-	Ω
Low Voltage Detector for uC	V_{LVD1}	VDD > 2.3V		2.3		V
Low Voltage Reset	V_{LVR}	-		1.8v		V
RC oscillator frequency	F_{ROSC}	-	2		6	MHz

17.3 AC Characteristics

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Built-in CPU Op. Frequency	F_{CPU}	RC, V_{DD} = 3.0V	0.5	4	6	MHz
Frequency Deviation by Voltage Drop for RC Oscillator	$\frac{\Delta f}{f}$	$\frac{f(3.6V) - f(2.6)}{f(3.0V)}$	-	3	10	%
POR Duration	T_{POR}	F_{OSC} = 4 MHz	-	0.5	1	mS
System Start-Up Time	T_{SST}	Power-up, reset	-	16384	-	$1/F_{CPU}$
System Wake-Up Time	T_{SWT}	Wake-up from STOP mode	4096	-	16384	$1/F_{CPU}$

18 Revision History

Revision	Page	Descriptions	Date
V0.1		Original	-
V0.2		modify Port 0 drive “VOH”	-
V1.0		Official version	2011/07/21
V2.0		Modify document format.	2011/11/15
V2.1	P.5 P.6	1. Modify PAD assignment. 2. Modify PIN description. 3. Modify MG65L566 To MG65L566A	2011/12/20