Version: 0.04

MG69L220A

Data Sheet

8-Bit Micro-Controller with IO function

Version 0.04

Table of Contents

1 Features

- Single Chip 8-bit CPU
- Memory
  - Program Mask ROM : 8K Bytes
  - Data RAM : 144 Bytes
- Operating voltage: 1.8V to 3.6V
- 42 Programmable GPIO
  - High sink current output
  - Shared input or output pins:
    - Input/output pins P0[7:4]
    - Input pins P0[3:0]
    - Quasi-bi-directional IO pins P1[4:0]
    - Output pins P2[7:0], P3[7:0], P4[7:0], P5[3:0]
- Watchdog timer built-in
- Two re-loadable 8-bit timers
- HALT mode and STOP mode for power saving
- Build-in dual oscillation circuit:
  - RC type main oscillator
  - X32 for sub-oscillator
  - Dual clock operation
- Build-in low voltage detectors (typical voltage: below 2.1V) and low voltage reset (typical voltage: below 1.8V)

1.1 Application Field

General Key Pad Controller.

2 General Description

MG69L220A integrates an 8-bit CPU core, SRAM and system control circuits by a CMOS silicon gate technology. The ROM can store data table and program.

8 I/O 116 dots LCD driver and one large sink output pin make this chip very suitable for AURC, timepiece and sport meter.

3 Pin Configurations

3.1 Pad Assignment

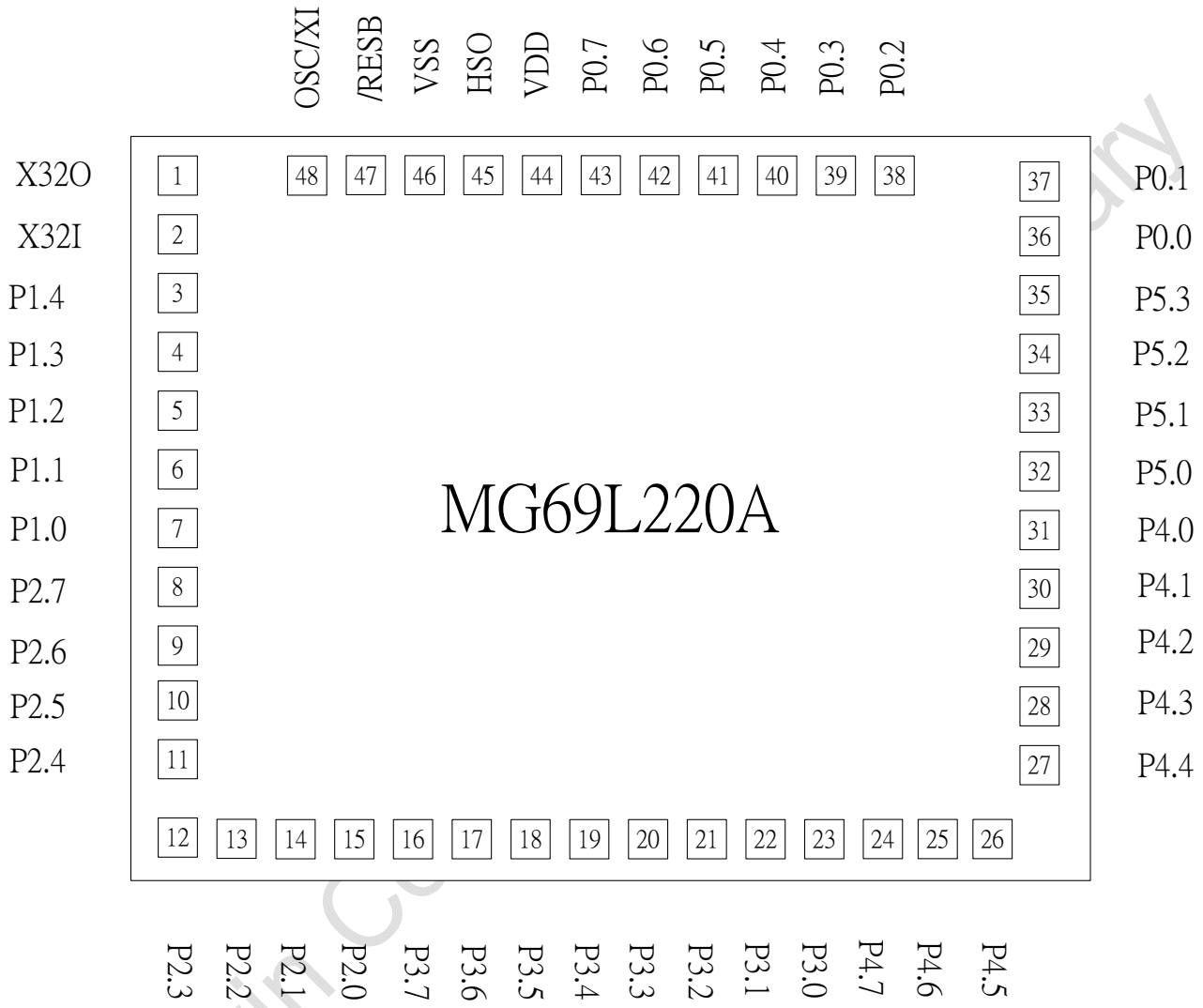


Figure 3-1 Pad Assignment

3.2 Pin Description

Table 3-1 Pin Description

Pad	Name	Type	Description
1,2	X32O, X32I	B	32.768KHz crystal oscillator pins.
3 ~ 7	P1[4:0]	I/0	Quasi-bi-directional IO pin.
8 ~ 15	P2[7:0]	O	Open-drain with pull-high output pin.
16 ~ 23	P3[7:0]	O	Open-drain with pull-high output pin.
24 ~ 31	P4[7:0]	O	Open-drain with pull-high output pin.
32 ~ 35	P5.0 ~ P5.3	O	Open-drain with pull-high output pin.
36 ~ 39	P0.0 ~ P0.3	I	Input pin with interrupt function.
40 ~ 43	P0.4 ~ P0.7	B	Programmable I/O ports with interrupt function.
44	VDD	P	Positive power pins (need to connect together)
45	HSO	O	Direct sink (sink current: 150mA) for high light LED. Default value is high after reset.
46	VSS	P	Ground pins (need to connect together)
47	/RES	I	System reset pin (low active).
48	OSCI	I	RC oscillator input pin.

Note: In the “Type” field,
“I” means input only.
“O” means output only.
“B” means bi-direction.
“P” means Power, “G” means Ground.

4 Block Diagram

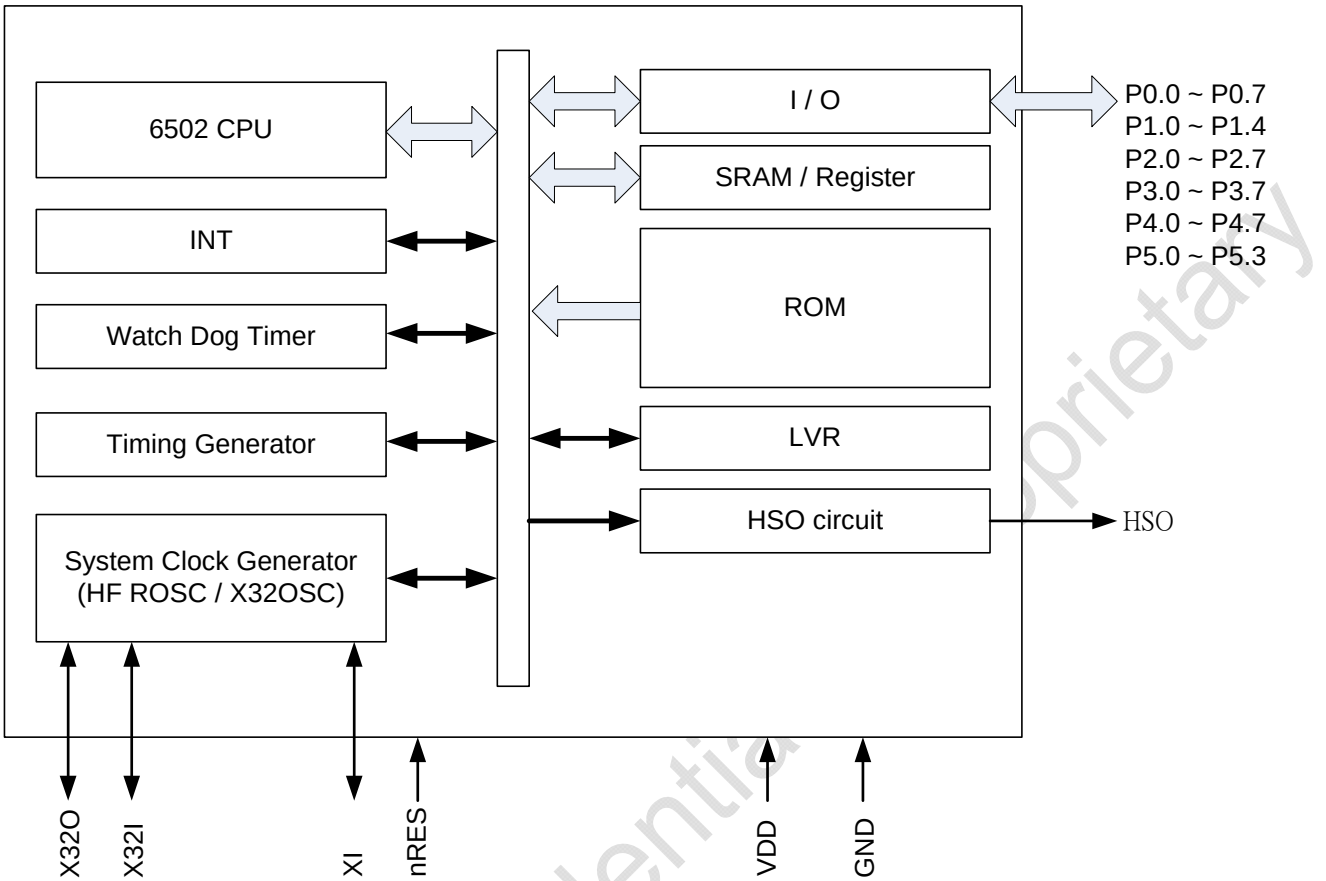


Figure 4-1 Block Diagram

5 Function Description

5.1 Registers

	A
	Y
	X
	P
PCH	PCL
1	S

5.2 Accumulator

The accumulator is a general-purpose 8-bit register, which stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of two data words used in these operations.

5.3 Index Register(X,Y)

There are two 8-bit index registers (X and Y), which may be used to count program steps or to provide an index value to be used in generating an effective address. When executing an instruction, which specifies indexed addressing, the CPU fetches the OP Code and the base address, and modifies the address by adding the index register to it prior to performing the desired operation. Pre- or post-index of index address is possible.

5.4 Processor Status Register

The 8-bit processor status register contains seven status flags. Some of the flags are controlled by the program, others may be controlled both the program and the CPU.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N	V	1	B	D	I	Z	C

N: Signed flag, 1 = negative, 0 = positive
V: Overflow flag, 1 = true, 0 = false
B: BRK interrupt command, 1 = BRK, 0 = IRQB
D: Decimal mode, 1 = true, 0 = false
I: IRQB disable flag, 1 = disable, 0 = enable
Z: Zero flag, 1 = true, 0 = false
C: Carry flag, 1 = true, 0 = false

5.5 Program Counter(PC)

The 16-bit program counter register provides the addresses, which step the micro-controller through sequential program instructions. Each time the micro-controller fetch an instruction from program memory, the lower byte of the program counter (PCL) is placed on the low-order 8 bits of the address bus and the higher byte of the program counter (PCH) is placed on the high-order 8 bits. The counter is incremented each time an instruction or data is fetched from program memory.

5.6 Stack Point(S)

The stack pointer is an 8-bit register, which is used to control the addressing of the variable-length stack. The stack pointer is automatically incremented and decremented under control of the micro-controller to perform stack manipulations under direction of either the program or interrupts (/NMI or /IRQ). The stack allows simple implementation of nested subroutines and multiple level interrupts. The stack pointer is initialized by the user's firmware.

6 Memory Organization

There are 144 bytes SRAM, located in address 0000H to 007FH and 1000H to 100FH, in the MG69L220A. They could be used as either working RAM or stacks according to application programs. For the purposes above, the location 0000H to 007FH and 0100H to 017FH overlap. In other words, accessing any locations inside the range 0000H to 007FH is equivalent to access the corresponding ones in the range 0100 to 017FH. All special function registers, SFRs, are located at the region 00C0H to 00FFH. Such an arrangement could benefit from the faster access time of zero-page.

There are 8K bytes program / data ROM in MG69L220A. The ROM address from E000H to FFFFH can store program and data. The address mapping of MG69L220A is shown as below

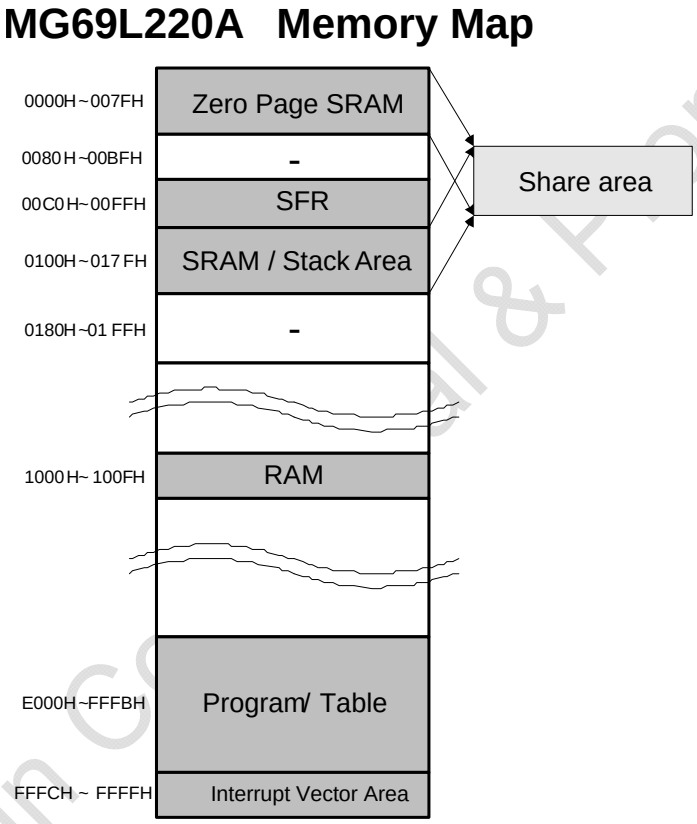


Figure 6-1 Memory Map

6.1 SFR Mapping

The address 00C0H to 00FFH is reserved for special function registers (SFR). The SFR is used to control or store the status of I/O, timers, system clock and other peripheral.

※ All SFRs are not supported by bit-manipulation instructions.

Table 6-1 SFR Table

SFR (special function register): 00C0H~00FFH

Address	Content	Default	Address	Content	Default
00C0		--------	00D0		--------
00C1		--------	00D1		--------
00C2	IRQ_EN / IRQ_ST	0-00000-	00D2	P0port	XXXXXXXX
00C3	IRQ_CLR	0-00000-	00D3	P0dir	0000----
00C4	RESFlag	--0X1--X	00D4	P0plh	11111111
00C5	RESOK	XXXX---0	00D5	P0opd	0000----
00C6		--------	00D6	P1port	---00000
00C7		--------	00D7	P1plh	---11111
00C8	TM0	11111111	00D8	P2port	00000000
00C9		--------	00D9	P3port	00000000
00CA	TM0_CTL	00---000	00DA	HSOR	1------0
00CB		--------	00DB		--------
00CC	DIV_SEL	------00	00DC	P4port	00000000
00CD	TM1	11111111	00DD	P5port	----0000
00CE		--------	00DE		0-----00
00CF	TM1_CTL	00---000	00DF		--------

Address	Content	Default	Address	Content	Default
00E0		--------	00F0	SCK_SEL	0----000
00E1		--------	00F1		--------
00E2		--------	00F2		--------
00E3		--------	00F3		--------
00E4		--------	00F4		--------
00E5		--------	00F5		--------
00E6		--------	00F6		--------
00E7		--------	00F7		--------
00E8		--------	00F8		--------
00E9		--------	00F9	CWPR	XXXXXXXX
00EA		--------	00FA		--------
00EB		--------	00FB		--------
00EC		--------	00FC	PWR_CR	-----000
00ED		--------	00FD		--------
00EE		--------	00FE		--------
00EF		--------	00FF		--------

6.2 Write Protect Function Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00F9H	CWPR	PT7	PT6	PT5	PT4	PT3	PT2	PT1	PT0	-	√

Condition Write Protect flag register (CWPR) is used to protect IRQ_CLR.7 (WDT), PWR_CR.1 (CKC0), PWR_CR.2 (CKC1), SCK_SEL. If want to change IRQ_CLR.7 (WDT), PWR_CR.1 (CKC0), PWR_CR.2 (CKC1) SCK_SEL, it must write “78H” to CWPR first.

PT7~PT0: Write Protect Pattern. In MG69L220A write protect pattern is “78H”

Note:

1. *When CWPR is written by firmware, it would be automatically cleared by hardware after the “next write action” of firmware.*

※Bit-manipulation instructions are not available on this register.

7 Interrupt

There are five kinds interrupt source is provided in MG69L220A. The flag IRQ_EN and IRQ_ST are used to control the interrupts. When flag IRQ_ST is set to '1' by hardware and the corresponding bits of flag IRQ_EN has been set by software, an interrupt is generated. When an interrupt occurs, all of the interrupts are inhibited until the CLI or STA IRQ_EN, # I instruction is invoked. Executing the SEI instruction can also disable the interrupts.

Table 7-1 Interrupt Vector Table

Vector Address	Item	Flag	Properties	Memo
FFFEH, FFFFH	P1 IRQ	IRQ_ST.1	Ext.	P1.0 ~ P1.4 interrupt vector
	P0 IRQ	IRQ_ST.2	Ext.	P0.0 ~ P0.7 interrupt vector
	TM0 IRQ	IRQ_ST.3	Int.	TM0 underflow interrupt
	TM1 IRQ	IRQ_ST.4	Int.	TM1 underflow interrupt
	DIV IRQ	IRQ_ST.5	Int.	Divider carry out interrupt
FFFCH, FFFDH	RESET	None	Ext.	Initial reset
	WDT	IRQ_ST.7	Int.	Watch dog timer reset
	LVR	None	Int.	Low voltage reset

7.1 Interrupt Register

IRQ enable flag

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C2H	IRQ_EN	PDBOR	-	DIVx	TM1	TM0	P0	P1	-	-	√

Program can enable or disable the ability of triggering IRQ through this register.
0: Disable (default "0" at initialization)
1: Enable
P0: Falling edge occurs at port 0 input mode
P1: Falling edge occurs at port 1
TM0: Timer 0 underflow
TM1: Timer 1 underflow
DIVx: Divider selected interrupt frequency occurred
PDBOR: Power down BOR (0: enable BOR IP 1: disable BOR IP)

IRQ status flag

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C2H	IRQ_ST	WDT	-	DIVx	TM1	TM0	P0	P1	-	√	-

When IRQ occurs, program can read this register to know which source triggering IRQ. If the interrupt triggering is enabled and the interrupt event is accepted, the correspond IRQ status flag should be cleared by program after the interrupt vector is loaded into program counter.

IRQ clear flag

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C3H	IRQ_CLR	WDT	-	DIVx	TM1	TM0	P0	P1	-	-	√

Program can clear the interrupt event by writing '1' into the corresponding bit. The IRQ_CLR.7 (WDT) is protected by CWPR.

Reset status flag

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C4H	RESFlag	-	-	IAR_F	EXTR_F	LVPOR			LVD	√	√

IAR_F: Illegal address reset flag. (reset by POR and LVR)
1:An illegal address reset occurs.
0:This bit is set by hardware and clears by writing ‘1’.

EXTR_F: External reset flag (reset by POR and LVR)
1: An external reset occurs.
0:This bit is set by hardware and clears by writing ‘1’.

LVPOR: Low voltage reset and POR reset occur. (set by POR and LVR)
1:VDD is under 1.8V or power-on.
0: This bit is set by hardware and clears by writing ‘1’.

LVD: Low voltage0 detected. (POR, LVR, BOR, illegal address reset and external reset)
1:VDD is under 2.1V.
0:This bit is set by hardware and clears by writing ‘1’.

7.2 Interrupt System

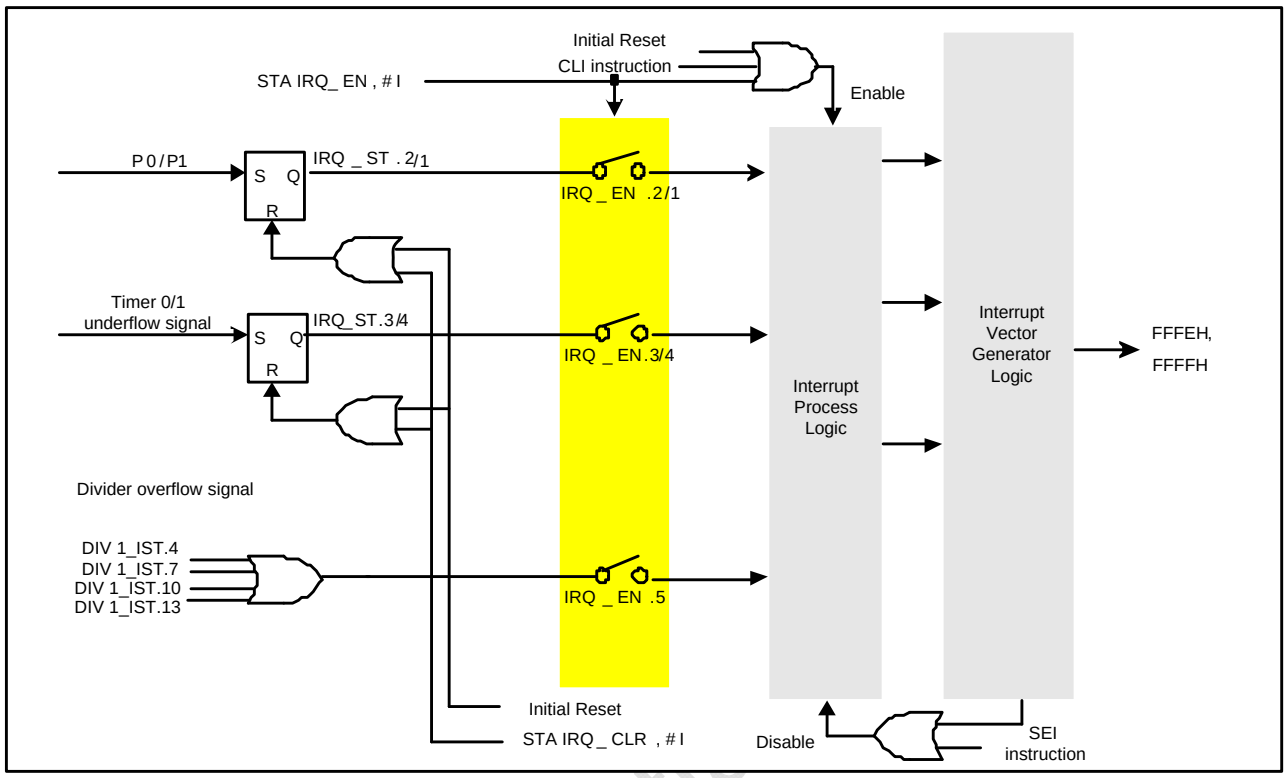


Figure 7-1 Interrupt System Diagram

8 Reset

8.1 Low Voltage Reset (LVR)

The MG69L220A provides low voltage reset circuit in order to monitor the supply voltage of the device. If the supply voltage of the device is within the range 0.9V ~ VLVR, such as changing a battery, the LVR will automatically reset the device internally.

The LVR includes the following specifications

1. The low voltage (0.9V~VLVR) has to remain in their original state to exceed 1ms. If the low voltage state does not exceed 1ms, the LVR will ignore it and do not perform a reset function.
2. In the LVR mode, the clock source (INT./EXT. OSC) continuous oscillating and the IO status becomes default value.

8.2 Watchdog Timer (WDT)

(The example is base on 32.768KHz and SCK_SEL.1 = 1)

Name								Bit 8	R	W
WDT								1.9 (Hz)	-	-

The watchdog timer time-out period is obtained by the equation: (F_{DIV} /512)/512 or (F_{DIV} /4096)/512 select by SCK_SEL.1 (CKS1).
Before watchdog timer time-out occurs, the program must clear the 9-bit WDT timer by writing 1 to IRQ_CLR.7.
WDT overflow will cause system reset and set IRQ_CLR.7 to high.

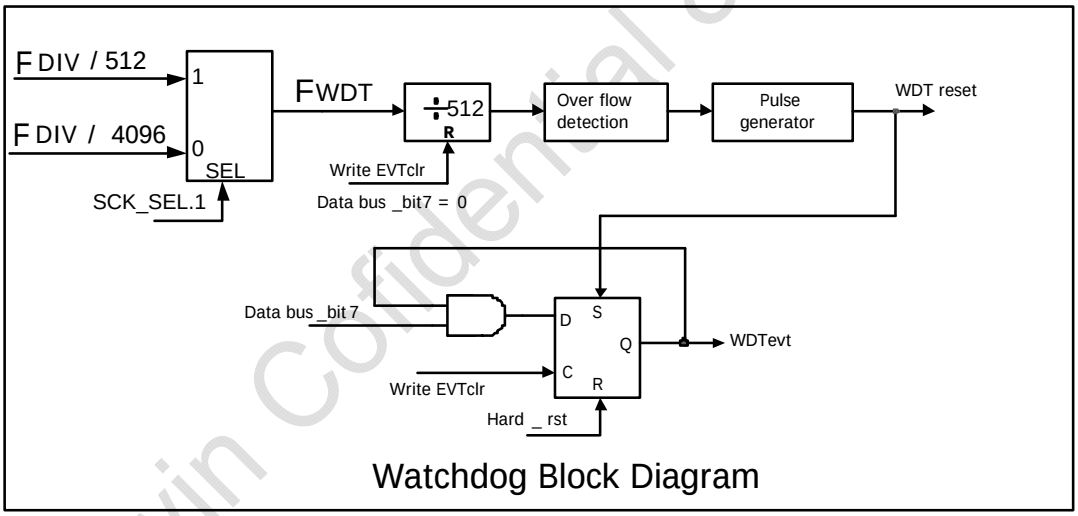


Figure 8-1 Watch Dog Diagram

8.3 Reset OK

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C5H	RESOK	RK7	RK6	RK5	RK4	-	-	-	IO_RES	-	√

RESOK (Reset OK): If the device reset OK and work well, **must** write #$90 into this register.
For example:

```
Program_start:    LDA    #10010000b
                  STA    $C5
```

IO_RES: IO reset selector.
0:IO status is reset by WDT, IA reset, LVR and POR, EXT_RESET (Default).
1:IO status is reset by LVR, EXT_RESET and POR.

9 Power Control

9.1 Power Control Register

System clock selector (※The Clock Control Register is protected by CWPR.)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00F0H	SCK_SEL	CKS7	-	-	-	-	CKS2	CKS1	CKS0	-	√

CKS0: F_{CPU} clock source select. 0: F_{OSC}, 1: F_{X32}
CKS1: Watchdog clock source select. 0: F_{DIV}/4096, 1: F_{DIV}/512
CKS2: De-bounce (awakened from stop mode) time selector. 0: F_{OSC}/16384, 1: F_{OSC}/256
CKS7: Select the input clock source of divider. 0: F_{OSC}, 1: F_{X32}

Power saving control

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00FCH	PWR_CR	-	-	-	-	-	CKC1	CKC0	HALT	-	√

※ CKC1 and CKC0 are protected by CWPR

CKC1	CKC0	System clock control
0	0	F_{OSC} enable, F_{X32} enable (Dual mode)
0	1	F_{OSC} enable, F_{X32} disable (Single mode)
1	0	F_{OSC} disable, F_{X32} enable (Slow mode)
1	1	F_{OSC} disable, F_{X32} disable (Stop mode)

Note: Dual mode and slow mode is inhibited when code option is selected to F_{X32} disable.

HALT: F_{CPU} off-line control bit. 1: F_{CPU} off-line, 0: F_{CPU} on-line

Program can switch the normal operation mode to the power-saving mode for saving power consumption through this register. There are three power saving modes in this system.

Slow mode: *(PWR_CR.CKC1 = 1, PWR_CR.CKC0 = 0)*
The main uC clock (F_{OSC}) stops oscillating. Only very low power is needed for uC to keep running.

Stop mode: *(PWR_CR.CKC1 = 1, PWR_CR.CKC0 = 1)*
Both system clocks stop oscillating. The uC can be awakened from stop mode by 4-ways: port 0 falling edge, port 1 falling edge, hardware reset, or power-on reset. When the stop mode is released, only the oscillator, which is providing the uC clock, will be enabled again.
If uC clock source is F_{X32} and system into STOP mode (set PWR_CR[2:1] = 11). The F_{X32} will be enabled and F_{OSC} still keep same status, when uC waken up by port0 or port1.

Halt mode: *(PWR_CR.HALT = 1)*
The F_{CPU} clock in off-line status. The oscillator(s) still keep same status. The uC can be awakened from halt mode by 3-ways: the interrupt events, hardware reset, or power-on reset.

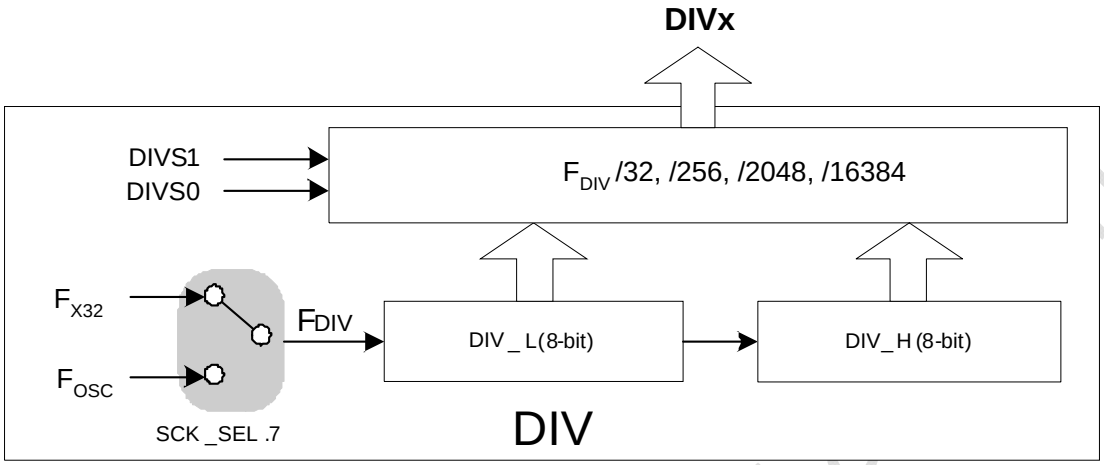
10 Divider

10.1 Divider

DIV interrupt selector

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00CCH	DIV_SEL	-	-	-	-	-	-	DIVS1	DIVS0	-	√

The divider clock source comes from F_{X32} (sub-main clock) or F_{OSC} (main clock).
Program can select divider interrupt frequency by DIV_SEL register.



DIVS1	DIVS0	DIV interrupt occurs status
0	0	F_{DIV} / 16384
0	1	F_{DIV} / 2048
1	0	F_{DIV} / 256
1	1	F_{DIV} / 32

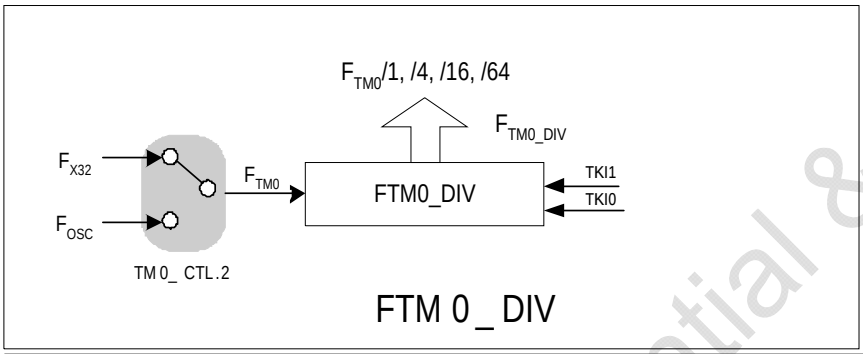
11 Timer

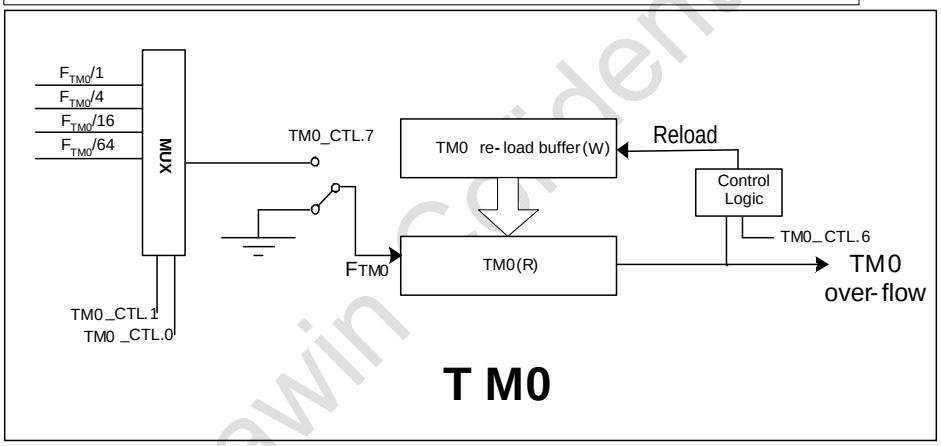
11.1 Timer0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C8H	TM0	T7	T6	T5	T4	T3	T2	T1	T0	√	√
00CAH	TM0_CTL	STC	RL/S	-	-	-	TCS0	TKI1	TKI0		√

Timer 0 is an 8-bit down-count counter.
STC: Start/Stop counting. 1: start and pre-load the value to counter, 0: stop timer clock
RL/S: Auto-reload disable/enable. 1: disable auto-reload, 0: enable auto-reload
TCS0: select the input clock source of timer0. 0:F_{OSC}, 1: F_{X32}

TKI1	TKI0	Selected TM0 input frequency (F_{TM0_DIV})
0	0	F_{TM0} / 1
0	1	F_{TM0} / 4
1	0	F_{TM0} / 16
1	1	F_{TM0} / 64





F_{TM0_UV}, can be calculated with the equation:
$F_{TM0\_UV} = F_{TM0} / (TM0+1)$, where the F_{TM0} is the timer input frequency set by TKI1 and TKI0.

For example: (if F_{TM0} = 2.000MHz, TKI1=TKI0=0)

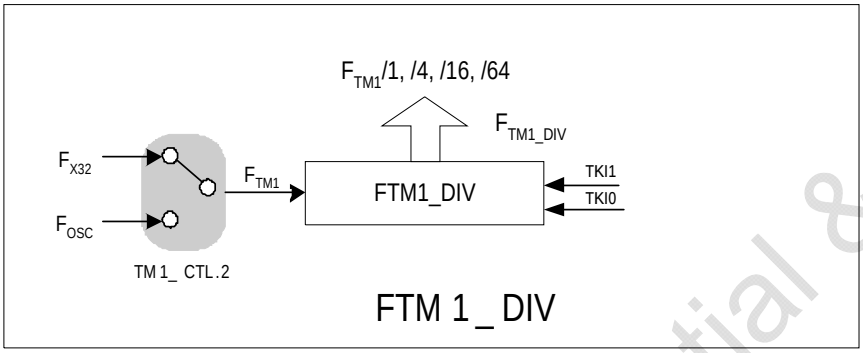
TM0	Frequency
00H	Reserved
01H	1.000MHz
02H	667kHz
…	…
FFH	7.84kHz

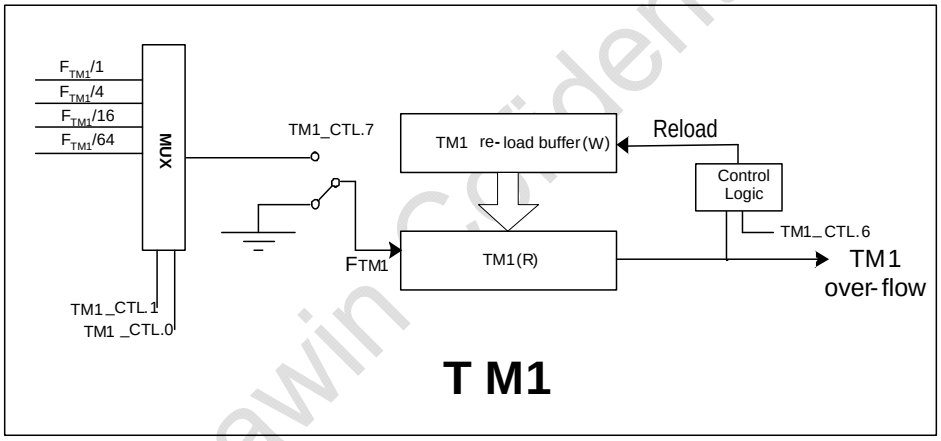
11.2 Timer1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00CDH	TM1	T7	T6	T5	T4	T3	T2	T1	T0	√	√
00CFH	TM1_CTL	STC	RL/S	-	-	-	TCS1	TKI1	TKI0		√

Timer 1 is an 8-bit down-count counter.
STC: Start/Stop counting. 1: start and pre-load the value to counter, 0: stop timer clock
RL/S: Auto-reload disable/enable. 1: disable auto-reload, 0: enable auto-reload
TCS1: select the input clock source of timer1. 0: F_{OSC}, 1: F_{X32}

TKI1	TKI0	Selected TM1 input frequency (F_{TM1_DIV})
0	0	F_{TM1} / 1
0	1	F_{TM1} / 4
1	0	F_{TM1} / 16
1	1	F_{TM1} / 64





F_{TM1_UV}, can be calculated with the equation:
$F_{TM1\_UV} = F_{TM1} / (TM1+1)$, where the F_{TM1} is the timer input frequency set by TKI1 and TKI0.

For example: (if F_{TM1} = 2.000MHz,TKI1=TKI0=0)

TM1	Frequency
00H	Reserved
01H	1.000MHz
02H	667kHz
…	…
FFH	7.84kHz

12 Configurable I/O Ports

12.1 Port 0

Port 0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D2H	P0port	P07	P06	P05	P04	P03	P02	P01	P00	√	-

Port 0 is combined with 4-bit input port and 4-bit I/O port. P0.7~P0.4 can be programmed as input or output individually. When P0.n (n= 4~7) is configured as an output pin, the P0.n pin would output the logic content of internal P0obuf.n (P0 output buffer). The default value of P0obuf is `0000----`b.
When the P0.n is configured as output mode, reading P0.n would always read logic '0'.
When the P0.n is configured as input mode, reading P0.n would always read the logic value from pad.

Port 0 Output Buffer

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D2H	P0port	P07	P06	P05	P04	-	-	-	-	-	√

This register is used to buffer the output value of P0.7 ~ P0.4 in output mode and it is write-only.

※ Bit-manipulation instructions are not available on this register.

Port 0 Direction Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D3H	P0dir	DR7	DR6	DR5	DR4	-	-	-	-	-	√

P0_DR (Port 0 Direction)

P0_DR.n = 0: P0.n is configured as an input pin. (Default)
1: P0.n is configured as an output pin.

※ Bit-manipulation instructions are not available on this register.

Port 0 Pull-high Control Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D4H	P0plh	PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0	-	√

1: Enable internal pull-high (default); 0: Disable internal pull-high
PHn: Control bit is used to enable the pull-high of P0.n pin.

※ Bit-manipulation instructions are not available on this register.

Port 0 Open-Drain Control Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D5H	P0opd	OD7	OD6	OD5	OD4	-	-	-	-	-	√

0: Disable open-drain output (CMOS output); 1: Enable open-drain output
ODn: Control bit is used to enable the open-drain of P0.n pin.

※ Bit-manipulation instructions not available on this register.

12.2 Port 1

Port 1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D6H	P1port	-	-	-	P14	P13	P12	P11	P10	√	√

Port1 is a 5-bit quasi-bi-directional open drain output with internal pull-high resistors. This register is used to buffer the output value of P1.0 ~ P1.4. Reading P1.n would always read the logic value from pad. **The pull-high resistors will be temporarily disable if the output value is low.**

※ Bit-manipulation instructions are not available on this register.

Port 1 Pull-high Control Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D7H	P1plh	-	-	-	PH4	PH3	PH2	PH1	PH0	-	√

1: Enable internal pull-high (Default)
0: Disable internal pull-high
PHn: Control bit is used to enable the pull-high of P1.n pin.

※ Bit-manipulation instructions are not available on this register.

12.3 Port 2

Port 2

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D8H	P2port	P27	P26	P25	P24	P23	P22	P21	P20	-	√

Port2 is an open drain output port with internal pull-high resistors. This register is used to buffer the output value of P2.0 ~ P2.7. **The pull-high resistors will be temporarily disable if the output value is low.**

※ Bit-manipulation instructions are not available on this register.

12.4 Port 3

Port 3

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D9H	P3port	P37	P36	P35	P34	P33	P32	P31	P30	-	√

Port3 is open drain output with internal pull-high resistors when segment/OD option select to I/O function. This register is used to buffer out value of P3.0 ~ P3.7. **The pull-high resistors will be temporarily disable if the output value is low.**

※ Bit-manipulation instructions are not available on this register.

12.5 Port 4

Port 4

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00DCH	P4port	P47	P46	P45	P44	P43	P42	P41	P40	-	√

Port4 is open drain output with internal pull-high resistors when segment/OD option select to I/O function. This register is used to buffer out value of P4.0 ~ P4.7. **The pull-high resistors will be temporarily disable if the output value is low.**

※ Bit-manipulation instructions are not available on this register.

12.6 Port 5

Port 5

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00DDH	P5port	-	-	-	-	P53	P52	P51	P50	-	√

Port5 is open drain output(High Sink Current 16mA) with internal pull-high resistors when COM/OD option select to I/O function. This register is used to buffer out value of P5.0 ~ P5.3. **The pull-high resistors will be temporarily disable if the output value is low.**

※ Bit-manipulation instructions are not available on this register.

12.7 High sink output register

HSO Buffer

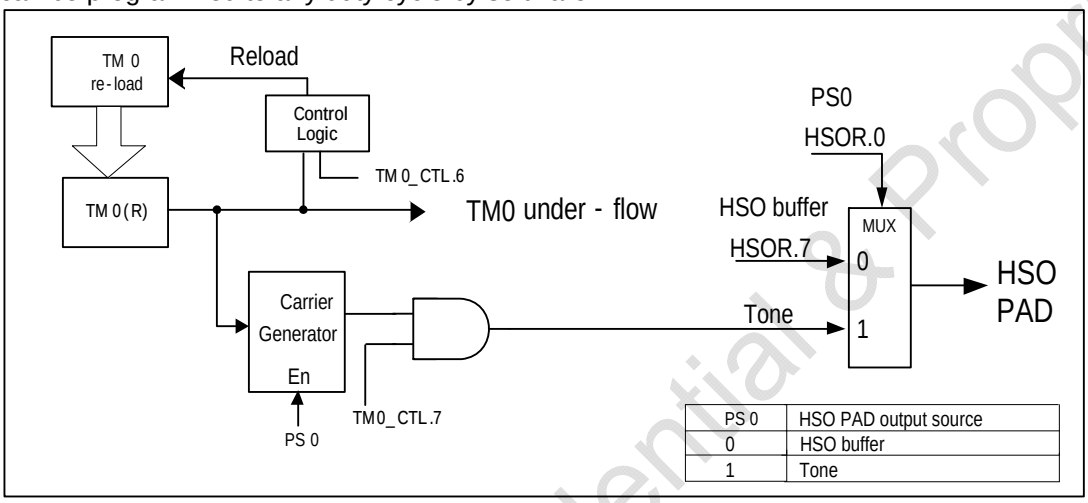
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00DAH	HSOR	HSO	-	-	-	-	-	-	PS0	-	√

HSO pad is a high sink current output pin. The HSO PAD output from HSO or Tone is select by PS0.

HSOR.7 Can set up 1/3 or 2/3 duty cycle by using instruction, writer “1”, Through HSOR to PAD output High, until writer “0”, the output status will change to Low

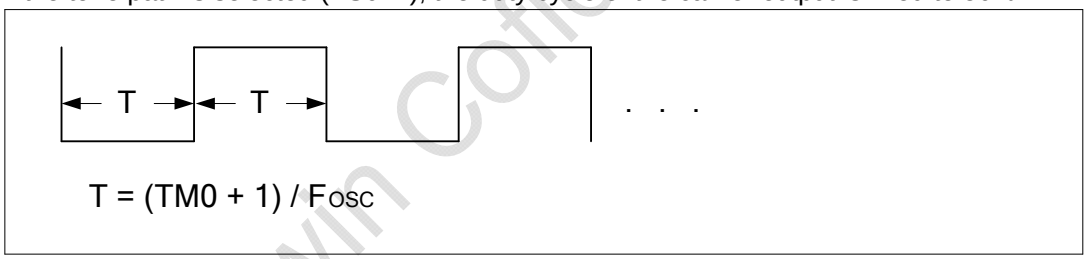
※ Bit-manipulation instructions are not available on this register.

PS0 (HSOR.0) can set the HSO pad output source as HSO buffer or tone generator. The HSO output waveform can be programmed to any duty cycle by software.



PS 0	HSO PAD output source
0	HSO buffer
1	Tone

If the tone path is selected (PS0=1), the duty cycle of the carrier output is fixed to 50%.



The counter underflow frequency of timer0 can be calculated with the equation:
$F_{TM0\_UV} = F_{TM0} / (TM0reg+1)$. The F_{TM0} is Timer0 clock input.
For example: F_{TM0} = 455KHz,TM0reg = 0BH
$F_{TM0\_UV} = F_{TM0} / (TM0reg+1) = 455K/(0BH+1) = 37.92KHz$.

13 Mask Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
				Fm	WDT		

Bit3: Fm
0 (Fm/2): FCPU clock / 2
1 (Fm): FCPU clock / 1

Bit2: WDT
0 (Disable): Disable watchdog timer function
1 (Enable): Enable watchdog function

14 Application Circuit

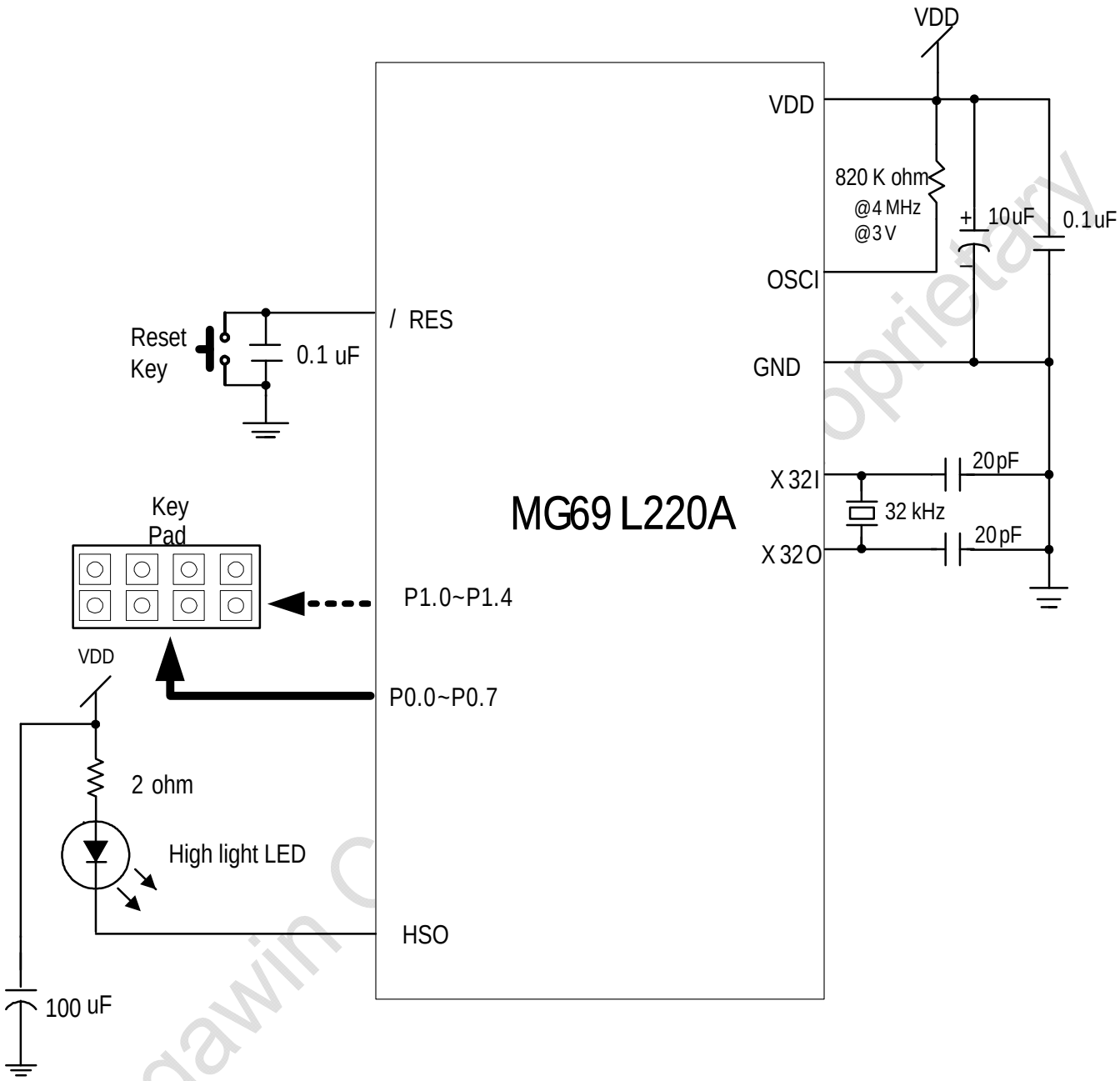


Figure 14-1 Application Circuit - Remote Controller

15 Electrical Characteristics

15.1 Absolute Maximum Rating

PARAMETER	RATING	UNIT
Supply Voltage to Ground Potential	-0.3 to +5.0	V
Applied Input / Output Voltage	-0.3 to +5.0	V
Power Dissipation	60	mW
Ambient Operating Temperature	-10 to +50	°C
Storage Temperature	-55 to +150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

15.2 DC Characteristics

(VDD-VSS = 3.0 V, FOSC = 4MHz, Ta = 25° C; unless otherwise specified)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Op. Voltage	V_{DD}	-	1.8	-	3.6	V
Op. Current 1	I_{OP}	Dual mode, No load, LCD on F_{CPU} = 4MHz	-	1.8	5.6	mA
Halt Current 1	I_{STB3}	Slow mode, HALT, No load, F_{CPU} = 32768Hz, DIV_X INT off	-	6	8	μA
Stop Current	I_{STB1}	STOP mode, No load, LCD off	-	-	1	μA
Input High Voltage	V_{IH}	-	0.7 V_{DD}	-	V_{DD}	V
Input Low Voltage	V_{IL}	-	0	-	0.3 V_{DD}	V
Port 0 Drive Current	I_{OH1}	V_{OH} = 2.4V, V_{DD} = 3.0V	10	-	-	mA
Port 0 Sink Current	I_{OL1}	V_{OL} = 0.4V, V_{DD} = 3.0V	16	-	-	mA
HSO Drive Current	I_{OH2}	V_{OH} = 2.4V, V_{DD} = 3.0V	10	-	-	mA
HSO Sink Current	I_{OL2}	V_{OL} = 1.0V, V_{DD} = 3.0V	250	-	-	mA
P1.0 to P1.4 Sink Current	I_{OL3}	V_{OL} = 0.4V, V_{DD} = 3.0V	16	-	-	mA
P2~4 Sink Current	I_{OL4}	V_{OL} = 0.4V, V_{DD} = 3.0V	10			mA
P5 Sink Current	I_{OL5}	V_{OL} = 0.4V, V_{DD} = 3.0V	16			mA
P0 Internal Pull-high Resistor	R_{PH1}	V_{IL} = 0V	25K	50K	75K	Ω
P1~5 Internal Pull-high Resistor	R_{PH2}	V_{IL} = 0V	25K	50K	75K	Ω
/RES Pull-high Resistor	R_{RES}	VIL = 0V	-	30K	-	Ω
Low Voltage Detector for uC	V_{LVD0}	VDD > 2.1V	2.0	2.1	2.2	V
Low Voltage Reset	V_{LVR}	-	1.7	1.8	1.9	V

15.3 AC Characteristics

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Built-in CPU Op. Frequency	F_{CPU}	RC, V_{DD} = 3.0V	0.5	4	6	MHz
Frequency Deviation by Voltage Drop for RC Oscillator	$\frac{\Delta f}{f}$	$\frac{f(3.6V) - f(2.6)}{f(3.0V)}$	-	3	10	%
POR Duration	T_{POR}	F_{OSC} = 4 MHz	-	4	1	mS
System Start-Up Time	T_{SST}	Power-up, reset	-	16384	-	$1/F_{CPU}$
System Wake-Up Time	T_{SWT}	Wake-up from STOP mode	256	-	16384	$1/F_{CPU}$

16 Revision History

Revision	Page	Descriptions	Date
V0.01		Datasheet release	2012/02/01
V0.02		Modify halt mode current	2012/03/01
V0.03		----------	2012/03/19
V0.04		----------	2012/03/22