Version: 2.0

MG69L331

Data Sheet

8-Bit Micro-Controller with IR function

Version 2.0

Table of Contents

1 Features

- Single Chip 8-bit CPU
- Operation voltage: 1.8V to 3.6V
- Memory
  - Program OTP ROM : 16K Bytes
  - Data RAM : 128 Bytes
- 11 input/output pins with pull high resistor and TK-scan function.
- 2 input/output pins with pull high resistor and PWM output function.
- 2 output pins shared with oscillator pad by code option.
- 1 dedicated push pull I/O combined with IR amplifier input.
- Stop mode: micro-controller no operation. (High speed oscillator stops oscillating)
- Build-in 4MHz +/- 1.5% internal oscillator.
- Watchdog timer built-in.
- One re-loadable 8-bit timer and one 8-bit timer with one capture function.
- Build-in low voltage detector (2.3V) and low voltage reset (typical voltage: below 1.8V).
- Oscillator (455K resonator or 3.58M/4M crystal).

Selection Information

	MG69L331A
ROM (Program ROM)	16K x 8-bit (16K x 8-bit)
I/O	16(max)

1.1 Application Field

General IR Controller, Toy

2 General Description

MG69L331A integrates an 8-bit CPU core, SRAM, timer and system control circuits by a CMOS silicon gate technology. The ROM can store data table and program.

Fifteen I/O and one large sink output pin make this chip very suitable for IR application.

3 Pin Configurations

3.1 Pad Assignment

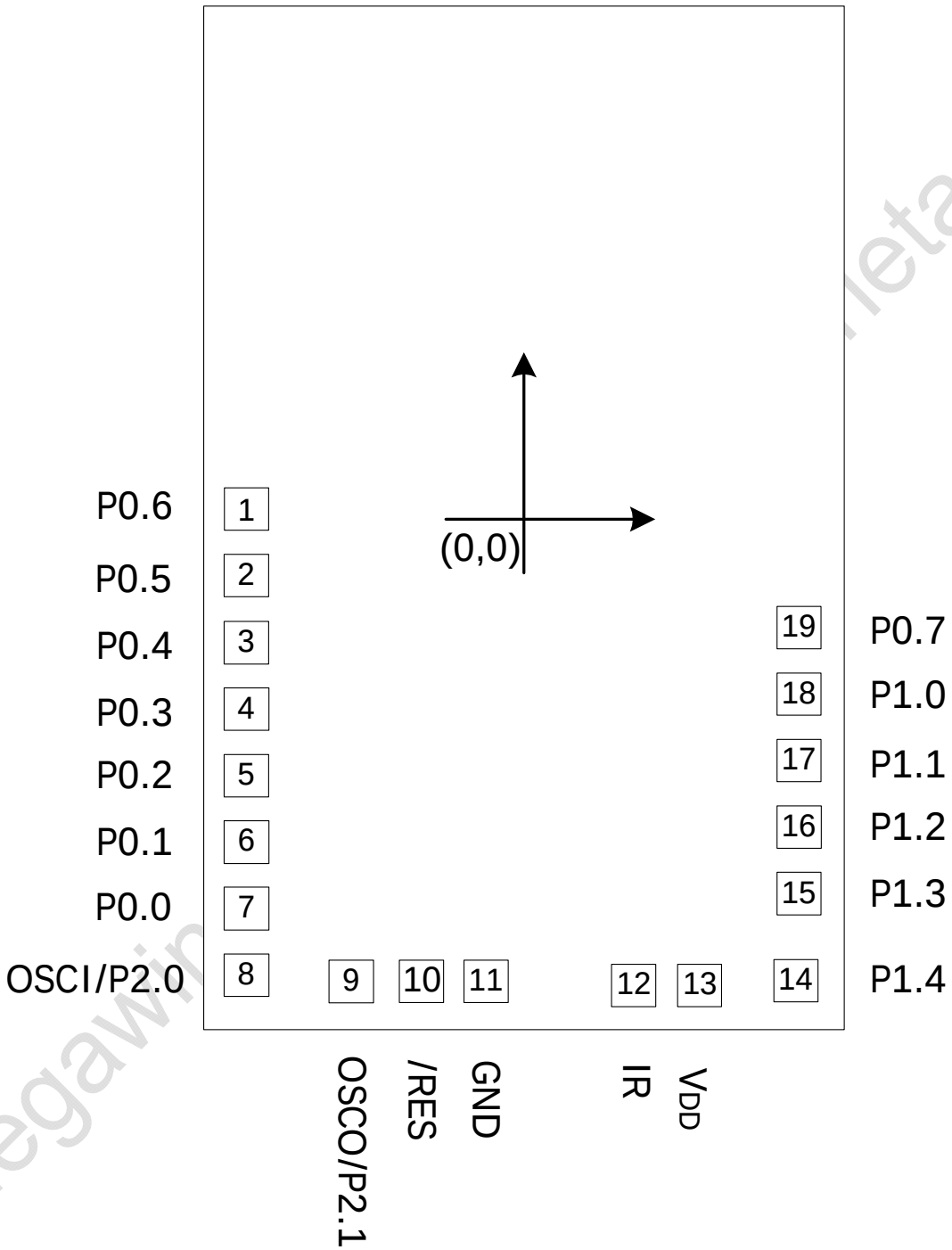


Figure 3-1 Pad Assignment

3.2 Pin Description

Table 3-1 Pin Description

Pad No.	Pad Name	I/O	Description
9, 8	OSCO/P2.1, OSCI/P2.0	O, I/O	Resonator or crystal oscillator pins shared with P2
13	VDD	P	Positive power pins
10	/RES	I	System reset pin (low active). Built in pull up 30K ohms.
11	GND	P	Ground pin
12	IR	I/O	IR input/output pin. Direct sink (sink current: 250mA) for IR LED. Default value is high after reset. The IR output pin is inverting bit7 of IR_CTL Buffer. So, write “1” to bit7 of the IR_CTL buffer the IR is output “0” and write “0” to bit7 of the IR_CTL buffer the IR is output “1”.
17 ~ 14	P1.0 ~ P1.4	I/O	Programmable I/O ports, input with pull high, CMOS output and interrupt function. The P1.0 ~ P1.2 can be used as TK-scan function in stop mode and also can be shared with timer0 function.
7 ~ 1, 19	P0.0 ~ P0.7	I/O	Programmable I/O ports, CMOS output, Input with pull high and interrupt function. The P0.0 ~ P0.7 can be used as TK-scan function in stop mode.

Note: In the “Type” field,
“I” means input only.
“O” means output only.
“B” means bi-direction.
“P” means Power, “G” means Ground.

4 Block Diagram

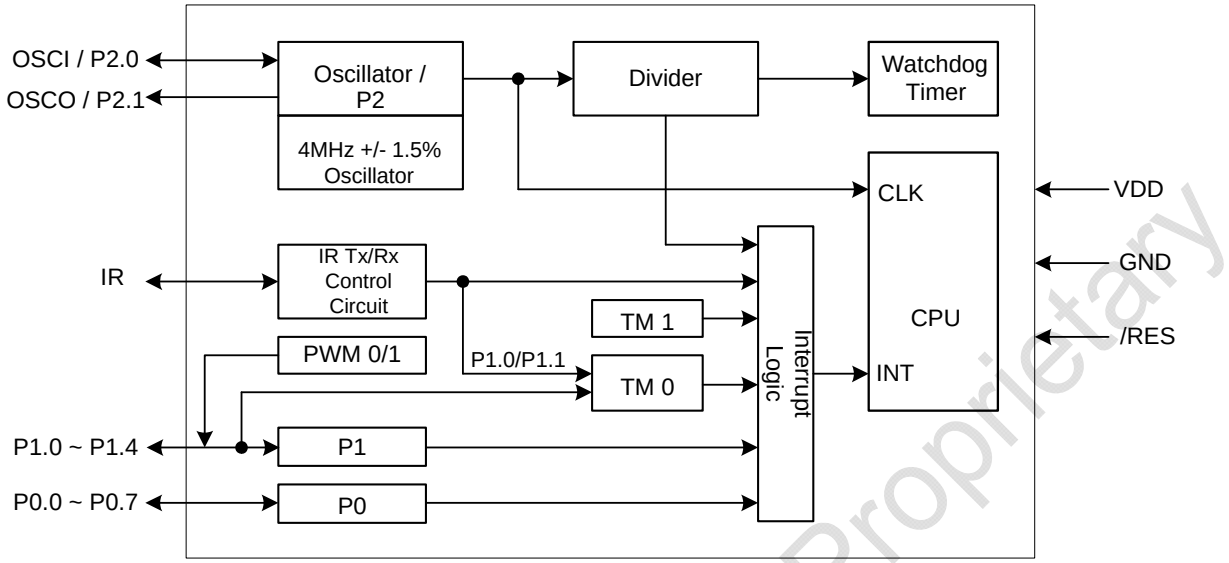


Figure 4-1 Block Diagram

5 Function Description

5.1 Registers

	A
	Y
	X
	P
PCH	PCL
1	S

5.2 Accumulator

The accumulator is a general-purpose 8-bit register, which stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of two data words used in these operations.

5.3 Index Register(X,Y)

There are two 8-bit index registers (X and Y), which may be used to count program steps or to provide an index value to be used in generating an effective address. When executing an instruction, which specifies indexed addressing, the CPU fetches the OP Code and the base address, and modifies the address by adding the index register to it prior to performing the desired operation. Pre- or post-index of index address is possible.

5.4 Processor Status Register

The 8-bit processor status register contains seven status flags. Some of the flags are controlled by the program, others may be controlled both the program and the CPU.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N	V	1	B	D	I	Z	C

N: Signed flag, 1 = negative, 0 = positive
V: Overflow flag, 1 = true, 0 = false
B: BRK interrupt command, 1 = BRK, 0 = IRQB
D: Decimal mode, 1 = true, 0 = false
I: IRQB disable flag, 1 = disable, 0 = enable
Z: Zero flag, 1 = true, 0 = false
C: Carry flag, 1 = true, 0 = false

5.5 Program Counter(PC)

The 16-bit program counter register provides the addresses, which step the micro-controller through sequential program instructions. Each time the micro-controller fetch an instruction from program memory, the lower byte of the program counter (PCL) is placed on the low-order 8 bits of the address bus and the higher byte of the program counter (PCH) is placed on the high-order 8 bits. The counter is incremented each time an instruction or data is fetched from program memory.

5.6 Stack Point(S)

The stack pointer is an 8-bit register, which is used to control the addressing of the variable-length stack. The stack pointer is automatically incremented and decremented under control of the micro-controller to perform stack manipulations under direction of either the program or interrupts (/NMI or /IRQ). The stack allows simple implementation of nested subroutines and multiple level interrupts. The stack pointer is initialized by the user's firmware.

6 Memory Organization

There are 128 bytes SRAM in MG69L331A. They are working RAM (0000H to 007FH) and stacks (0100H to 017FH). The stack area is shared with address 0000H to 007FH. The addresses 00E0H to 00F5H are special function registers area. Bit-manipulation instruction is available on SRAM except SFR.

There are 16K bytes program/data ROM in MG69L331A. The ROM address from C000H to FFFFH can store program and data. The address mapping of MG69L331A is shown as below.

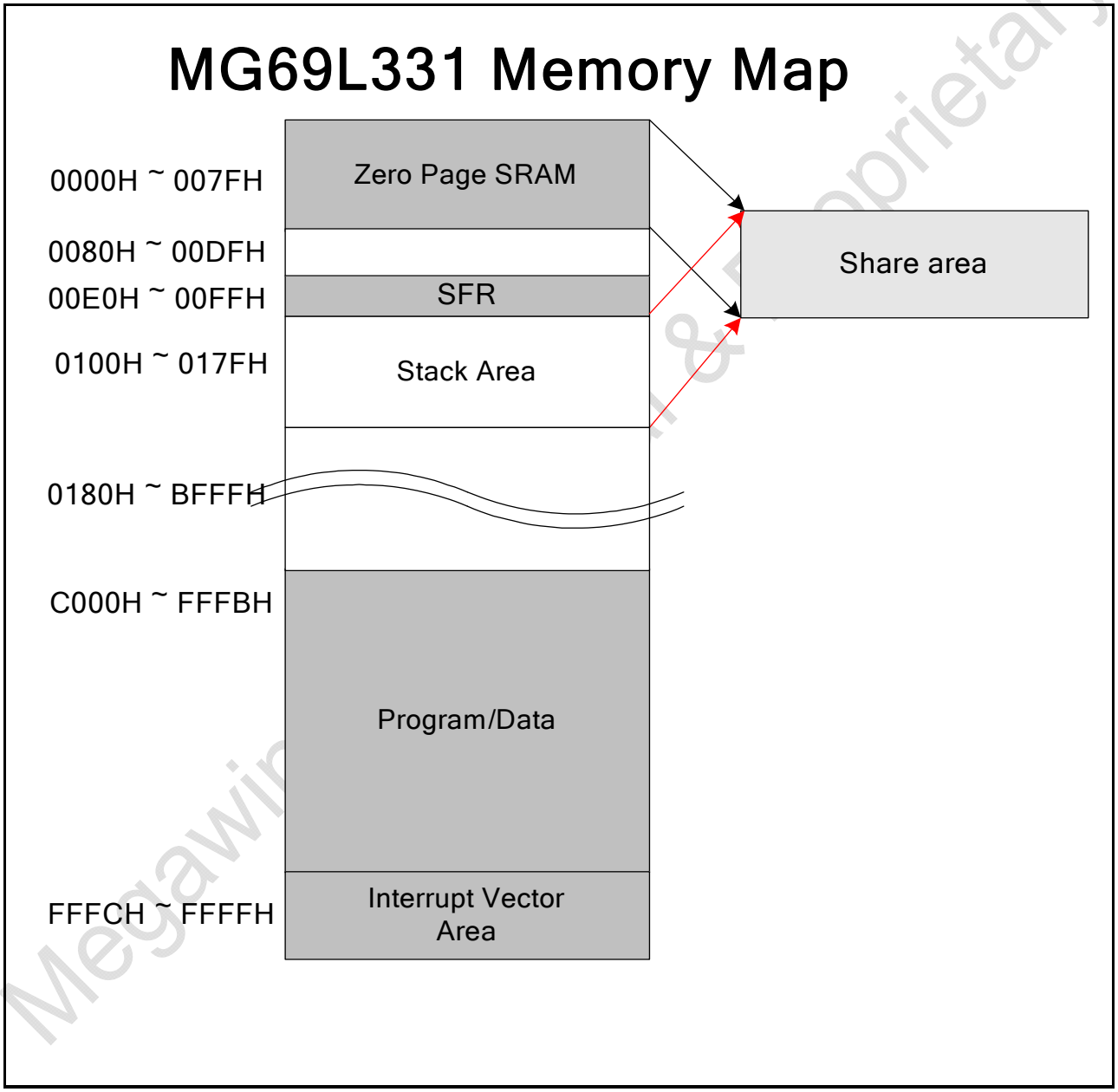


Figure 6-1 Memory Map

6.1 SFR Mapping

The address 00C0H to 00FFH is reserved for special function registers (SFR). The SFR is used to control or store the status of I/O, timers, system clock and other peripheral.

※ All SFRs are not supported by bit-manipulation instructions.
※ Please initialize all the SFRs after power-on.

Table 6-1 SFR Table

SFR (special function register): 00E0H ~ 00FBH (page 0 area)

Address	Content	Default	Address	Content	Default
00E0	MCLKmgr	0--0---0	00F0	P0obuf (W)/P0pad (R)	00000000
00E1		--------	00F1	P0dir	00000000
00E2	IRQen	0--00000	00F2		--------
00E3	EVTflag & EVTclr (Hard_rst)	0X000000	00F3		--------
00E4		--------	00F4	P1obuf(W)/P1pad(R)	---00000
00E5		--------	00F5	P1dir	---00000
00E6		--------	00F6		--------
00E7		--------	00F7		--------
00E8	TM0	11111111	00F8		--------
00E9	TM0_CTL	00000000	00F9		--------
00EA	TM0_CAP	00000000	00FA	IR_CTL	00-00000
00EB	TM0_CAP_C	11111111	00FB	TKSCAN	XXXXXXXX
00EC	TM1	11111111	00FC	P2obuf	------11
00ED	TM1_CTL	000----0	00FD		--------
00EE	PWM0	10000000	00FE	TRIM0	00000000
00EF	PWM1	10000000	00FF		--------

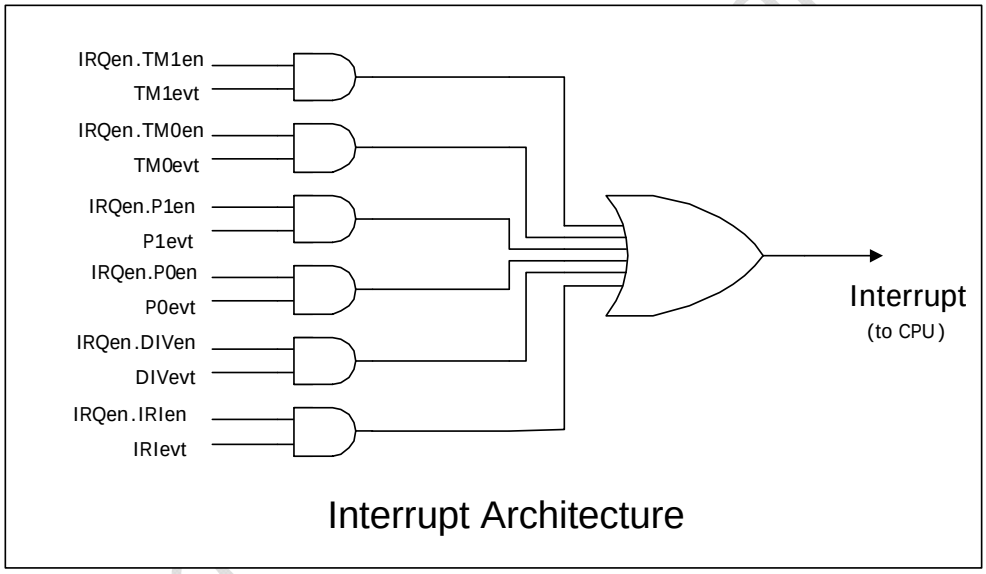
7 Interrupt

The MG69L331A provides 6 interrupt sources: P0, P1, IRI, TM0, TM1 and divider. Each of the Interrupt sources can be individually enabled or disabled by setting or clearing the corresponding bit in the IRQen. Six interrupts share the interrupt vector FFFEH/FFFFH.

Examples:
DIV interrupt: When IRQen.DIVen = 1 and DIVevt = 1.
P0 interrupt: When IRQen.P0en = 1 and P0evt = 1.
TM0 interrupt: IRQen.TM0en = 1 and TM0evt = 1.

Interrupt Vectors

Vector Address	Item	Flag	Properties	Memo
FFFCH, FFFDH	RESET	None	Ext.	Initial reset
"	WDT	WDTirq	Int.	Watch dog reset
"	LVR	None	Ext.	Low voltage reset
FFFEH, FFFFH	P0	P0irq	Ext.	Port P0 interrupt vector
"	P1	P1irq	Ext.	Port P1 interrupt vector
"	IRI	IRIirq	Ext.	IRI interrupt vector
"	DIV	DIVirq	Int.	Divider carry out interrupt
"	TM0	TM0irq	Int.	TM0 underflow interrupt
"	TM1	TM1irq	Int.	TM1 underflow interrupt



Interrupt Architecture

7.1 Interrupt Register

IRQ enable flag

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E2H	IRQen	IRI	-	-	DIV	TM0	TM1	P1	P0	√	√

Programmer can enable or disable the ability of triggering IRQ through this register.
0: Disable (default "0" at initialization)
1: Enable
P0 (or P1): Falling edge occurs at port 0 (or port 1) input mode
TM1 (or TM0): Timer1 (or Timer 0) underflow occurred.
DIV: DIV interrupts frequency occurred
IRI: Edge occurs at IR pin in input mode

IRQ status flag

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E3H	EVTflag	IRI	LVD	WDT	DIV	TM0	TM1	P1	P0	√	-

When IRQ occurs, programmer can read this register to know which source triggering IRQ.

P0 (or P1): P0 (or P1) interrupt flag. Set by falling edge on any pin of port0 (or port1). Clear by software.
TM1 (or TM0): Timer1 (or Timer 0) underflow flag and the flag clear by software.
DIV: Divider interrupts flag. Clear by software.
WDT: WDT time-out flag. Clear flag and WDT counter by software.
LVD: Low voltage detected. 1: VDD is under 2.3V. 0: VDD is above 2.3V. It is set by hardware and read only.
IRI:IRI interrupt flag. Set by falling and rising edge on IRI (set by TM0_CTL.3). Clear by software.

IRQ clear flag

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E3H	EVTclr	IRI	-	WDT	DIV	TM0	TM1	P1	P0	-	√

Programmer can clear the interrupt event by writing '0' into the corresponding bit.

7.2 Interrupt System

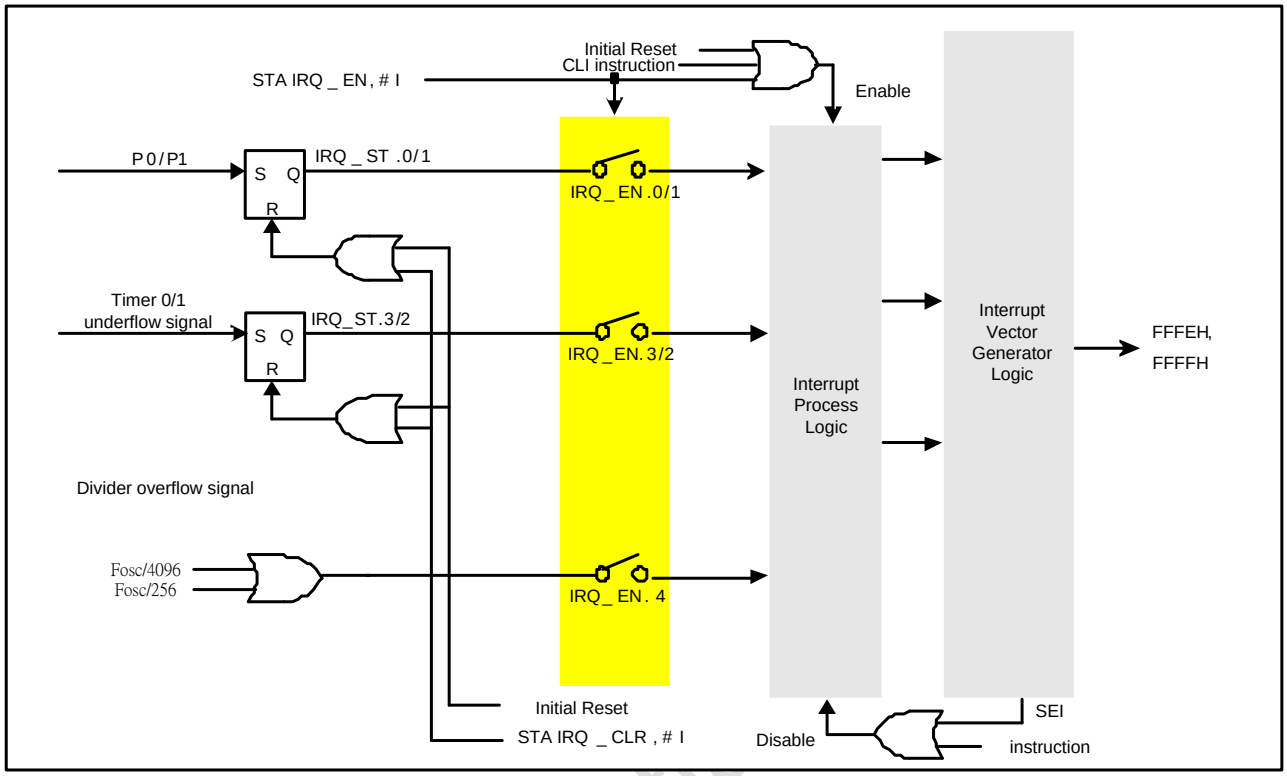


Figure 7-1 Interrupt System Diagram

8 Reset

8.1 Low Voltage Reset (LVR)

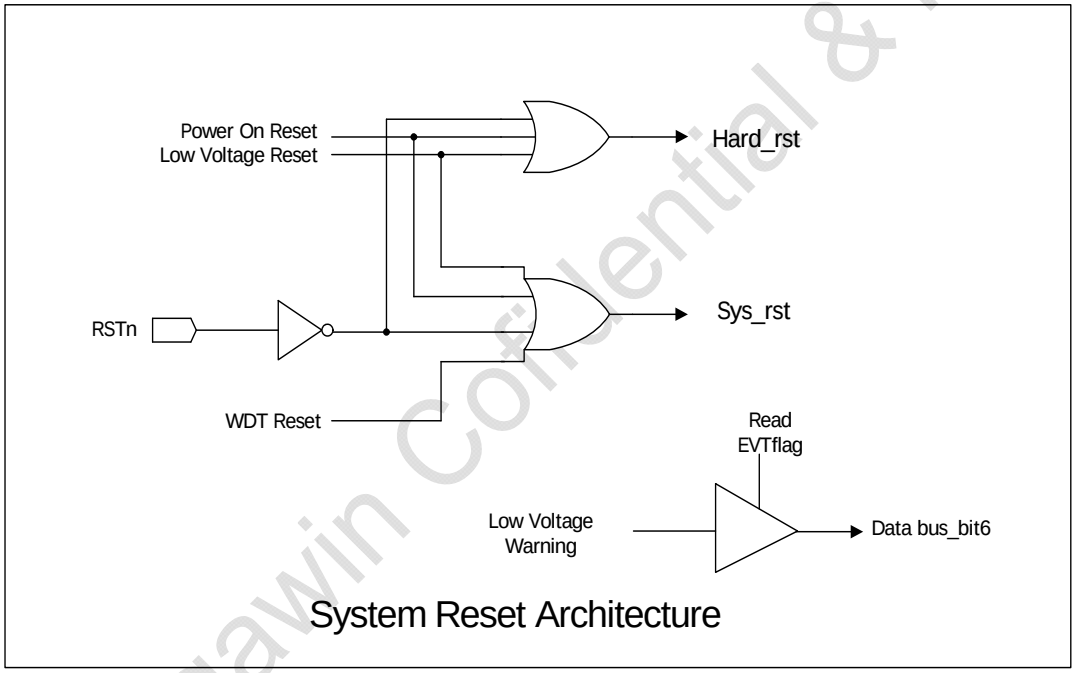
The MG69L331A provides low voltage reset circuit in order to monitor the supply voltage of the device. If the supply voltage of the device is within the range 0.9V ~ V_{LVR} , such as changing a battery, the LVR will automatically reset the device internally.

The LVR includes the following specifications:

1. The low voltage (0.9V~V_{LVR}) has to remain in their original state to exceed 1ms. If the low voltage state does not exceed 1ms, the LVR will ignore it and do not perform a reset function.
2. In the LVR mode, the on-chip oscillator is stopped and the on-chip SRAM is held. Port2 set to open drain high (pull-high disable), port0 and port1 set to input mode and IR is output floating.

8.2 Low Voltage Detector

The low voltage detector (2.3V) has no de-bounce ability. When V_{DD} is equal or lower than LVD, the LVD flag will be set high immediately. De-bounce should be implemented by software.



System Reset Architecture

8.3 Watchdog Timer (WDT)

(The example is base on 4MHz) Unit:Hz

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
WDThigh	-	-	-	-	-	-	-	1.9	-	-

The watchdog timer time-out period is obtained by the equation: (F_{osc} /4096)/512
Before watchdog timer time-out occurs, the program must clear the 9-bit WDT timer by writing 0 to EVTclr.5. WDT overflow will cause system reset and set EVTflag.5 to high.

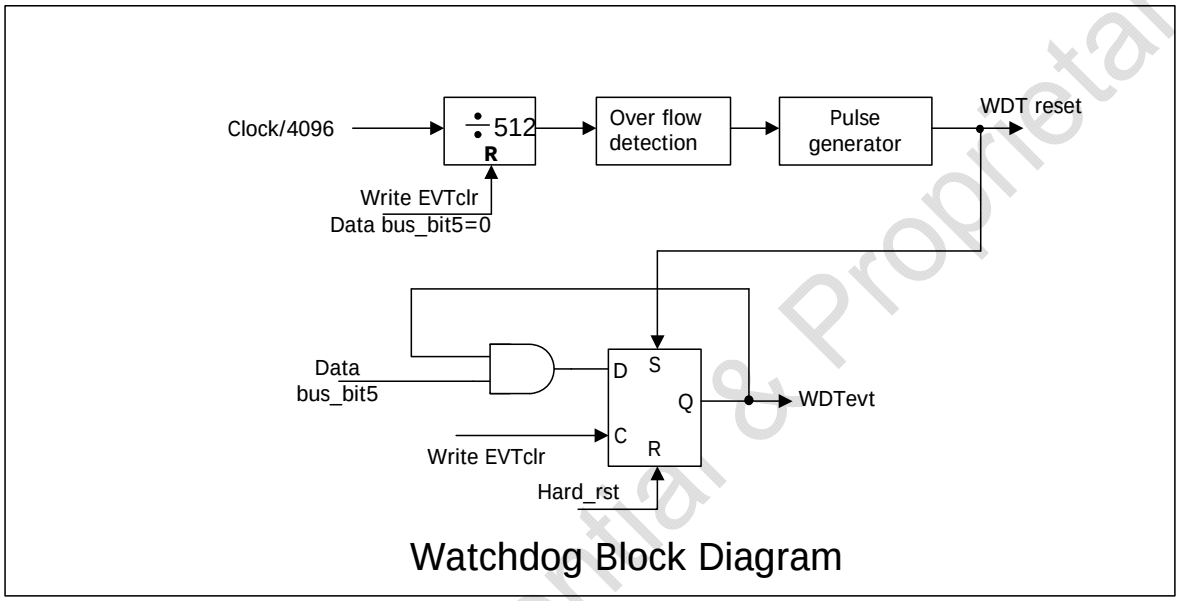


Figure 8-1 Watch Dog Diagram

8.4 Reset OK

Main Clock Manager

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E0H	MCLKmgr	ROK	-	-	DIVsel	-	-	-	OSCen	-	√

ROK (Reset OK): If the device reset OK and work well, must write any value into this bit.
For example:

```
Program_start: STZ $E0
```

9 Power Control

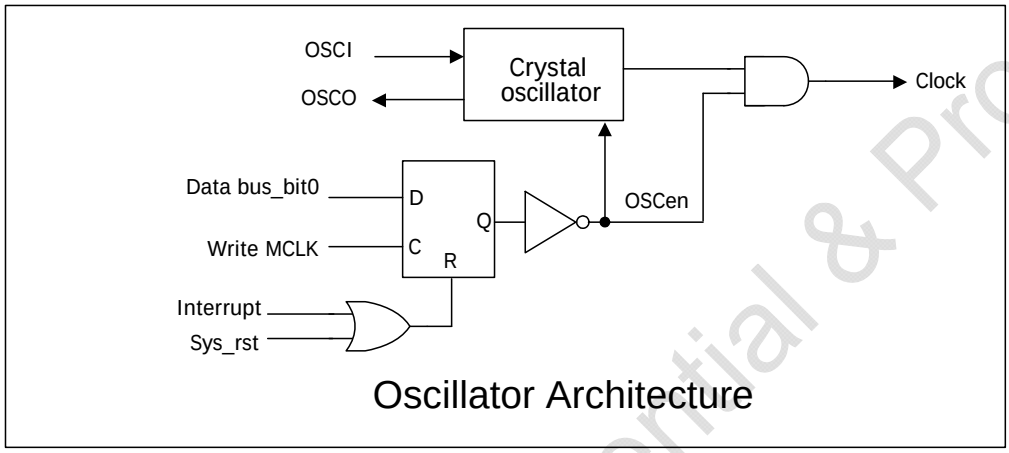
9.1 Power Control Register

Main Clock Manager

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E0H	MCLKmgr	ROK	-	-	DIVsel	-	-	-	OSCen	-	√

OSCen: 0:The oscillator is free run.
1: The oscillator is frozen (stop mode).
DIVsel: Divider interrupt frequency selector
0: The Fosc/4096 interrupt frequency is selected
1: The Fosc/256 interrupt frequency is selected

The uC can be awakened by 5-ways: port 0 interrupt, port 1 interrupt, IRI, hardware reset, or power-on reset.



Oscillator Architecture

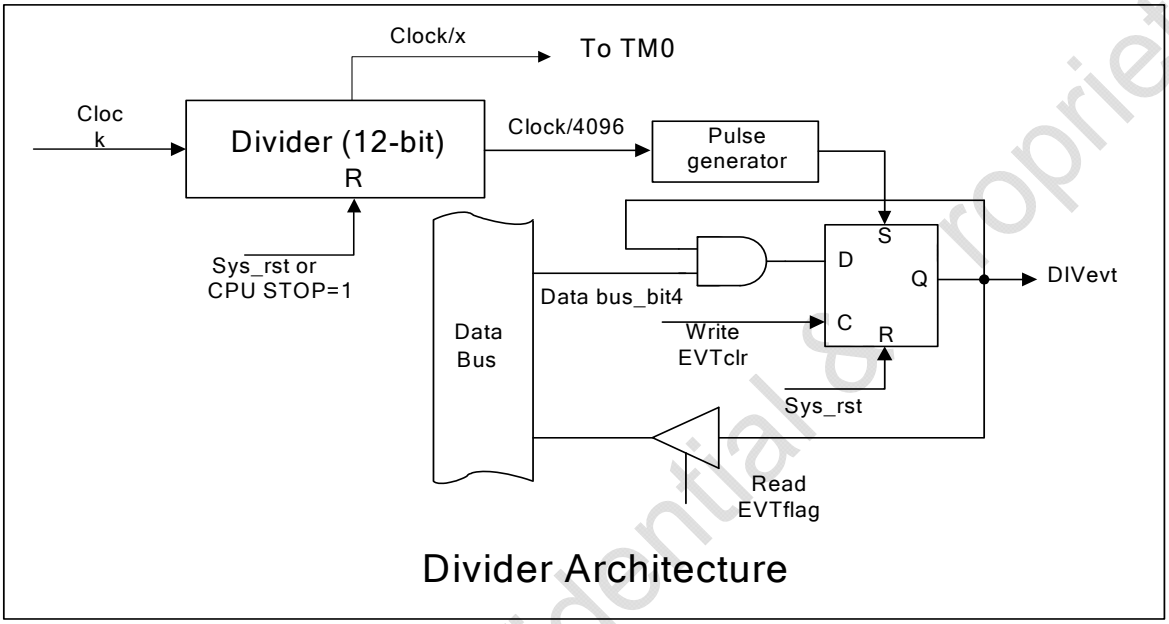
10 Divider

10.1 Divider

Divider (The example is base on 3. 579545MHz) **Unit: Hz**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
DIVlow	13984	227968	55937	111875	223750	447500	895000	1790000	-	-
DIVhigh					874	1748	3496	6992		

The time-out period is obtained by the equation: 4096/OSC.
The DIV flag will be set when 4096/OSC or 256/OSC (selected by DIVsel) is met.



Divider Architecture

11 Timer

11.1 Timer0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E8H	TM0	T7	T6	T5	T4	T3	T2	T1	T0	√	√
00E9H	TM0_CTL	STC	RL/S	TKES	CPS	CTKS	DTY	TKI1	TKI0	-	√
00EAH	TM0_CAP	CP7	CP6	CP5	CP4	CP3	CP2	CP1	CP0	√	-
00EBH	TM0_CAPB	CPB7	CPB6	CPB5	CPB4	CPB3	CPB2	CPB1	CPB0	√	-

※ Bit-manipulation instructions are not available on this register.

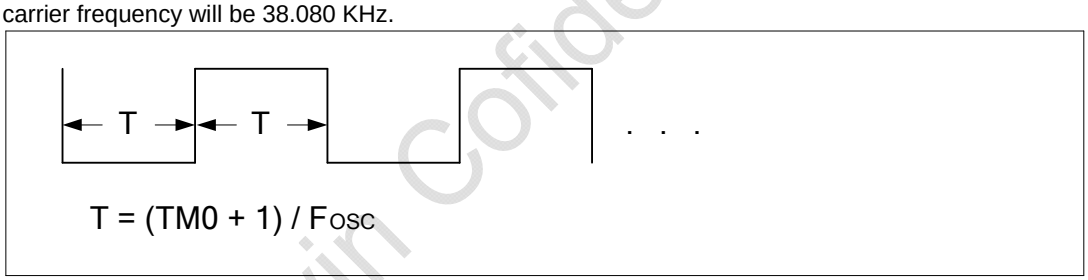
Timer 0 is an 8-bit down-count counter. The counter underflow frequency of timer 0 can be calculated with the equation: $F_{TM0\_UV} = F_{TM0} / (TM0+1)$

TM0: Read TM0 will get the counting value. Write TM0 will set the underflow value.
TM0 (R): TM0 counting value SFR.
TM0 (W): TM0 underflow reload value SFR.

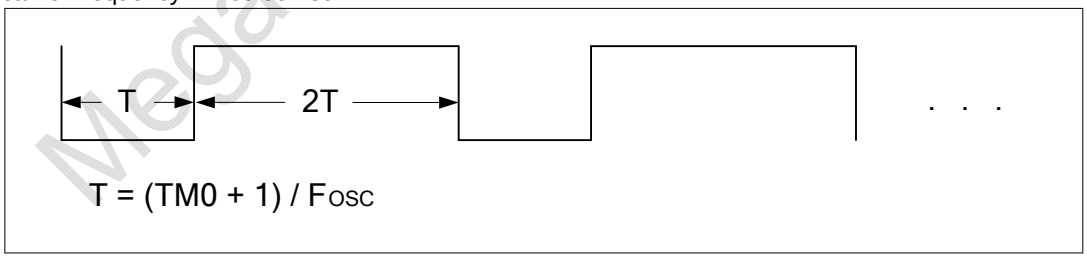
TM0_CAP: Capture the TM0 counting value.
TM0_CAPB: 1's complement of TM0_CAP.

TM0_CTL:
STC: Start/Stop counting. 1: start and pre-load the value to counter, 0: stop timer clock (set this bit to 1 will be ignored when this bit already set to 1)
RL/S: Auto-reload disable/enable. 1: disable auto-reload, 0: enable auto-reload
TKES: Event or series input clock-in trigger edge selector; 0: rising edge, 1: falling edge
CPS: Capture TM0 counting value trigger source selection. 0: IRI (IR pin configured as input mode), 1: P1.1.
CTKS: Capture source trigger edge selector; 0: rising edge, 1: falling edge

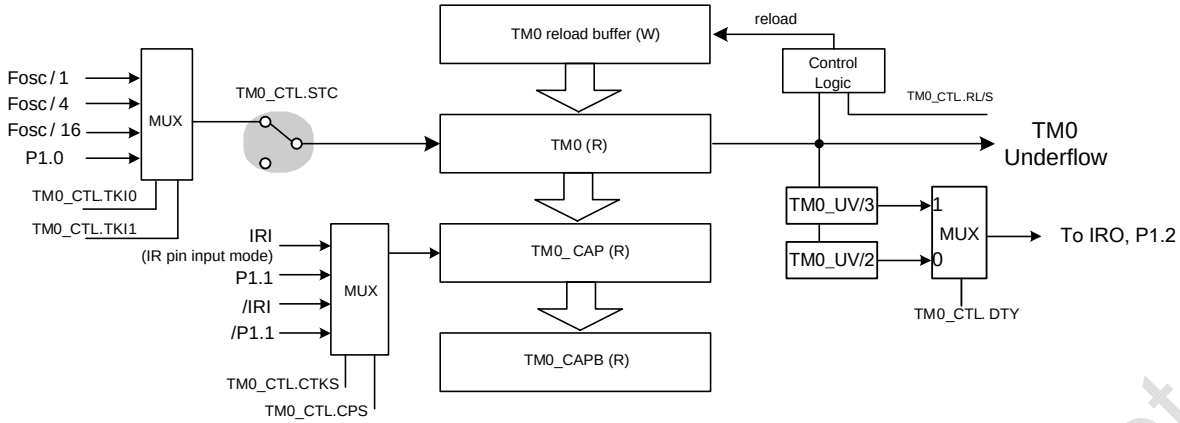
DTY: TM0 underflow duty select. "0": duty is 1:1 (high = 1, low = 1). "1": duty is 1:2 (low = 1, high = 2)
If TM0_CTL.DTY = 0, the duty cycle of the carrier output is 50%. For example: if F_{OSC} = 3.579545MHz, TM0 = 2EH, the IR carrier frequency will be 38.080 KHz.



If TM0_CTL.DTY = 1, the duty cycle of the carrier output is 33.3%. For example: if F_{OSC} = 3.579545MHz, TM0 = 1EH, the IR carrier frequency will be 38.489KHz.



TKI1	TKI0	Selected TM0 input clock source
0	0	Fosc / 1
0	1	Fosc / 4
1	0	Fosc / 16
1	1	P1.0



TM 0

11.2 Timer1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00ECH	TM1	T7	T6	T5	T4	T3	T2	T1	T0	√	√
00EDH	TM1_CTL	STC	RL/S	TKES	-	-	-	-	TKI0	-	√

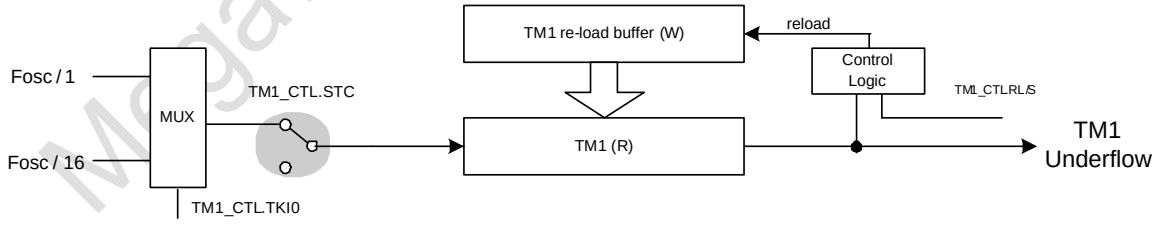
※ Bit-manipulation instructions are not available on this register.

Timer 1 is an 8-bit down-count counter. The counter underflow frequency of timer 1 can be calculated with the equation: $F_{TM1\_UV} = F_{TM1} / (TM1+1)$

TM1: Read TM1 will get the counting value. Write TM1 will set the underflow value.

TM1_CTL:
STC: Start/Stop counting. 1: start and pre-load the value to counter, 0: stop timer clock (set this bit to 1 will be ignored when this bit already set to 1)
RL/S: Auto-reload disable/enable. 1: disable auto-reload, 0: enable auto-reload
TKES: Event or series input clock-in trigger edge selector; 0: rising edge, 1: falling edge

TKI0	Selected TM1 input clock source
0	Fosc / 1
1	Fosc / 16



TM 1

12 Configurable I/O Ports

12.1 Port 0

Port 0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00F0H	P0obuf	P07	P06	P05	P04	P03	P02	P01	P00	-	√
00F0H	P0pad	P07	P06	P05	P04	P03	P02	P01	P00	√	-

P0obuf is used to buffer the output value of P0.0 ~ P0.7 and it is write-only. P0pad is used to buffer the input value of P0.0 ~ P0.7 and it is read-only. P0.0~P0.7 can be programmed as input or output individually. When P0.n is configured as an output pin, the P0.n pin would output the logic content of P0obuf.n. Reading P0pad.n would always read logic '1', if the P0.n were configured as output mode.
When the P0.n is configured as input mode, reading P0pad.n would always read the logic value from pad. **The pull-high resistors will be temporarily disabled if the output value is low.**

※ Bit-manipulation instructions are not available on this register.

Port 0 Direction Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00F1H	P0dir	DR7	DR6	DR5	DR4	DR3	DR2	DR1	DR0	-	√

P0dir.n = 0: P0.n is configured as an input pin with pull-high resistor (50K). (Default)
1: P0.n is configured as an output pin.

※ Bit-manipulation instructions are not available on this register.

12.2 Port 1

Port 1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00F4H	P1obuf	-	-	-	P14	P13	P12	P11	P10	-	√
00F4H	P1pad	-	-	-	P14	P13	P12	P11	P10	√	-

P1obuf is used to buffer the output value of P1.0 ~ P1.4 and it is write-only. P1pad is used to buffer the input value of P1.0 ~ P1.4 and it is read-only. P1.0~P1.4 can be programmed as input or output individually. When P1.n is configured as an output pin, the P1.n pin would output the logic content of P1obuf.n. Reading P1pad.n would always read logic '1', if the P1.n were configured as output mode. When the P1.n is configured as input mode, reading P1pad.n would always read the logic value from pad. **The pull-high resistors will be temporarily disabled if the output value is low.**

※ Bit-manipulation instructions are not available on this register.

Port 1 Direction Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00F5H	P1dir	-	-	-	DR4	DR3	DR2	DR1	DR0	-	√

P1dir.n = 0: P1.n is configured as an input pin with pull-high resistor (50K). (Default)
1: P1.n is configured as an output pin.

※ Bit-manipulation instructions are not available on this register.

12.3 Port 2

Port 2

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00FCH	P2obuf	-	-	-	-	-	-	P21	P20	-	√

OSCI and OSCO could share with P2 by code option. Port 2 is a 2-bit open drain output with internal pull-high resistors. This register is used to buffer the out value of P2 and it is write-only. **The pull-high resistors will be temporarily disabled if the output value is low.**

※ Bit-manipulation instructions are not available on this register.

12.4 IR

IR_CTL

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00FAH	IR_CTL	IRO	IRPH	-	PS4	PS3	PS2	PS1	IR_SL	-	√
00FAH	IR_CTL	IRI	-	-	-	-	-	-	-	√	-

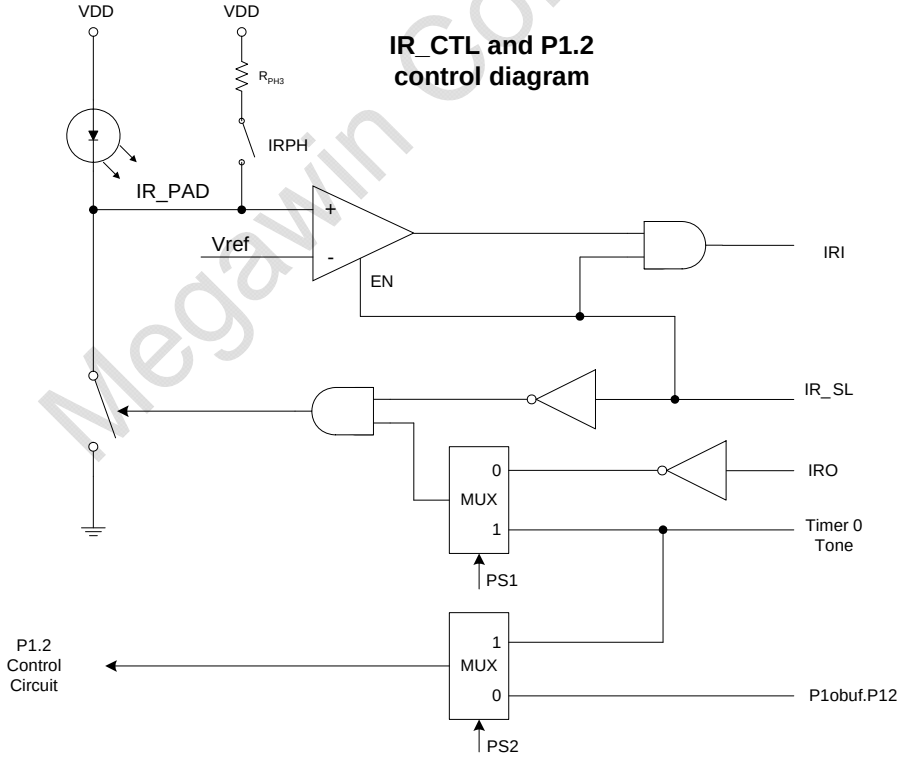
※ Bit-manipulation instructions are not available on this register.

IR_CTL is the IR pin input or output control register.

IR_SL: IR pin is input or output selector. 0: output mode, 1: input mode
PS1: IR pin output source selector. 0: /IRO, 1: timer0 tone output
PS2: P1.2 pin output source selector. 0: P1obuf.P12, 1: timer0 tone output
PS3: P1.3 pin output source selector (if P1dir.3=1). 0: P1obuf.P13, 1: PWM 0 output
PS4: P1.4 pin output source selector (if P1dir.4=1). 0: P1obuf.P14, 1: PWM 1 output

IRPH: IR_PAD pull-high control bit. 0: Disable internal pull-high, 1: Enable internal pull-high
IRO: The IR pin output status in output mode (IR_SL=0 and PS2 =0). The IR pin output status is the inverted value of IR_CTL.7. So, write "1" to bit7 of the IR_CTL.7 (IRO) the IR pin will output low voltage and write "0" to bit7 of the IR_CTL.7 (IRO) the IR pin will output high voltage.
IRI: In input mode (IR_SL=1), the IR pin will be a high sensitive input port. Reading IR_CTL.7 (IRI) would always read the logic value from pad.

IR_CTL and P1.2 control diagram



13 PWM

PWM0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00EEH	PWM0	PW07	PW06	PW05	PW04	PW03	PW02	PW01	PW00	√	√

The PWM clock source frequency is CPU clock source. P1.3/PWM pins produce 8-bit resolution PWM output. The PWM output duty is proportional to the code value of data buffer. Default is 1000 0000B

PWM1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00EFH	PWM1	PW17	PW16	PW15	PW14	PW13	PW12	PW11	PW10	√	√

The PWM clock source frequency is CPU clock source. P1.4/PWM pins produce 8-bit resolution PWM output. The PWM output duty is proportional to the code value of data buffer. Default is 1000 0000B

14 TK-SCAN

TK-scan Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00FBH	TKSCAN	CI3	CI2	CI1	CI0	SO3	SO2	SO1	SO0	√	-

MG69L331 built in low speed T type key-scan hardware. It can be used to scan keypad by hardware with less I/O pin counts than matrix type key-scan. This function only will be active automatically when this chip is setting into stop mode.

In stop mode, the P0.0~P0.7 and P1.0~P1.2 will output a low scan pulse in order. When a key is pressed, the MG69L331 will be woken up. The encoded scan key output code is stored in SO3~SO0, encoded scan key capture code is stored in CI3~CI0. Reading the SO3~SO0 and CI3~CI0 can decide which key is pressed. The TKSCAN SFR will be cleared by hardware reset.

The scan output mapping table is shown as below:

SO3~SO0 Output Code	Output Low I/O Pin
0000	P0.0
0001	P0.1
0010	P0.2
…	…
1001	P1.1
1010	P1.2

The capture input mapping table is shown as below:

CI3~CI0 Capture Code	Input Low I/O Pin
0000	P0.0
0001	P0.1
0010	P0.2
…	…
1001	P1.1
1010	P1.2

15 Option Register

Internal Oscillator Trimming Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00FEH	TRIM0	TR07	TR06	TR05	TR04	TR03	TR02	TR01	TR00	√	√

MG69L331 built in an 8MHz internal oscillator. It can be trimming by TRIM0 SFR.

TR03 ~ TR00: Fine tuning the value of internal oscillator.
TR07 ~ TR04: Coarse tuning the value of internal oscillator.

Mask Option

Item	1 / 0
WDT	Enable / Disable
P2 or OSC	Port 2 / Crystal
TK-SCAN	Enable / Disable

16 Programming Notice

The status after different reset condition is listed below:

	Power on reset	CPU /RES pin reset
SRAM Data	Unknown	Unchanged
CPU Register	Unknown	Unknown
Special Function Register	Default value	Default value

17 Application Circuit

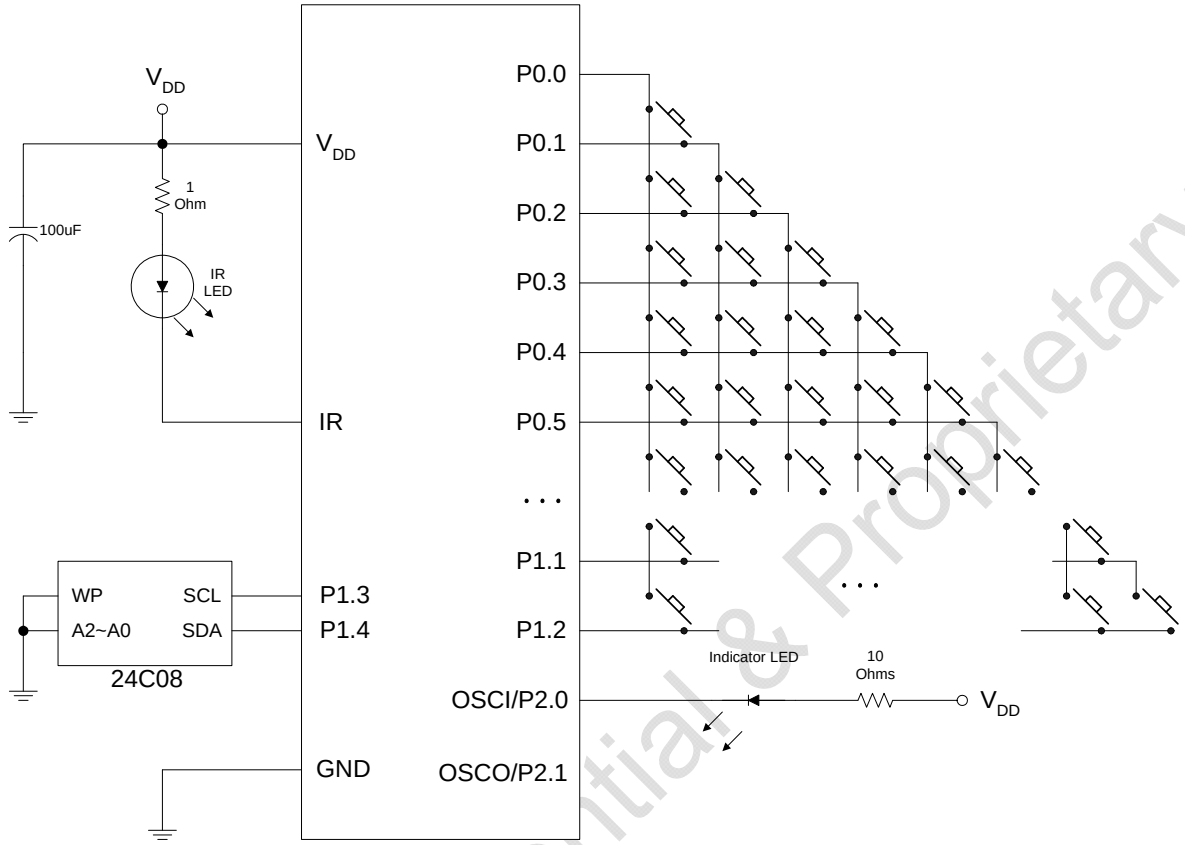


Figure 178-1 Application Circuit

18 Electrical Characteristics

18.1 Absolute Maximum Rating

PARAMETER	RATING	UNIT
Supply Voltage to Ground Potential	VSS-0.3 to VSS+4.0	V
Applied Input / Output Voltage	VSS-0.3 to VDD+0.3	V
Ambient Operating Temperature	0 to +70	°C
Storage Temperature	-50 to +125	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

18.2 DC Characteristics

(V_{DD}-V_{SS} = 3.0 V, F_{OSC} = 4MHz, Ta = 25° C; unless otherwise specified)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Op. Voltage	V_{DD}	-	1.8	-	3.6	V
Op. Current	I_{OP}	No load (Ext.-V) In normal operation	-	1.5	5	mA
Standby Current	I_{STB}	No load (Ext.-V)	-	1	3	μA
Input High Voltage	V_{IH}	-	0.7 V_{DD}	-	V_{DD}	V
Input Low Voltage	V_{IL}	-	0	-	0.3V_{DD}	V
Port 0, 1 Drive Current	I_{OH0}	V_{OH} = 2.4V, V_{DD} = 3.0V	-	5.0	-	mA
Port 0, 1, 2 Sink Current	I_{OL0}	V_{OL} = 0.4V, V_{DD} = 3.0V	-	10.0	-	mA
IRO Drive Current	I_{OH1}	V_{OH} = 2.7V, V_{DD} = 3.0V	10.0	-	-	mA
IRO Sink Current	I_{OL2}	V_{OL} = 1.0V, V_{DD} = 3.0V	250.0	-	-	mA
P0/P1/P2 Pull-high Resistor	R_{PH1}	V_{IL} = 0V	-	50K	-	Ω
IR Pull-high Resistor	R_{PH3}	V_{IL} = 0V	-	40K	-	Ω
/RES Pull-high Resistor	R_{RES}	V_{IL} = 0V	-	30K	-	Ω
Low Voltage Detector	V_{LVD}	V_{DD} > 2.3V	-	2.3	-	V
Low Voltage Reset	V_{LVR}	-	-	1.8	-	V

18.3 AC Characteristics

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CPU Op. Frequency	F_{CPU}	V_{DD} = 3.0V	0.4	4	8	MHz
System Start-Up Time	T_{SST}	Power-up, reset or wake-up from STOP mode	-	16384	-	1/ F_{CPU}
POR Duration	T_{POR}	F_{OSC} = 4 MHz	10	15	50	mS

19 Revision History

Revision	Page	Descriptions	Date
V0.1		MG69L331A original version	-
V1.06		Modify LVD & IR pull-high resistor spec.	-
V1.07		Non	2011/08/10
V2.0		Modify document format	2011/11/16