Version: 1.0

MG69L340

Data Sheet

8-Bit Micro-Controller with IR function

Version 1.0

Table of Contents

1 Features

- Single Chip 8-bit CPU
- Operation voltage: 1.8V to 3.6V
- Memory
  - Program ROM : 24K Bytes
  - Data RAM : 128 Bytes(shared with stack)
- 4 input with pull high resister, 4 input/output pins, 7 open-drain output pins with pull high resistor, 2 quasi input/output pins.
- 1 dedicated push pull output.
- Stop mode: micro-controller no operation.
  (Oscillators stop oscillating)
- Build-in 4MHz +/- 1.5% internal oscillator.
- Watchdog timer built-in
- One re-loadable 8-bit timer.
- Build-in low voltage detector (2.1V) and low voltage reset (typical voltage: below 1.8V).
- Oscillator (455K resonator or 3.58M/4M crystal) share with P2.0, P2.1 by code option.

Selection Information<<<

	MG69L340A
ROM (Program ROM)	24K x 8-bit (16K x 8-bit)
I/O	16/18

1.1 Application Field

General IR Controller, Toy

2 General Description

MG69L340A integrates an 8-bit CPU core, SRAM, timer and system control circuits by a CMOS silicon gate technology. The ROM can store data table and program.

Maximum seventeen I/O and one large sink output pin make this chip very suitable for IR application.

3 Pin Configurations

3.1 Pad Assignment

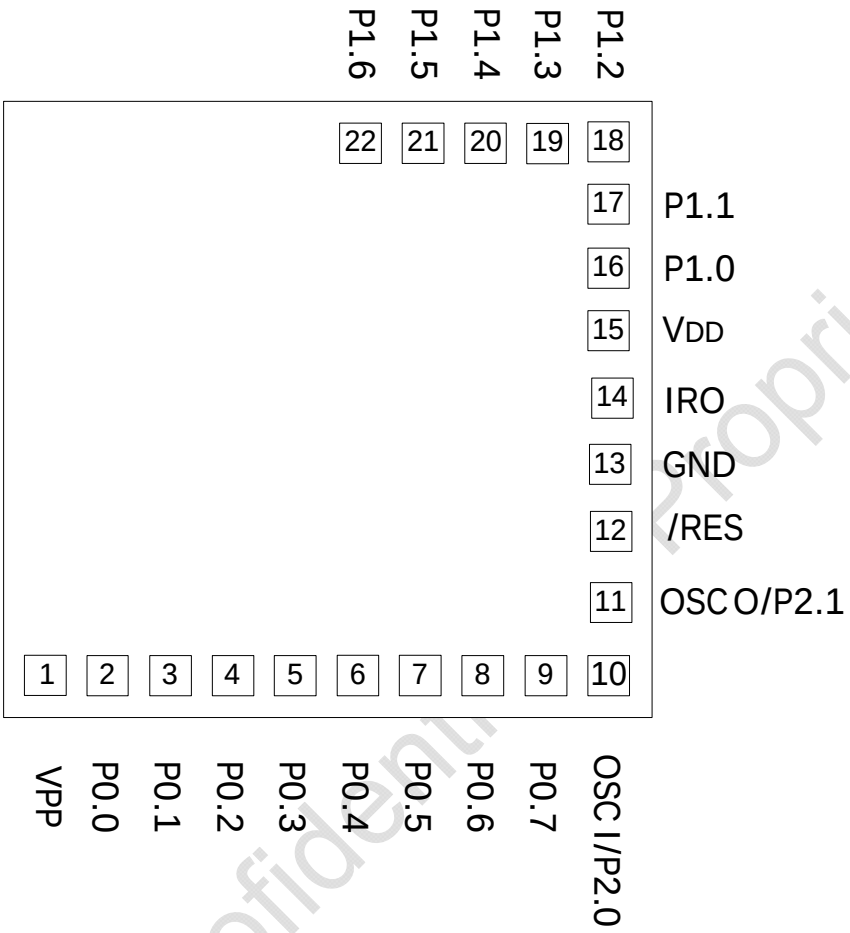


Figure 3-1 Pad Assignment

3.2 Pin Description

Table 3-1 Pin Description

Pad No.	Pad Name	I/O	Description
1	VPP	P	For system used only
15	VDD	P	Positive power pin
12	/RES	I	System reset pin (low active). Built in pull up 30K ohms.
13	GND	P	Ground pin
14	IRO	O	IRO output pin. Direct sink (sink current: 100mA) for IR LED. Default value is high after reset. The IRO output pin is inverting bit0 of IRO Buffer. So, write "1" to bit0 of the IRO buffer the IRO is output "0" and write "0" to bit0 of the IRO buffer the IRO is output "1".
10, 11	OSCI/P2.0, OSCO/P2.1	I/O, O	Resonator or crystal oscillator pins share with port 2. Port 2 is a quasi-bi-directional NMOS output pin with pull high (50K ohms). It is select by code option.
16 ~ 22	P1.0 ~ P1.6	O	Output pin with internal pull high (50K ohms).
2 ~ 5	P0.0 ~ P0.3	I	Input ports with internal pull high and interrupt function.
6 ~ 9	P0.4 ~ P0.7	I/O	Programmable I/O ports with interrupt function.

Note: In the "Type" field,
"I" means input only.
"O" means output only.
"B" means bi-direction.
"P" means Power, "G" means Ground.

4 Block Diagram

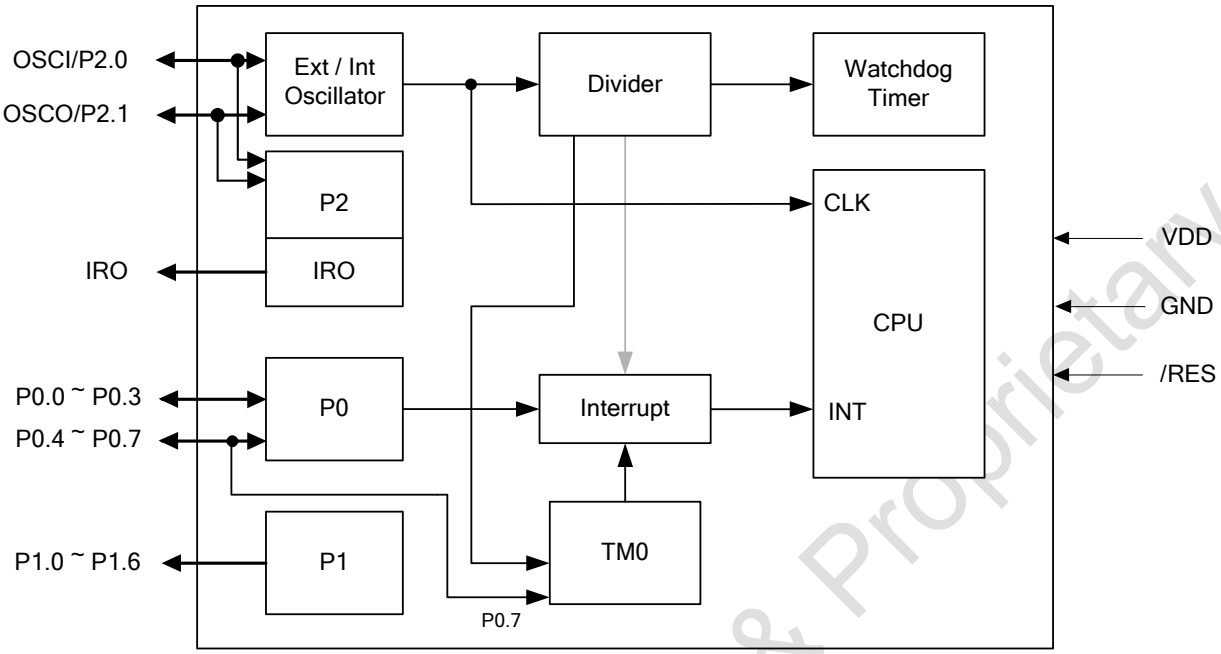


Figure 4-1 Block Diagram

5 Function Description

5.1 Registers

	A
	Y
	X
	P
PCH	PCL
1	S

5.2 Accumulator

The accumulator is a general-purpose 8-bit register, which stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of two data words used in these operations.

5.3 Index Register(X,Y)

There are two 8-bit index registers (X and Y), which may be used to count program steps or to provide an index value to be used in generating an effective address. When executing an instruction, which specifies indexed addressing, the CPU fetches the OP Code and the base address, and modifies the address by adding the index register to it prior to performing the desired operation. Pre- or post-index of index address is possible.

5.4 Processor Status Register

The 8-bit processor status register contains seven status flags. Some of the flags are controlled by the program, others may be controlled both the program and the CPU.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N	V	1	B	D	I	Z	C

N: Signed flag, 1 = negative, 0 = positive
V: Overflow flag, 1 = true, 0 = false
B: BRK interrupt command, 1 = BRK, 0 = IRQB
D: Decimal mode, 1 = true, 0 = false
I: IRQB disable flag, 1 = disable, 0 = enable
Z: Zero flag, 1 = true, 0 = false
C: Carry flag, 1 = true, 0 = false

5.5 Program Counter(PC)

The 16-bit program counter register provides the addresses, which step the micro-controller through sequential program instructions. Each time the micro-controller fetch an instruction from program memory, the lower byte of the program counter (PCL) is placed on the low-order 8 bits of the address bus and the higher byte of the program counter (PCH) is placed on the high-order 8 bits. The counter is incremented each time an instruction or data is fetched from program memory.

5.6 Stack Point(S)

The stack pointer is an 8-bit register, which is used to control the addressing of the variable-length stack. The stack pointer is automatically incremented and decremented under control of the micro-controller to perform stack manipulations under direction of either the program or interrupts (/NMI or /IRQ). The stack allows simple implementation of nested subroutines and multiple level interrupts. The stack pointer is initialized by the user's firmware.

6 Memory Organization

There are 128 bytes SRAM in MG69L340A. They are working RAM (0000H to 007FH) and stacks (0100H to 017FH). The stack area is shared with address 0000H to 007FH. The address 00E0H to 00FFH are special function registers area. Bit-manipulation instruction is available on SRAM except SFR.

There are 24K bytes program/data ROM in MG69L340A. The ROM address from A000H to FFFFH can store program and data. The address mapping of MG69L340A is shown as below.

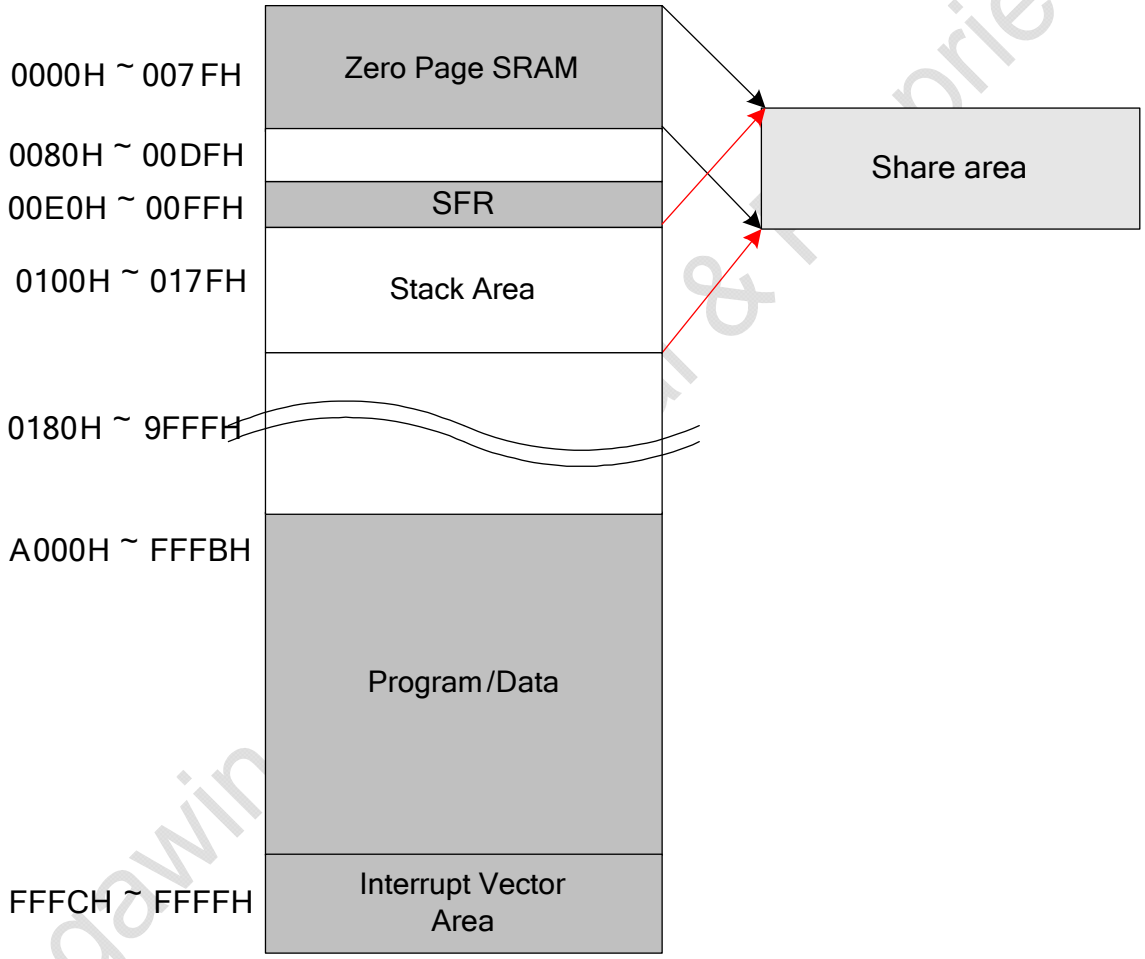


Figure 6-1 Memory Map

6.1 SFR Mapping

The address 00E0H to 00FFH are reserved for special function registers (SFR). The SFR is used to control or store the status of I/O, system clock and other peripheral.

※ All SFRs are not supported by bit-manipulation instructions.
※ Please initialize all the SFRs after power-on.

Table 6-1 SFR Table

SFR (special function register): 00E0H ~ 00FFH (page 0 area) <<<

Address	Content	Default	Address	Content	Default
00E0	MCLKmgr	---0---0	00F0	P0obuf	0000----
00E1		--------	00F1	P0pad	XXXXXXXX
00E2	IRQen	---00--0	00F2	P0dir	0000----
00E3	EVTflag & EVTclr (Hard_rst)	-X000--0	00F3	P0opd	0000----
00E4		--------	00F4	P0plh	0000----
00E5		--------	00F5	P1obuf	-0000000
00E6		--------	00F6		--------
00E7		--------	00F7		--------
00E8	TM0	11111111	00F8		--------
00E9	TM0_CTL	000---00	00F9	CWPR	--------
00EA		--------	00FA	IRO	0-------
00EB		--------	00FB		--------
00EC	EFS_CTL	0--0-000	00FC	P2obuf	------11
00ED		--------	00FD	P2pad	------XX
00EE		--------	00FE		--------
00EF	TRIM0	00000000	00FF		--------

6.2 Write Protect Function Register

Conditional Write Protect Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00F9H	CWPR	PT7	PT6	PT5	PT4	PT3	PT2	PT1	PT0	-	√

Conditional Write Protect Register (CWPR) is used to protect EVTclr.5 (WDTclr), MCLKmgr.0 (OSCen) and TRIM0 flags. If programmer wants to change the value of EVTclr.5 (WDTclr), MCLKmgr.0 (OSCen) or TRIM0, an “A6H” must write to CWPR firstly. *When CWPR is written by firmware, it would be cleared by hardware automatically after the “next write action” of firmware.*

PT7~PT0: Write protect pattern. The write protect pattern is “A6H” in MG69L340.

※ Bit-manipulation instructions are not available on this register.

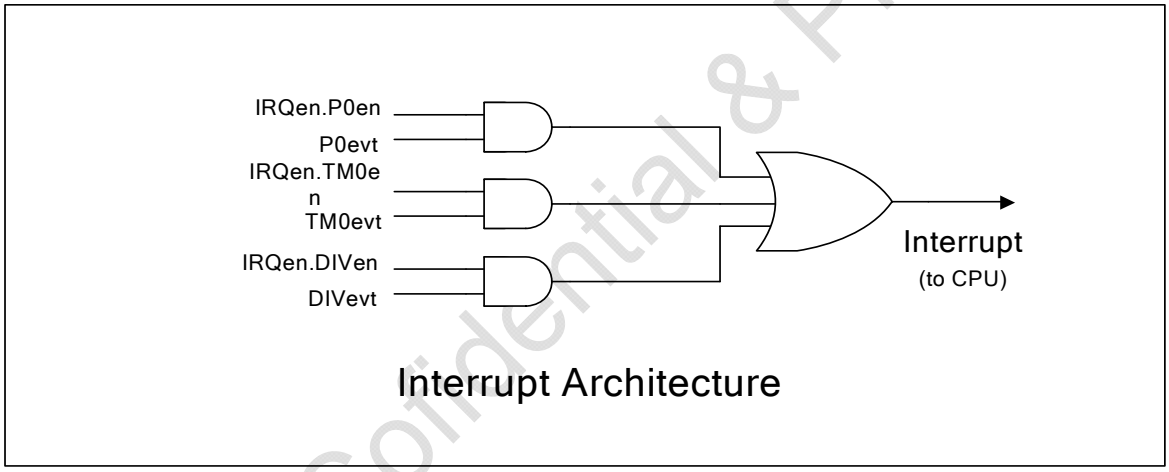
7 Interrupt

The MG69L340A provides 3 interrupt sources: port0, TM0 and divider. Each of the Interrupt sources can be individually enabled or disabled by setting or clearing the corresponding bit in the IRQen. Two interrupts share the interrupt vector FFFEH/FFFFH.

DIV interrupt: When IRQen.DIVen = 1 and DIVevt = 1.
P0 interrupt: When IRQen.P0en = 1 and P0evt = 1.
TM0 interrupt: IRQen.TM0en = 1 and TM0evt = 1.

Table 7-1 Interrupt Vector Table

Vector Address	Item	Flag	Properties	Memo
FFFCH, FFFDH	RESET	None	Ext.	Initial reset
"	WDT	WDTirq	Int.	Watch dog reset
"	LVR	None	Ext.	Low voltage reset
FFFEH, FFFFH	P0	P0irq	Ext.	Port P0 interrupt vector
"	DIV	DIVirq	Int.	Divider carry out interrupt
"	TM0	TM0irq	Int.	TM0 underflow interrupt



Interrupt Architecture

7.1 Interrupt Register

IRQ enable flag

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E2H	IRQen	-	-	-	DIVen	TM0en	-	-	P0en	-	√

Programmer can enable or disable the ability of triggering IRQ through this register.
0: Disable (default "0" at initialization)
1: Enable
P0en, Falling edge occurs at port 0 (input mode)
TM0en: Timer0 underflow occurred.
DIVen: DIV interrupts frequency occurred

IRQ status flag

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E3H	EVTflag	-	LVD	WDT	DIV	TM0	-	-	P0	√	-

When IRQ occurs, programmer can read this register to know which source triggering IRQ.

P0:P0 interrupt flag. Set by falling edge on any pin of port0. Clear by software.
DIV: Divider interrupts flag. Clear by software.
WDT: WDT time-out flag. Clear flag and WDT counter by software.
TM0: Timer0 underflow flag and the flag clear by software.

LVD: Low voltage detected. 1:VDD is under 2.1V. 0:VDD is above 2.1V. It is set by hardware and read only.

IRQ clear flag

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E3H	EVTclr	-	-	WDT	DIV	TM0	-	-	P0	-	√

Programmer can clear the interrupt event by writing '0' into the corresponding bit.
WDTclr is protected by CWPR.

7.2 Interrupt System

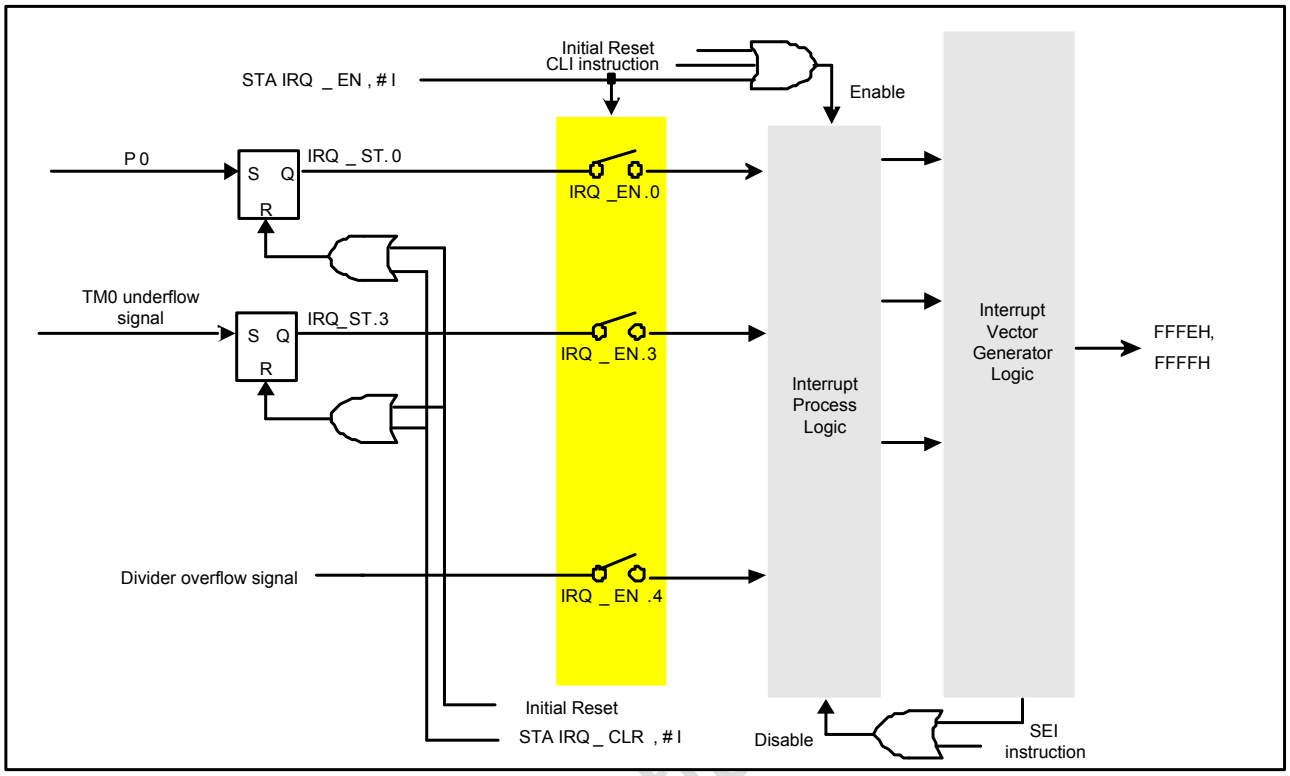


Figure 7-1 Interrupt System Diagram

8 Reset

8.1 Low Voltage Reset (LVR)

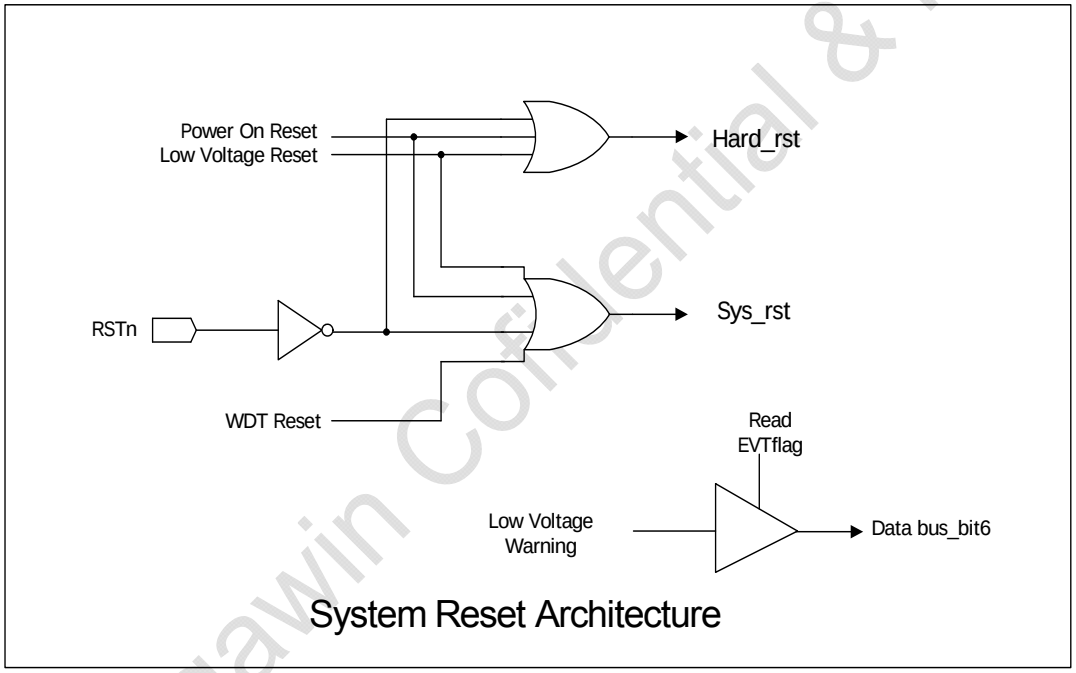
The MG69L340A provides low voltage reset circuit in order to monitor the supply voltage of the device. If the supply voltage of the device is within the range 0.9V ~ V_{LVR} , such as changing a battery, the LVR will automatically reset the device internally.

The LVR includes the following specifications:

1. The low voltage (0.9V~V_{LVR}) has to remain in their original state to exceed 1ms. If the low voltage state does not exceed 1ms, the LVR will ignore it and do not perform a reset function.
2. In the LVR mode, the on-chip oscillator is stopped and the on-chip SRAM is held. Port0 and port2 set to input mode (pull-high disable) and IRO, port1 is output floating.

8.2 Low Voltage Detector

The low voltage Detector (2.1V) has no de-bounce ability. When V_{DD} is equal or lower than LVD, the LVD flag to be set high immediately. De-bounce should be implemented by software.



System Reset Architecture

8.3 Watchdog Timer (WDT)

(The example is base on 4MHz) unit: Hz

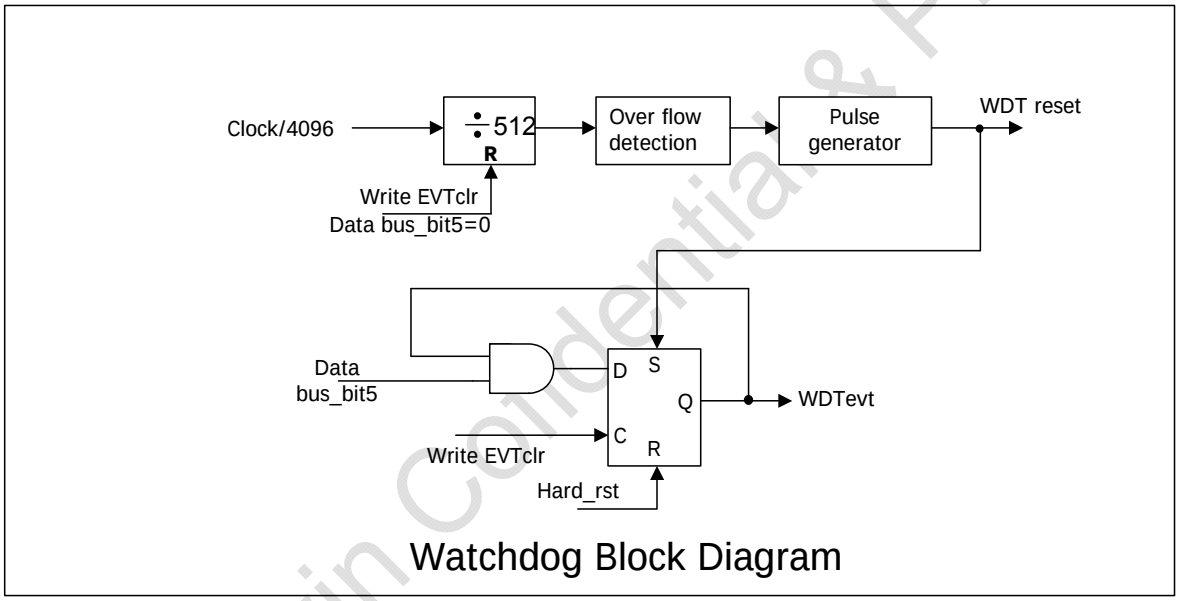
Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
WDThigh	-	-	-	-	-	-	-	1.9	-	-

The watchdog timer time-out period is obtained by the equation: (F_{OSC} / 4096)/512

Before watchdog timer time-out occurs, the program must write A6H to CWPR then clear the 9-bit WDT timer by writing 0 to EVTclr.5 at next write OP code. The WDT register contents will be reset by hardware reset, low voltage reset and power-on reset.

Example:

```
clear_WDT .macro
          sei
          lda   #A6H
          sta   CWPR          ;;(F9h)
          lda   #DFH
          sta   EVTclr        ;;(E3h)
          cli
.endm
```



Watchdog Block Diagram

8.4 Reset OK

Main Clock Manager<<<

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E0H	MCLKmgr	ROK	-	-	DIVsel	-	-	-	OSCen	-	√

ROK (Reset OK): If the device reset OK and work well, must write any value into this bit.
For example:

```
Program_start: STZ $E0
```

9 Power Control

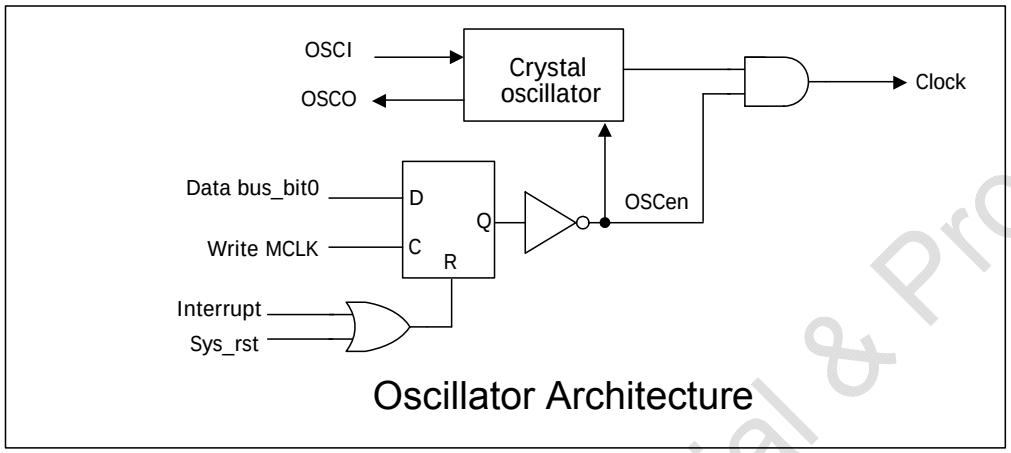
9.1 Power Control Register

Main Clock Manager<<<

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E0H	MCLKmgr	ROK	-	-	DIVsel	-	-	-	OSCen	-	√

OSCen: 0:The oscillator is free run. 1:The oscillator is frozen. OSCen is protected by CWPR.

The uC can be awakened by 3-ways: port 0 interrupt, hardware reset, or power-on reset.



Oscillator Architecture

DIVsel: Divider interrupt frequency selector
0: The Fosc/4096 interrupt frequency is selected
1: The Fosc/256 interrupt frequency is selected

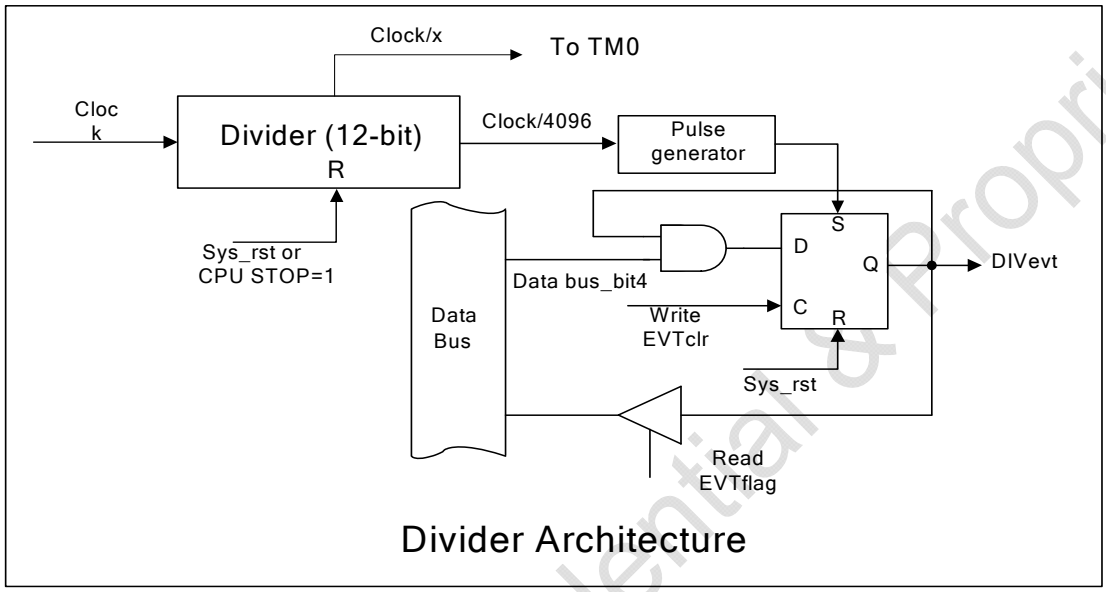
10 Divider

10.1 Divider

Divider (The example is base on 3. 579545MHz) Unit: Hz

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
DIVlow	13984	227968	55937	111875	223750	447500	895000	1790000	-	-
DIVhigh					874	1748	3496	6992		

The time-out period is obtained by the equation: 4096/OSC.
The DIV flag will be set when 4096/OSC or 256 /OSC (selected by DIVsel) is met.



Divider Architecture

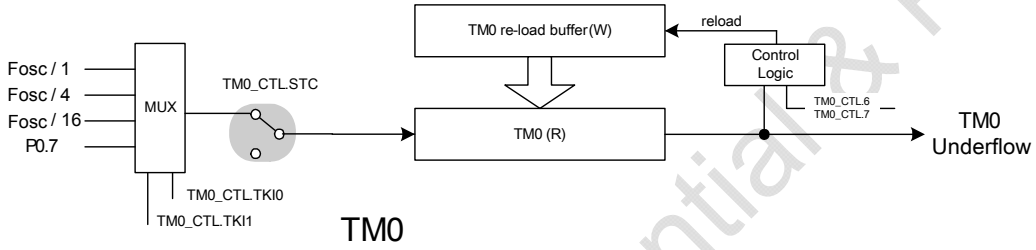
11 Timer

11.1 Timer0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E8H	TM0	T7	T6	T5	T4	T3	T2	T1	T0	-	√
00E9H	TM0_CTL	STC	RL/S	TKES	-	-	-	TKI1	TKI0	-	√

STC: Start/Stop counting. 1: start and pre-load the value to counter, 0: stop timer clock (set this bit to 1 will be ignored when this bit already set to 1)
RL/S: Auto-reload disable/enable. 1: disable auto-reload, 0: enable auto-reload
TKES: Event or series input clock-in trigger edge selector; 0: rising edge, 1: falling edge

TKI1	TKI0	Selected TM0 input clock source
0	0	Fosc / 1
0	1	Fosc / 4
1	0	Fosc / 16
1	1	P0.7



12 Configurable I/O Ports

12.1 Port 0

Port 0 Pad

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00F1H	P0pad	P07	P06	P05	P04	P03	P02	P01	P00	√	-

Port 0 is combined with 4-bit input port and 4-bit I/O port. P0.4~P0.7 can be programmed as input or output individually. When P0.n is configured as an output pin, the P0.n pin would output the logic content of P0obuf.n.

When the P0.n is configured as output mode, reading P0pad.n would always read logic '0'.
When the P0.n is configured as input mode, reading P0pad.n would always read the logic value from pad.

※ Bit-manipulation instructions are not available on this register.

Port 0 Output Buffer

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00F0H	P0obuf	P07	P06	P05	P04	-	-	-	-	-	√

This register is used to buffer the output value of P0.4 ~ P0.7 and it is write-only.

※ Bit-manipulation instructions are not available on this register.

Port 0 Direction Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00F2H	P0dir	DR7	DR6	DR5	DR4	-	-	-	-	-	√

P0dir.n = 0: P0.n is configured as an input pin. (Default)
1: P0.n is configured as an output pin.

※ Bit-manipulation instructions are not available on this register.

Port 0 Pull-high Control Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00F4H	P0plh	PH7	PH6	PH5	PH4	-	-	-	-	-	√

0: Disable internal pull-high, 1: Enable internal pull-high

PH0 ~ PH3: Pull-high is always enabled.
PH4 ~ PH7: These control bits are used to enable the pull-high of P0.4 ~ P0.7 pin.
Note: When P0.n is configured as an output pin, the pull high will be disabled.

※ Bit-manipulation instructions are not available on this register.

Port 0 Open-Drain Control Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00F3H	P0opd	OD7	OD6	OD5	OD4	-	-	-	-	-	√

0: Disable open-drain output (CMOS output), 1: Enable open-drain output

OD4 ~ OD7: These control bits are used to enable the open-drain of P0.4 ~ P0.7 pin.

※ Bit-manipulation instructions are not available on this register.

12.2 Port 1

Port 1 Output Buffer

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00F5H	P1obuf	-	P16	P15	P14	P13	P12	P11	P10	-	√

Port 1 is a 7-bit output port with internal pull-high resistors. This register is used to buffer the output value of P1.0 ~ P1.6 and it is write-only. **The pull-high resistors will be temporarily disable if the output value is low.**

※ Bit-manipulation instructions are not available on this register.

12.3 Port 2

Port 2 Pad

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00FDH	P2pad	-	-	-	-	-	-	P21	P20	√	-

When P2 is used as an input, the corresponding bit of P2obuf must be 1. In this condition, the corresponding pin is pulled to high by the internal pull-high resistor and it can be pulled to low by an external source. Reading P2pad.n would always read the logic value from pad.

※ Bit-manipulation instructions are not available on this register.

Port 2 Output Buffer

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00FCH	P2obuf	-	-	-	-	-	-	P21	P20	-	√

OSCI and OSCO could share with P2 by code option. Port 2 is a 2-bit quasi-bi-directional open drain output port with internal pull-high resistors. This register is used to buffer the out value of P2 and it is write-only. **The pull-high resistors will be temporarily disable if the output value is low.**

※ Bit-manipulation instructions are not available on this register.

12.4 IRO

IR Output Buffer

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00FAH	IRO	IR	-	-	-	-	-	-	-	-	√

Note: The IRO pin output status is the inverted value of IRO.7. So, write “1” to bit7 of the IRO buffer the IRO will output low voltage and write “0” to bit7 of the IR buffer the IRO will output high voltage.

13 Option Register

E-fuse control register <<<

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00ECH	EFS_CTL	WR	-	-	DIN	-	ADR2	ADR1	ADR0	-	√

WR: direct control E-fuse “WR” signal
DIN: direct control E-fuse “DIN” signal
ADR2 ~ ADR0: direct control E-fuse “ADR2 ~ ADR0” signals.
※ Bit-manipulation instructions are not available on this register.

Internal Oscillator Trimming Register <<<

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00EFH	TRIM0	TR07	TR06	TR05	TR04	TR03	TR02	TR01	TR00	√	√

MG69L340 build in a 4MHz internal RC oscillator. It can be trimming by TRIM0 SFR. TRIM0 is protected by CWPR.

TR03 ~ TR00: Fine tuning the value of internal oscillator.
TR07 ~ TR04: Coarse tuning the value of internal oscillator.

Mask Option

Item	selection
WDT	Enable / Disable
P2 or OSC	Port 2 / Crystal

14 Programming Notice

The status after different reset condition is listed below:

Item	Power on reset	CPU /RES pin reset
SRAM Data	Unknown	Unchanged
CPU Register	Unknown	Unknown
Special Function Register	Default value	Default value

15 Application Circuit

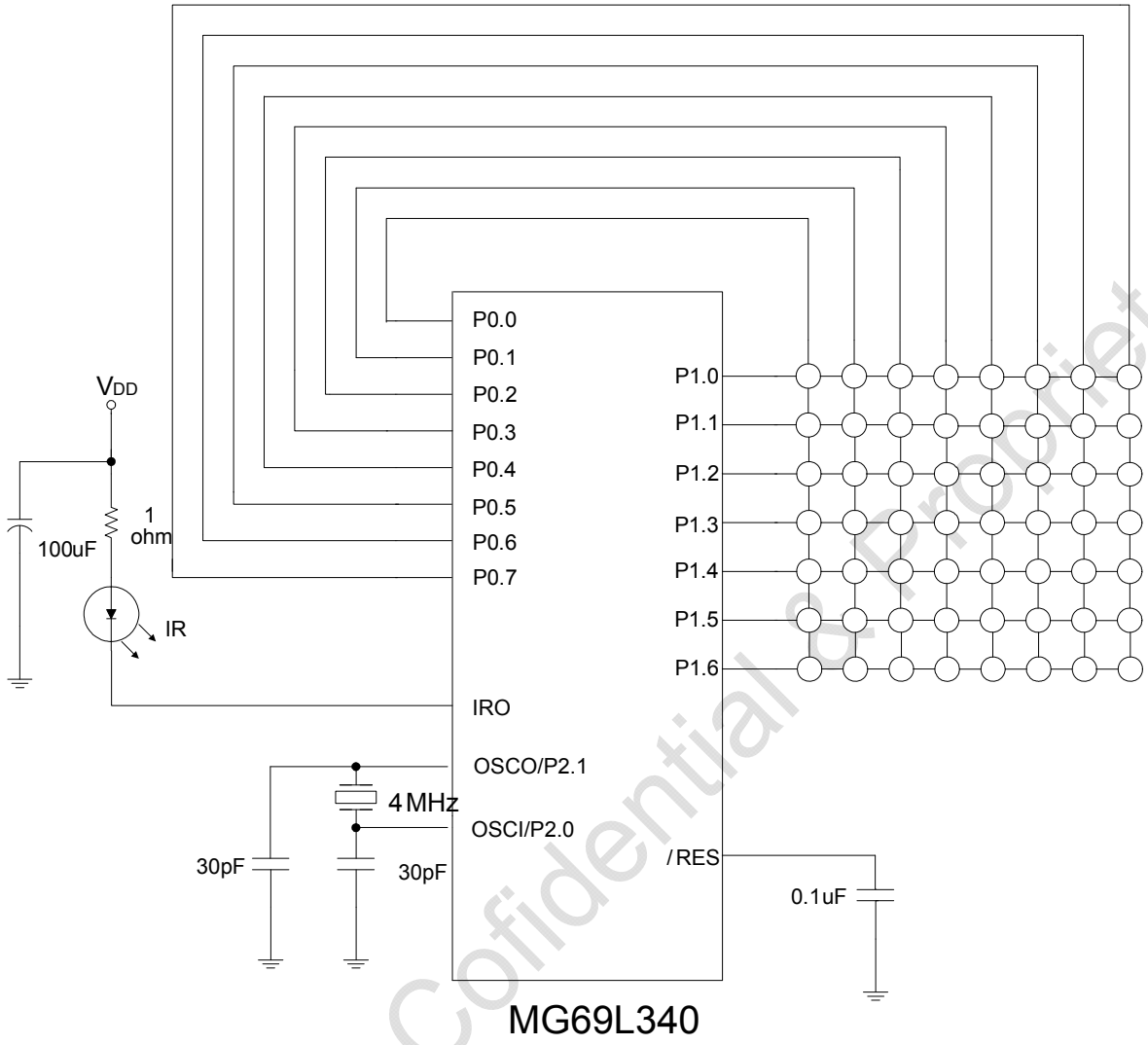


Figure 15-1 Application Circuit - LCD Remote Controller

16 Electrical Characteristics

16.1 Absolute Maximum Rating

PARAMETER	RATING	UNIT
Supply Voltage to Ground Potential	VSS-0.3 to VSS+4.0	V
Applied Input / Output Voltage	VSS-0.3 to VDD+0.3	V
Ambient Operating Temperature	0 to +70	°C
Storage Temperature	-50 to +125	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

16.2 DC Characteristics

(VDD-VSS = 3.0 V, FOSC = 4MHz, Ta = 25° C; unless otherwise specified)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Op. Voltage	V_{DD}	-	1.8	-	3.6	V
Op. Current	I_{OP}	No load (Ext.-V) In normal operation	-	1.3	5	mA
Standby Current	I_{STB1}	No load (Ext.-V)	-	1	3	μA
Key-scan Standby Current	I_{STB2}	No load (Ext.-V)	-	2	4	μA
Input High Voltage	V_{IH}	-	0.7 V_{DD}	-	V_{DD}	V
Input Low Voltage	V_{IL}	-	0	-	0.3V_{DD}	V
Port 0.4~0.7 Drive Current	I_{OH0}	V_{OH} = 2.7V, V_{DD} = 3.0V	-	2.0	-	mA
Port 0.4~0.7, Port 1.0~1.4, P2.0 Sink Current	I_{OL0}	V_{OL} = 0.4V, V_{DD} = 3.0V	-	3.0	-	mA
Port 1.5, 1.6 Sink Current	I_{OL1}	V_{OL} = 0.4V, V_{DD} = 3.0V	-	9.0	-	mA
IRO Drive Current	$I_{OH\ 2}$	V_{OH} = 2.7V, V_{DD} = 3.0V	10.0	-	-	mA
IRO Sink Current	$I_{OL\ 2}$	V_{OL} = 1.0V, V_{DD} = 3.0V	250.0	-	-	mA
P0, P1, P2 Pull-high Resistor	R_{PH}	V_{IL} = 0V	-	50K	-	Ω
/RES Pull-high Resistor	R_{RES}	V_{IL} = 0V	-	30K	-	Ω
Low Voltage Detector	V_{LVD}	V_{DD} > 2.1V	-	2.1	-	V
Low Voltage Reset	V_{LVR}	-	-	1.8	-	V

16.3 AC Characteristics

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CPU Op. Frequency	F_{CPU}	V_{DD} = 3.0V	0.4	4	8	MHz
Internal Oscillator Variation	ΔF_{OSC}	V_{DD} = 2.1V ~ 3.6V, T_a = -20° C ~ +50° C	-1.5	0	1.5	%
System Start-Up Time	T_{SST}	Power-up, reset or wake-up from STOP mode	-	32768	-	1/ F_{CPU}
POR Duration	T_{POR}	F_{OSC} = 4 MHz	10	15	50	mS

17 Revision History

Revision	Page	Descriptions	Date
V0.1		MG69L340A original version.	
V0.2		Modify the port 2 pin sequential and some typing mistakes.	
V0.3		Delete P2.0, IFSen and add trimming registers.	
V0.4		Modify EFS_CTL and TRIM0 address.	2011/01/10
V1.0		Modify document format.	2011/11/17

All change will be marked with "**<<<**"