Version: 1.00

MG69L355

Data Sheet

8-Bit Micro-Controller with IR function

Version 1.00

Table of Contents

1 Features

- Single Chip 8-bit CPU
- Memory
  - ROM : 96K Bytes
  - Data RAM : 256 Bytes (shared with stack)
- Operating voltage: 1.8V to 3.6V
- I/O pins:
  - 8 inputs with pull high resister
  - 4 open-drain output pins with pull high resistor selection
  - 4 output pins with NMOS/CMOS and pull high resistor selection
  - 7 quasi-bi-directional NMOS output pins with pull high resistor
  - 1 dedicated push pull I/O combined with IR amplifier input
- Two re-loadable 8-bit timers with capture function
- One re-loadable 16-bit timer
- Watchdog timer built-in
- Build-in low voltage detector (2.1V) and low voltage reset (typical voltage: below 1.8V)
- Stop mode: micro-controller no operation (Oscillators stop oscillating)
- Oscillator (455K resonator or 3.58M/4M crystal)

Selection Information

	MG69L355
ROM (Program ROM)	96K x 8-bit (32K x 8-bit)
I/O	24

1.1 Application Field

Toy controller, General IR controller

2 General Description

MG69L355 integrates an 8-bit CPU core, SRAM, timer and system control circuits by a CMOS silicon gate technology. The ROM can store data table and program.

Twenty-three I/O and one large sink output pin make this chip very suitable for IR application.

3 Pin Configurations

3.1 Pad Assignment

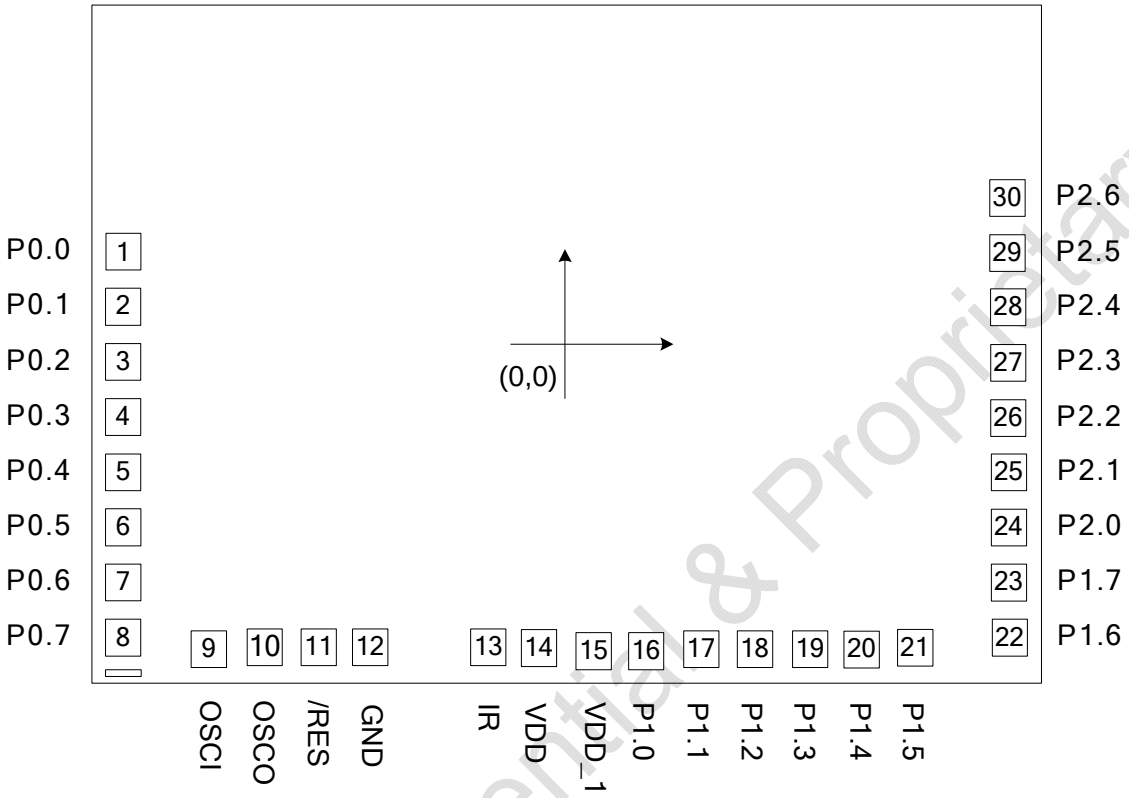


Figure 3-1 Pad Assignment

3.2 Pin Description

Table 3-1 Pin Description

Pad No.	Pad Name	I/O	Description
10, 9	OSCO, OSCI	O, I	Resonator or crystal oscillator pins
14,15	VDD, VDD_1	P	Positive power pins
11	/RES	I	System reset pin (low active). Built in pull up 10K ohms.
12	GND	P	Ground pin
13	IR	I/O	IR input/output pin. Direct sink (sink current: 100mA) for IR LED. Default value is high after reset. The IR output pin is inverting bit7 of IR_CTL Buffer. So, write “1” to bit7 of the IR_CTL buffer the IR is output “0” and write “0” to bit7 of the IR_CTL buffer the IR is output “1”.
1 ~ 8	P0.0 ~ P0.7	I	Input ports with internal pull high and interrupt function.
16 ~ 23	P1.0 ~ P1.7	O	P1.0 ~ P1.3 output pins with open drain and pull high resistor selection. P1.4~P1.7 output pins with NMOS/CMOS and pull high resistor selectable.
24 ~ 30	P2.0 ~ P2.6	O	Quasi-bi-directional NMOS output pins with pull high

Note: In the “Type” field,
“I” means input only.
“O” means output only.
“B” means bi-direction.
“P” means Power, “G” means Ground.

4 Block Diagram

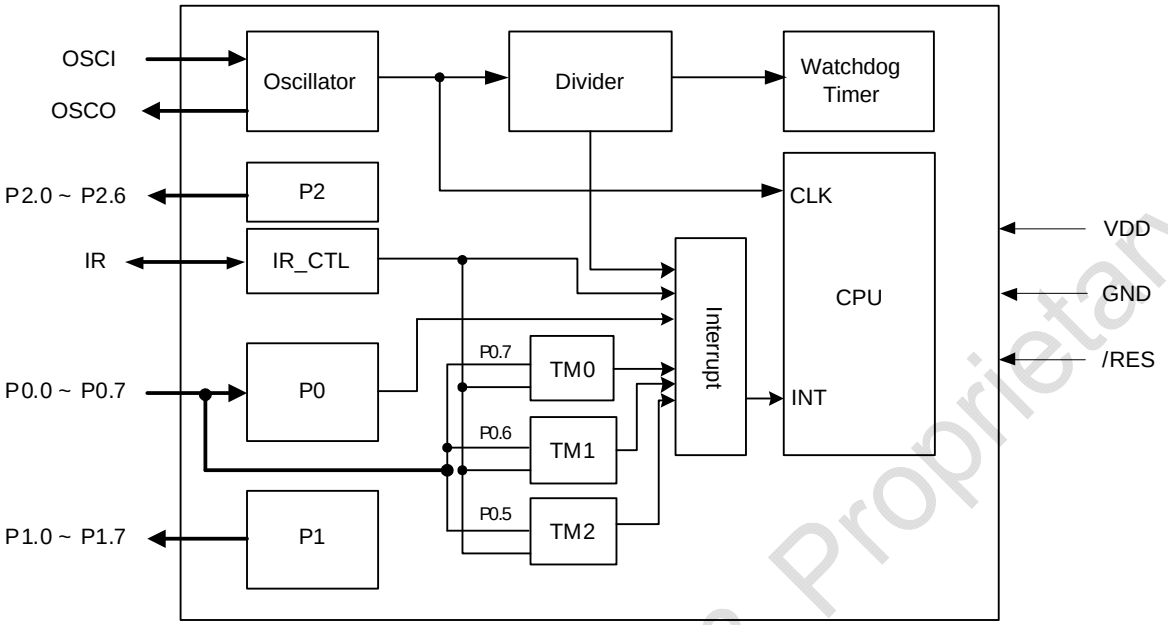


Figure 4-1 Block Diagram

5 Function Description

5.1 Registers

	A
	Y
	X
	P
PCH	PCL
1	S

5.2 Accumulator

The accumulator is a general-purpose 8-bit register, which stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of two data words used in these operations.

5.3 Index Register(X,Y)

There are two 8-bit index registers (X and Y), which may be used to count program steps or to provide an index value to be used in generating an effective address. When executing an instruction, which specifies indexed addressing, the CPU fetches the OP Code and the base address, and modifies the address by adding the index register to it prior to performing the desired operation. Pre- or post-index of index address is possible.

5.4 Processor Status Register

The 8-bit processor status register contains seven status flags. Some of the flags are controlled by the program, others may be controlled both the program and the CPU.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N	V	1	B	D	I	Z	C

N: Signed flag, 1 = negative, 0 = positive
V: Overflow flag, 1 = true, 0 = false
B: BRK interrupt command, 1 = BRK, 0 = IRQB
D: Decimal mode, 1 = true, 0 = false
I: IRQB disable flag, 1 = disable, 0 = enable
Z: Zero flag, 1 = true, 0 = false
C: Carry flag, 1 = true, 0 = false

5.5 Program Counter(PC)

The 16-bit program counter register provides the addresses, which step the micro-controller through sequential program instructions. Each time the micro-controller fetch an instruction from program memory, the lower byte of the program counter (PCL) is placed on the low-order 8 bits of the address bus and the higher byte of the program counter (PCH) is placed on the high-order 8 bits. The counter is incremented each time an instruction or data is fetched from program memory.

5.6 Stack Point(S)

The stack pointer is an 8-bit register, which is used to control the addressing of the variable-length stack. The stack pointer is automatically incremented and decremented under control of the micro-controller to perform stack manipulations under direction of either the program or interrupts (/NMI or /IRQ). The stack allows simple implementation of nested subroutines and multiple level interrupts. The stack pointer is initialized by the user's firmware.

6 Memory Organization

There are 256 bytes SRAM in MG69L355. They are working RAM (0000H to 00BFH) and stacks (01C0H to 01FFH). The address 0100H to 1BFH are shared with address 0000H to 00BFH. The address 00C0H to 00FFH is special function registers area. Bit-manipulation instruction is available on SRAM except SFR.

There are 96K bytes program/data ROM in MG69L355. It is combined with 32K program/data ROM and bank switching data ROM. The ROM address from 8000H to FFFFH can store program and other data. There are four banks in MG69L355 that is index by SFR. The default bank number is 00H after power on or reset. The bank select function, ranged from 4000H to 7FFFH (16Kbyte/bank), is used for extending memories if the ROM size is more than 32K bytes in MG69L355. The address mapping of MG69L355 is shown as below.

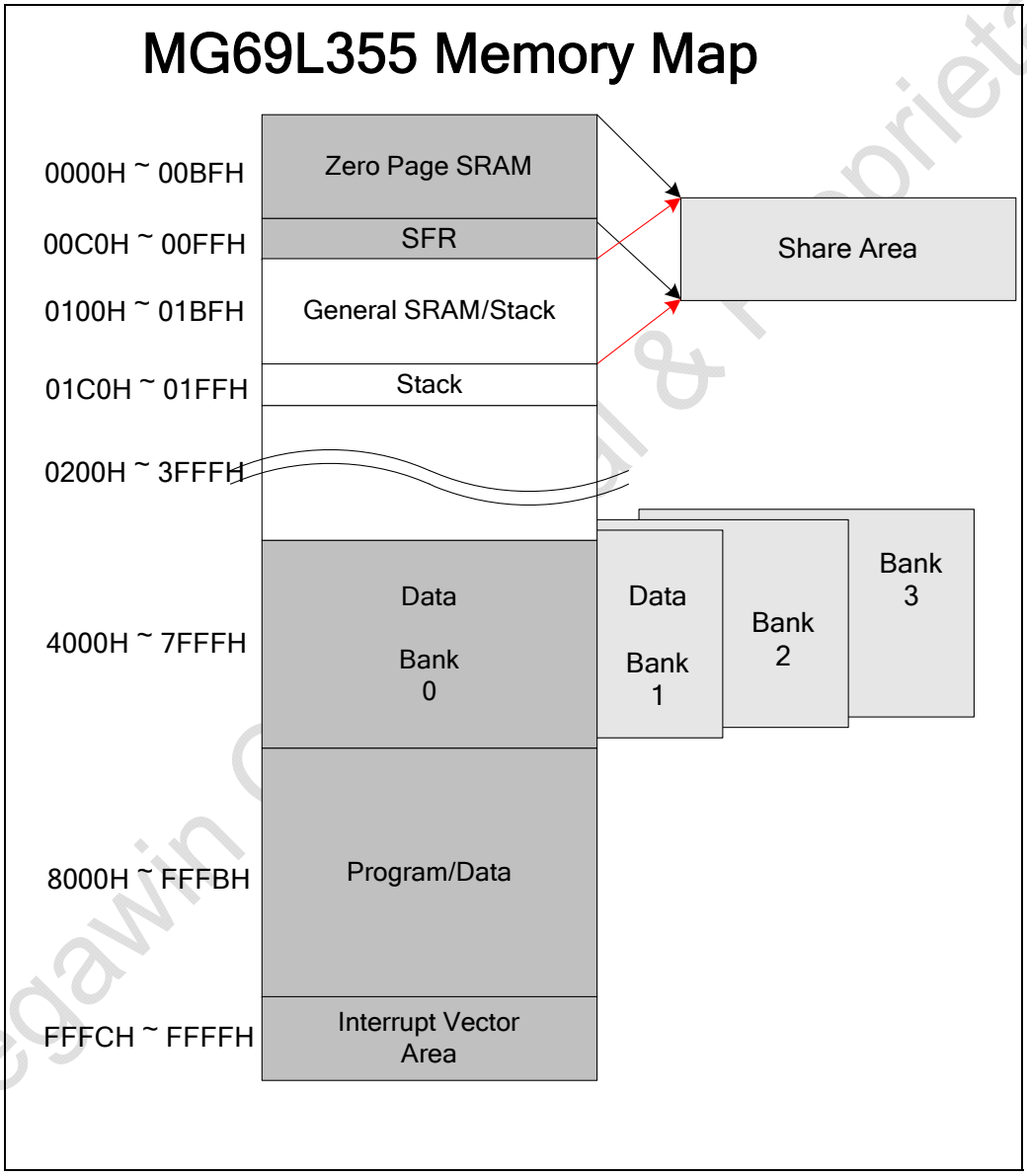


Figure 6-1 Memory Map

6.1 SFR Mapping

The address 00E0H to 00FFH are reserved for special function registers (SFR). The SFR is used to control or store the status of I/O, system clock and other peripheral.

※ All SFRs are not supported by bit-manipulation instructions.

Table 6-1 SFR Table

SFR (special function register): 00C0H~00FFH

Address	Content	Default	Address	Content	Default
00E0	MCLKmgr	---0---0	00F0	BANK	------00
00E1	RESOK	--------	00F1	P0pad	XXXXXXXX
00E2	IRQen	0--00000	00F2		--------
00E3	EVTflag & EVTclr (Hard_rst)	0X000000	00F3		--------
00E4		--------	00F4		--------
00E5	TM2L	11111111	00F5	P1obuf	11111111
00E6	TM2H	11111111	00F6	P1opd	1111----
00E7	TM2_CTL	000---00	00F7	P1plh	00000000
00E8	TM0	11111111	00F8		--------
00E9	TM0_CTL	00000-00	00F9		--------
00EA	TM0_CAP	00000000	00FA	IR_CTL	0------0
00EB	TM0_CAP_C	11111111	00FB		--------
00EC	TM1	11111111	00FC	P2	-1111111
00ED	TM1_CTL	00000-00	00FD		--------
00EE	TM1_CAP	00000000	00FE		--------
00EF	TM1_CAP_C	11111111	00FF		--------

6.2 System Control Registers

Bank select

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00F0H	BANK	-	-	-	-	-	-	BK1	BK0	√	√

Program can switch the memory bank through this register. This register in initialized to 00H after power on reset. For more detailed information, please refer to memory map description.

BANK0 ➔ BK1=0, BK0=0
BANK1 ➔ BK1=0, BK0=1
BANK2 ➔ BK1=1, BK0=0
BANK3 ➔ BK1=1, BK0=1

7 Interrupt

The MG69L355 provides 6 interrupt sources: port0, Timer0, Timer1, Timer2, IRI (IR pin configured as input mode) and divider. Each of the Interrupt sources can be individually enabled or disabled by setting or clearing a bit in the IRQen. Six interrupts share the interrupt vector FFFEH/FFFFH.
DIV interrupt: IRQen.4 (DIVen) = 1 and DIVevt = 1.
P0 interrupt: IRQen.0 (P0en) = 1 and P0evt = 1.
TM2 interrupt IRQen.1 (TM2en) = 1 and TM2evt = 1.
TM1 interrupt IRQen.2 (TM1en) = 1 and TM1evt = 1.
TM0 interrupt IRQen.3 (TM0en) = 1 and TM0evt = 1.
IRI interrupt IRQen.7 (IRIen) =1 and IRIevt =1

Table 7-1 Interrupt Vector Table

Vector Address	Item	Flag	Properties	Memo
FFFCH, FFFDH	RESET	None	Ext.	Initial reset
"	WDT	WDTirq	Int.	Watchdog reset
"	LVR	None	Ext.	Low voltage reset
FFFEH, FFFFH	P0	P0irq	Ext.	Port P0 interrupt vector
"	DIV	DIVirq	Int.	Divider carry out interrupt
"	TM0	TM0irq	Int.	TM0 underflow interrupt
"	TM1	TM1irq	Int.	TM1 underflow interrupt
"	TM2	TM2irq	Int.	TM2 underflow interrupt
"	IRI	IRIirq	Ext.	IR input interrupt vector

7.1 Interrupt Register

IRQ enable flag

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E2H	IRQen	IRIen	-	-	DIVen	TM0en	TM1en	TM2en	P0en	-	√

Program can enable or disable the ability of triggering IRQ through this register.
0: Disable (default "0" at initialization)
1: Enable
P0en: Falling edge occurs at port 0 (input mode)
TM0en: Timer 0 underflow occurred.
TM1en: Timer 1 underflow occurred.
TM2en: Timer 2 underflow occurred.
DIVen: DIV interrupt frequency occurred
IRIen: edge occurs at IR pin (input mode)

IRQ status flag

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E3H	EVTflag	IRI	LVD	WDT	DIV	TM0	TM1	TM2	P0	√	-

When IRQ occurs, program can read this register to know which source triggering IRQ.
P0:P0 interrupt flag. Set by falling edge on any pin of port0. Clear by software.
DIV: Divider interrupts flag. Clear by software.
WDT: WDT time-out flag. Clear flag and WDT counter by software.
TM0: Timer 0 underflow flag and the flag clear by software.
TM1: Timer 1 underflow flag and the flag clear by software.
TM2: Timer 2 underflow flag and the flag clear by software.
LVD: Low voltage detected. 1:VDD is under 2.1V. 0:VDD is above 2.1V. It is set by hardware and read only.
IRI:IRI interrupt flag. Set by falling or rising edge on IR pin (input mode). Clear by software.

IRQ clear flag

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E3H	EVTclr	IRI	-	WDT	DIV	TM0	TM1	TM2	P0	-	√

Program can clear the interrupt event by writing '0' into the corresponding bit.

7.2 Interrupt System

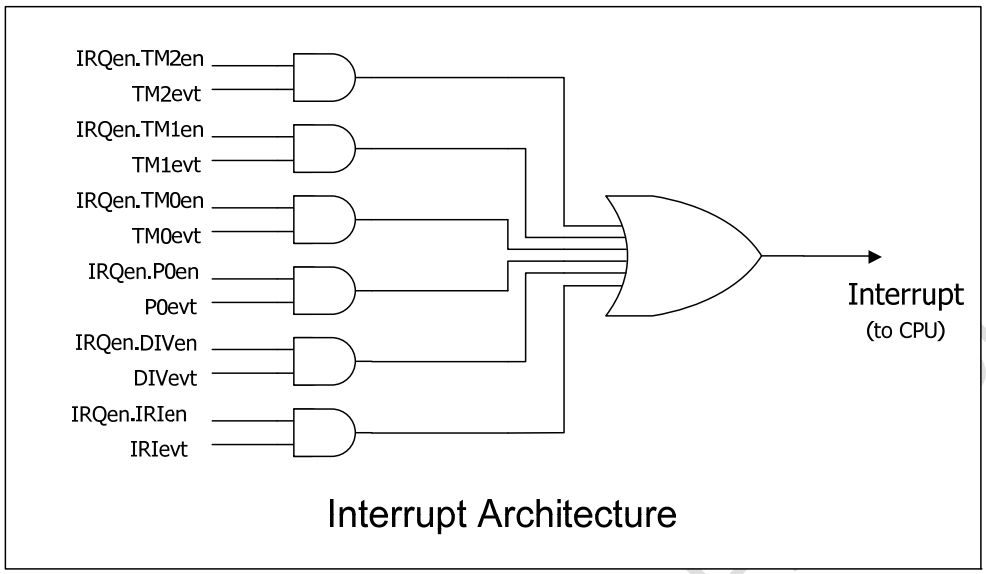
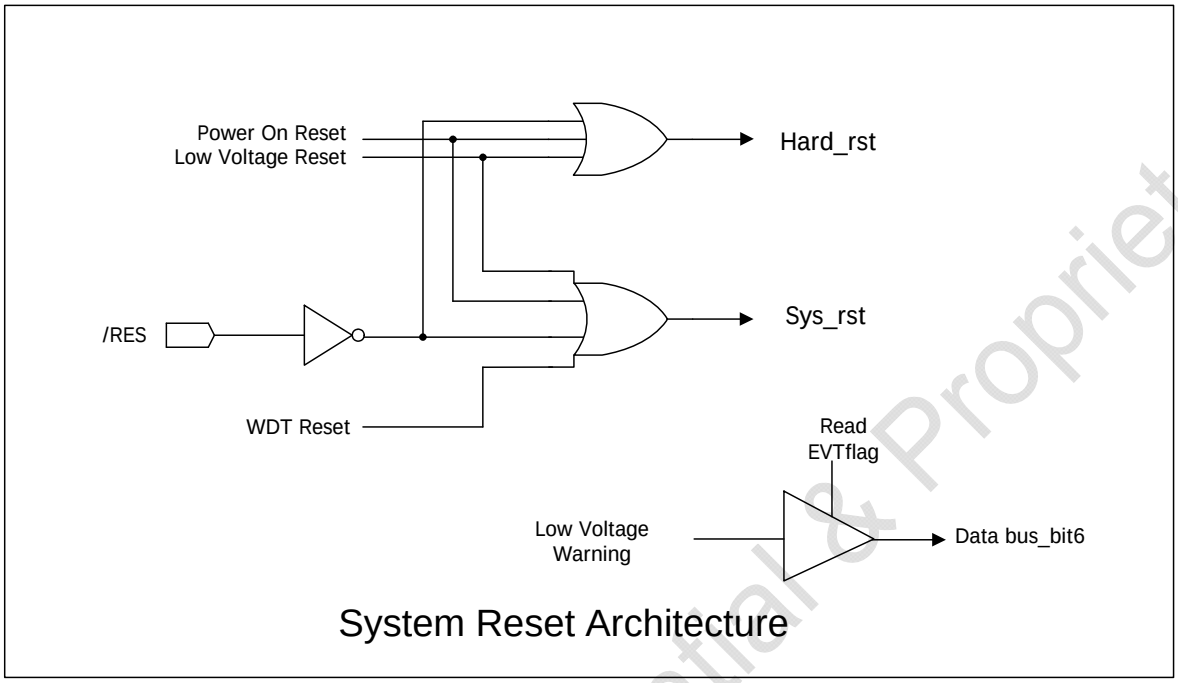


Figure 7-1 Interrupt System Diagram

8 Reset

8.1 System Reset Structure

MG69L355 have 4 kind of reset (Reset pin, POR, LVR and WDT).
The Chip reset Circuit shown below:



System Reset Architecture

8.2 Low Voltage Reset (LVR)

The MG69L355 provides low voltage reset circuit in order to monitor the supply voltage of the device. If the supply voltage of the device is within the range 0.9V ~ V_{LVR}, such as changing a battery, the LVR will automatically reset the device internally.

The LVR includes the following specifications:

1. The low voltage (0.9V~V_{LVR}) has to remain in their original state to exceed 1ms. If the low voltage state does not exceed 1ms, the LVR will ignore it and do not perform a reset function.
2. In the LVR mode, the on-chip oscillator is stopped and the on-chip SRAM is held. Port1 and Port2 set to high, port0 set to input mode with weakly pull high and IR is output high.

Low Voltage Detector:
The low voltage detector (2.1V) has no de-bounce ability. When V_{DD} is equal or lower than LVD, the LVD flag to be set high immediately. De-bounce should be implemented by software.

8.3 Watchdog Timer (WDT)

Watchdog Timer (WDT, The example is base on 3.579545MHz) Unit : Hz

Name					(Fosc /4096)/16				R	W
WDT	-	-	-	-	55	109	218	437	-	-

The watchdog timer time-out period is obtained by the equation: (Fosc / 4096)/16
Before watchdog timer time-out occurs, the program must clear the 4-bit WDT timer by writing 0 to EVTclr.5. WDT overflow will cause system reset and set EVTflag.5 to high.

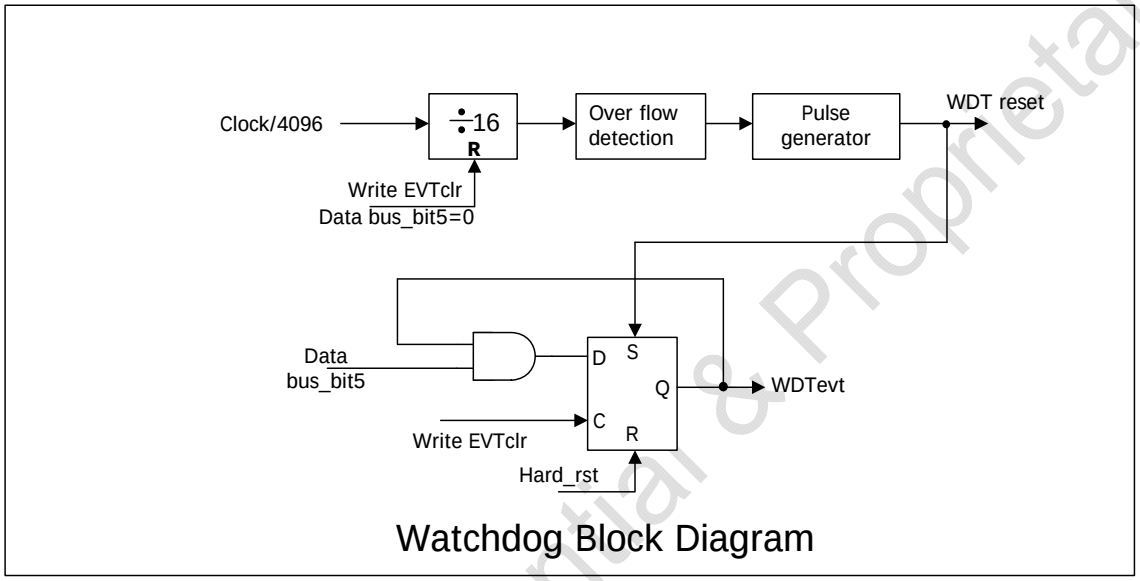


Figure 8-1 Watch Dog Diagram

8.4 Reset OK

Reset OK

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E1H	RESOK	RK7	RK6	RK5	RK4	-	-	-	-	-	√

RESOK (Reset OK): If the device reset OK and work well, **must** write #$90 into this register.
For example:

```
Program_start:    LDA   #10010000b
                  STA   $E1
```

Programming Notice
The status after different reset condition is listed below:

	Power on reset	CPU /RES pin reset
SRAM Data	Unknown	Unchanged
CPU Register	Unknown	Unknown
Special Function Register	Default value	Default value

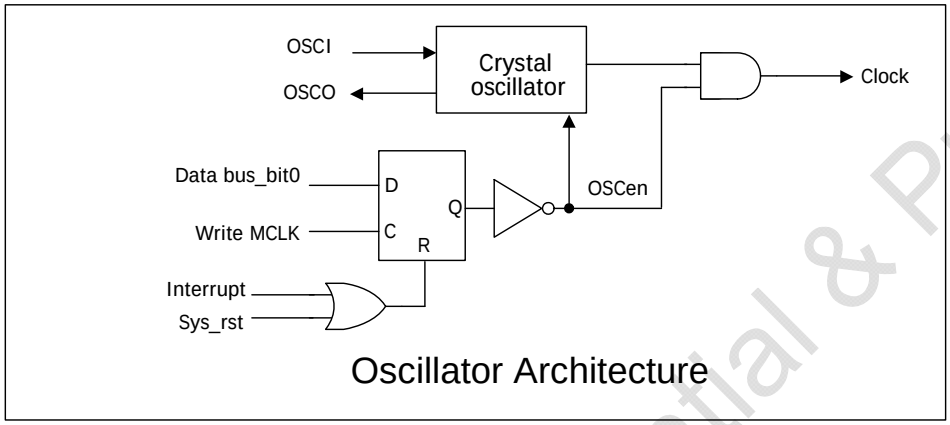
9 Power Control

9.1 Power Control Register

Main Clock Manager

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E0H	MCLKmgr	-	-	-	DIVsel	-	-	-	OSCen	-	√

OSCen: 0:The oscillator is free run. 1:The oscillator is frozen (stop mode).
When system clocks stop oscillating. The uC can be awakened from stop mode by 3-ways: port 0 interrupt, hardware reset, or power-on reset.
DIVsel: Divider interrupt frequency selector
0: The Fosc/4096 interrupt frequency is selected
1: The Fosc/256 interrupt frequency is selected



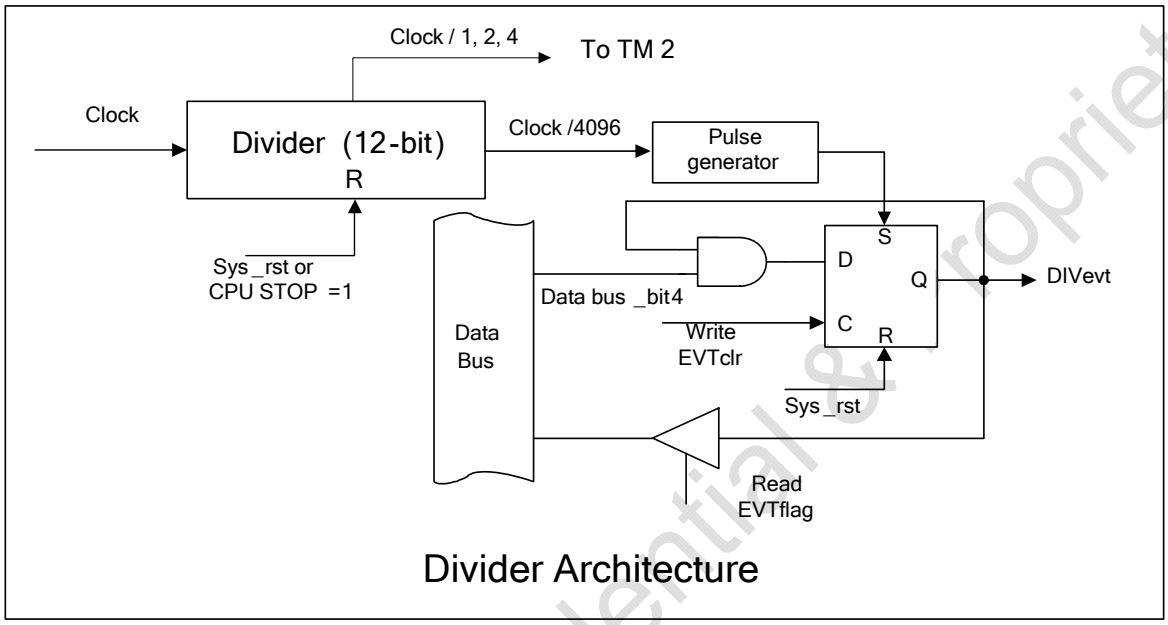
Oscillator Architecture

10 Divider

Divider (The example is base on 3. 579545MHz) **Unit : Hz**

Name	/256	/128	/64	/32	/16	/8	/4	/2	R	W
DIVlow	13984	227968	55937	111875	223750	447500	895000	1790000	-	-
Name					/4096	/2048	/1024	/512	R	W
DIVhigh	-	-	-	-	874	1748	3496	6992	-	-

The time-out period is obtained by the equation: 4096/OSC.
The DIV flag will be set when 4096/OSC or 256 /OSC (selected by DIVsel) is met.



Divider Architecture

11 Timer

11.1 Timer0

Timer0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E8H	TM0	T7	T6	T5	T4	T3	T2	T1	T0	√	√
00E9H	TM0_CTL	STC	RL/S	TKES	CPS	CTKS	-	TKI1	TKI0		√
00EAH	TM0_CAP	CP7	CP6	CP5	CP4	CP3	CP2	CP1	CP0	√	
00EBH	TM0_CAPB	CPB7	CPB6	CPB5	CPB4	CPB3	CPB2	CPB1	CPB0	√	

※ Bit-manipulation instructions are not available on this register.

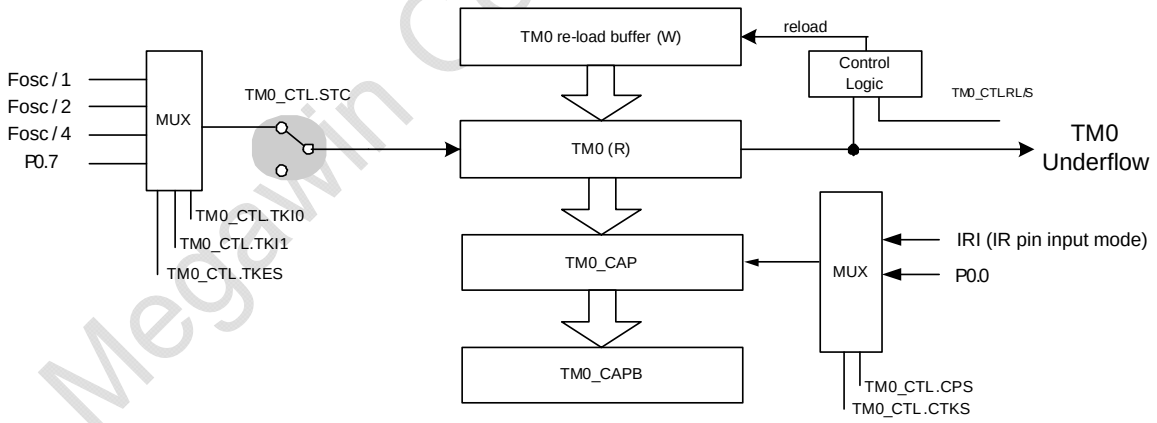
Timer 0 is an 8-bit down-count counter. The counter underflow frequency of timer 0 can be calculated with the equation: $F_{TM0\_UV} = F_{TM0} / (TM0+1)$

TM0: Read TM0 will get the counting value. Write TM0 will set the underflow value.

TM0_CAP: Capture the TM0 counting value.
TM0_CAPB: 1's complement of TM0_CAP.

TM0_CTL:
STC: Start/Stop counting. 1: start and pre-load the value to counter, 0: stop timer clock (set this bit to 1 will be ignored when this bit already set to 1)
RL/S: Auto-reload disable/enable. 1: disable auto-reload, 0: enable auto-reload
CPS: Capture TM0 counting value trigger source selection. 1: P0.0, 0: IRI (IR pin configured as input mode).
CTKS: Capture source trigger edge selector; 0: rising edge, 1: falling edge
TKES: Event or series input clock-in trigger edge selector; 0: rising edge, 1: falling edge

TKI1	TKI0	Selected TM0 input clock source
0	0	Fosc / 1
0	1	Fosc / 2
1	0	Fosc / 4
1	1	P0.7



TM0

11.2 Timer1

Timer1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00ECH	TM1	T7	T6	T5	T4	T3	T2	T1	T0	√	√
00EDH	TM1_CTL	STC	RL/S	TKES	CPS	CTKS	-	TKI1	TKI0		√
00EEH	TM1_CAP	CP7	CP6	CP5	CP4	CP3	CP2	CP1	CP0	√	
00EFH	TM1_CAPB	CPB7	CPB6	CPB5	CPB4	CPB3	CPB2	CPB1	CPB0	√	

※ Bit-manipulation instructions are not available on this register.

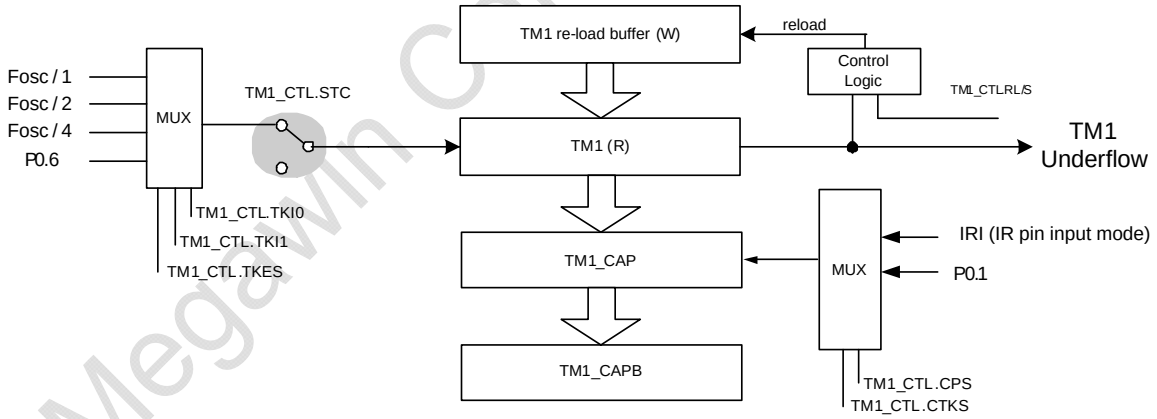
Timer 1 is an 8-bit down-count counter. The counter underflow frequency of timer 1 can be calculated with the equation: $F_{TM1\_UV} = F_{TM1} / (TM1+1)$

TM1: Read TM1 will get the counting value. Write TM1 will set the underflow value.

TM1_CAP: Capture TM1 counting value.
TM1_CAPB: 1's complement of TM1_CAP.

TM1_CTL:
STC: Start/Stop counting. 1: start and pre-load the value to counter, 0: stop timer clock (set this bit to 1 will be ignored when this bit already set to 1)
RL/S: Auto-reload disable/enable. 1: disable auto-reload, 0: enable auto-reload
CPS: Capture TM1 counting value trigger source select. 1: P0.1, 0: IRI (IR pin configured as input mode).
CTKS: Capture source trigger edge selector; 0: rising edge, 1: falling edge
TKES: Event or series input clock-in trigger edge selector; 0: rising edge, 1: falling edge

TKI1	TKI0	Selected TM1 input clock source
0	0	Fosc / 1
0	1	Fosc / 2
1	0	Fosc / 4
1	1	P0.6



TM1

11.3 Timer2

11.4 Timer2

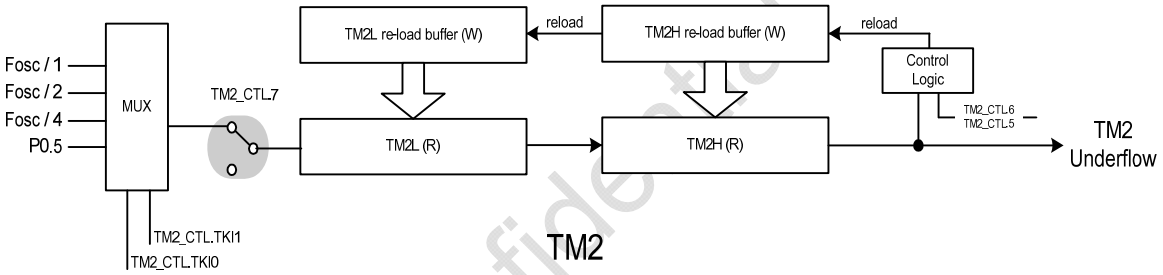
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E5H	TM2L	T7	T6	T5	T4	T3	T2	T1	T0	√	√
00E6H	TM2H	T15	T14	T13	T12	T11	T10	T9	T8	√	√
00E7H	TM2_CTL	STC	RL/S	TKES	-	-	-	TKI1	TKI0		√

※ Bit-manipulation instructions are not available on this register.

Timer 2 is a 16-bit down-count counter. The counter underflow frequency of timer 2 can be calculated with the equation: $F_{TM2\_UV} = F_{TM2} / (TM2+1)$

STC: Start/Stop counting. 1: start and pre-load the value to counter, 0: stop timer clock
RL/S: Auto-reload disable/enable. 1: disable auto-reload, 0: enable auto-reload
TKES: Event or series input clock-in trigger edge selector; 0: rising edge, 1: falling edge

TKI1	TKI0	Selected TM2 input clock source
0	0	Fosc / 1
0	1	Fosc / 2
1	0	Fosc / 4
1	1	P0.5



12 Configurable I/O Ports

12.1 Port 0

Port 0 Pad

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00F1H	P0pad	P07	P06	P05	P04	P03	P02	P01	P00	√	-

Port 0 is an 8-bit input port with pull high resistors. Reading P0pad.n would always read the logic value from pad.

※ Bit-manipulation instructions are not available on this register.

12.2 Port 1

Port 1 Buffer

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00F5H	P1obuf	P17	P16	P15	P14	P13	P12	P11	P10	-	√

Port 1 is an 8-bit output port with selectable pull-high resistors. This register is used to buffer the out value of P1.0 ~ P1.7 and it is write-only. The P13~P10 are open-drain output and P17~P14 are CMOS/NMOS selection. **The pull-high resistors will be temporarily disable if the output value is low.**

※ Bit-manipulation instructions are not available on this register.

Port 1 Open-Drain Control Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00F6H	P1opd	OD7	OD6	OD5	OD4	-	-	-	-	-	√

0: Disable open-drain output (CMOS output), 1: Enable open-drain output

OD4 ~ OD7: These control bits are used to enable the open-drain of P1.4 ~ P1.7 pin.

※ Bit-manipulation instructions are not available on this register.

Port 1 Pull-high Control Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00F7H	P1plh	PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0	-	√

0: Disable internal pull-high, 1: Enable internal pull-high

PH0 ~ PH7: These control bits are used to enable the pull-high of P1.0 ~ P1.7 pin.

※ Bit-manipulation instructions are not available on this register.

12.3 Port 2

Port 2

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00FCH	P2	-	P26	P25	P24	P23	P22	P21	P20	√	√

Port 2 is a 7-bit quasi-bi-directional open drain output port with internal pull-high resistors. This register is used to buffer the out value of P2.0 ~ P2.6. Reading P2.n would always read the logic value from pad. **The pull-high resistors will be temporarily disable if the output value is low.**

※ Bit-manipulation instructions are not available on this register.

12.4 IR Control Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00FAH	IR_CTL	IRO	-	-	-	-	-	-	IR_SL	-	√
00FAH	IR_CTL	IRI	-	-	-	-	-	-	-	√	-

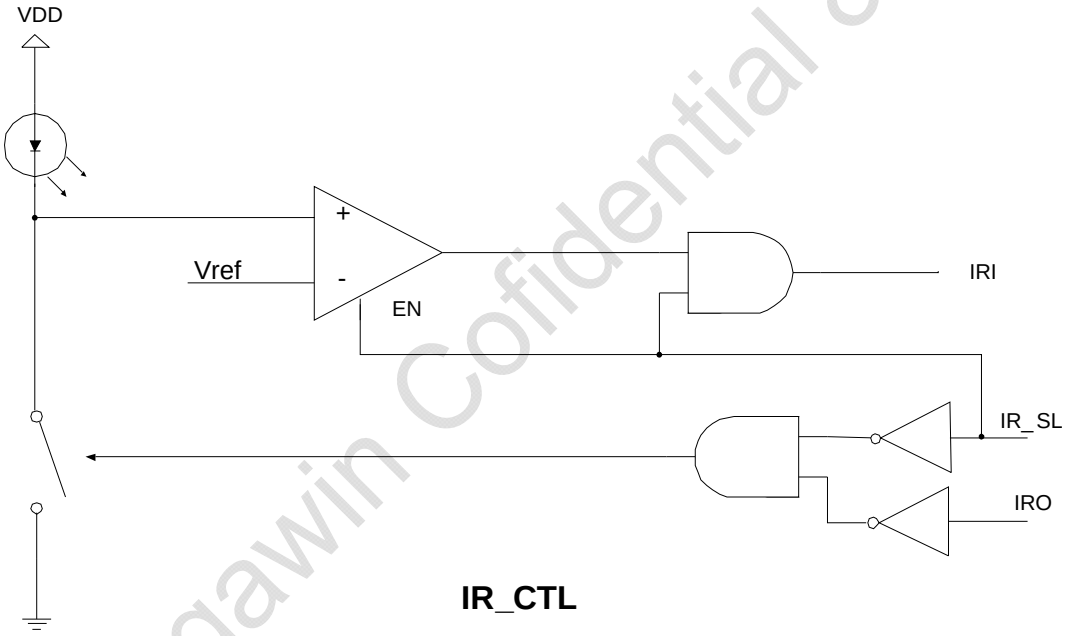
※ Bit-manipulation instructions are not available on this register.

IR_CTL is the IR pin input or output control register.

IR_SL: IR pin is input or output selector. 1: input mode, 0: output mode.

IRO: The IR pin output status in output mode (IR_SL=0). The IR pin output status is the inverted value of IR_CTL.7. So, write "1" to bit7 of the IR_CTL.7 (IRO) the IR pin will output low voltage and write "0" to bit7 of the IR_CTL.7 (IRO) the IR pin will output high voltage.

IRI: In input mode (IR_SL=1), the IR pin will be a high sensitive input port. Reading IR_CTL.7 (IRI) would always read the logic value from pad.



IR_CTL

13 Mask Option

WDT	Enable / Disable

14 Application Circuit

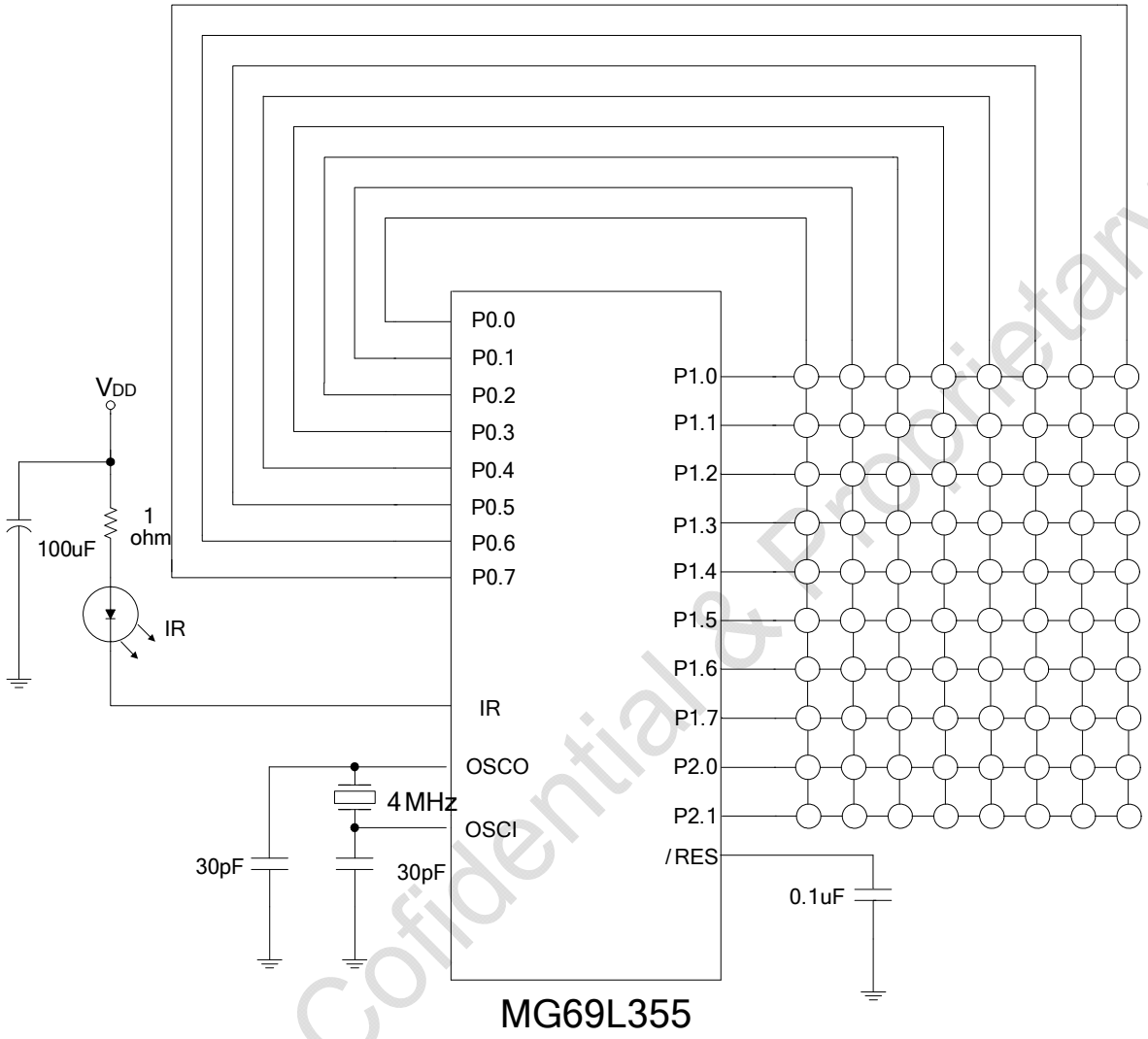


Figure 14-1 Application Circuit - Remote Controller

15 Electrical Characteristics

15.1 Absolute Maximum Rating

PARAMETER	RATING	UNIT
Supply Voltage to Ground Potential	VSS-0.3 to VSS+4.0	V
Applied Input / Output Voltage	VSS-0.3 to VDD+0.3	V
Ambient Operating Temperature	0 to +70	°C
Storage Temperature	-50 to +125	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

15.2 DC Characteristics

(VDD-VSS = 3.0 V, FOSC = 4MHz, Ta = 25° C; unless otherwise specified)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Op. Voltage	V_{DD}	-	1.8	-	3.6	V
Op. Current	I_{OP}	No load (Ext.-V) In normal operation	-	2.3	5	mA
Standby Current	I_{STB}	No load (Ext.-V)	-	1	3	μA
Input High Voltage	V_{IH}	-	0.7 V_{DD}	-	V_{DD}	V
Input Low Voltage	V_{IL}	-	0	-	0.3V_{DD}	V
Port 1.4~1.7 Drive Current	I_{OH0}	V_{OH} = 2.7V, V_{DD} = 3.0V (CMOS output mode)	5.0	10.0	-	mA
Port 1.0~1.7, Port 2.0~2.1 Sink Current	I_{OL0}	V_{OL} = 0.4V, V_{DD} = 3.0V	10.0	15.0	-	mA
IR Drive Current	$I_{OH\,2}$	V_{OH} = 2.7V, V_{DD} = 3.0V	5.0	8.0	-	mA
IR Sink Current	$I_{OL\,2}$	V_{OL} = 0.4V, V_{DD} = 3.0V	200	250	-	mA
P0/P1/P2 Pull-high Resistor	R_{PH}	V_{IL} = 0V	-	100K	-	Ω
/RES Pull-high Resistor	R_{RES}	V_{IL} = 0V	-	30K	-	Ω
Low Voltage Detector	V_{LVD}	V_{DD} > 2.1V	2.0	-	2.1	V
Low Voltage Reset	V_{LVR}	-	1.6	-	1.8	V

15.3 AC Characteristics

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CPU Op. Frequency	F_{CPU}	V_{DD} = 3.0V	0.4	4	8	MHz
System Start-Up Time	T_{SST}	Power-up, reset or wake-up from STOP mode	-	2048	-	1/ F_{CPU}

16 Revision History

Revision	Page	Descriptions	Date
Ver 0.10		MG69L355 original version	
Ver 0.11		Modified the logic structure	
Ver 0.12		Modified the learning circuit	
Ver 0.13		Modified DC characteristics	
Ver 0.14		Modified divider block diagram	
Ver 1.00		Update document format	2011/11/17