(Preliminary) MG69L952

8-bit I/O type MCU with LED driver

Features <<<

- Single chip 8-bit micro-controller
- Operating voltage: 1.8V to 3.6V
- Memory:
  - Program ROM : 64K bytes
  - Data RAM : 256 bytes
- 30 (6 + 24) high drive/sink I/O for LED display.
- 8 general input/output pins (P0.0 to P0.7)
- Two AUD output pins with 8-bit resolution for audio output
- Built-in RTC (Real Time Clock).
- Built-in low voltage reset (1.8V)
- Built-in two programmable timers and one 16-bit capture timer
  - Timer0, Timer1, Timer 2
- Oscillator:
  - Main oscillator (Crystal, Ceramic and RC up to 4MHz @ 2.0V) operation at crystal or RC mode is selected by code option
  - Sub-oscillator (Crystal and Ceramic up to 100KHz @ 2.0V) operation at crystal mode only

Application Field

LED Calendar, LED Name Badge, Toy Controller

2010/11 version 0.04

MEGAWIN

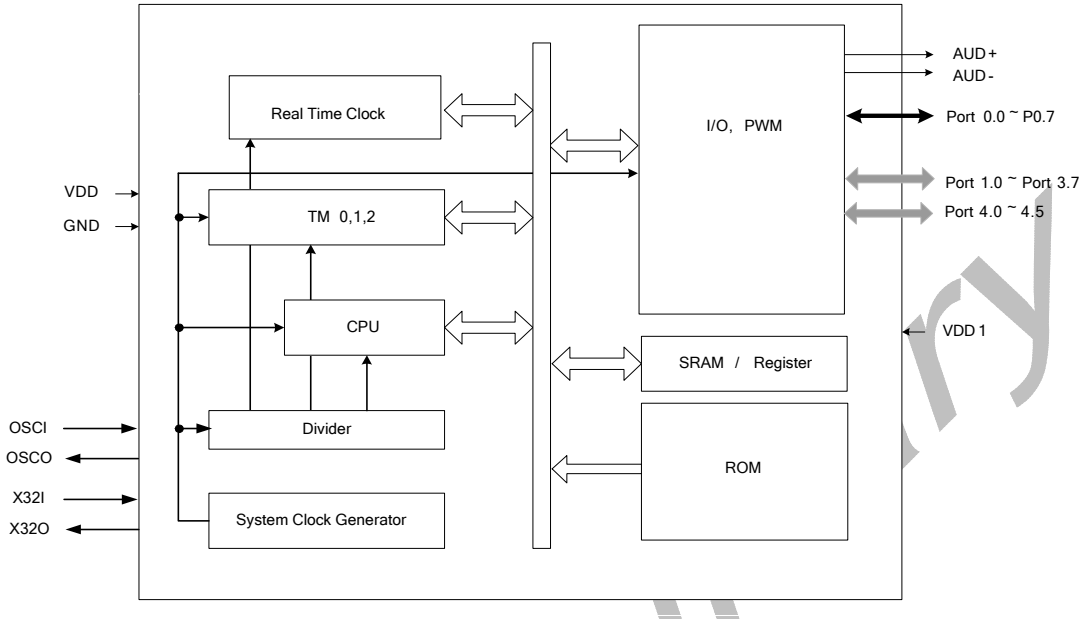
General Description

MG69L952 is a cost effective, high performance 8-bit micro-controller of MEGAWIN. It integrates an 8-bit CPU core, ROM, RAM, timers, RTC, I/O ports, and system control circuits into a single chip. It is suitable for LED calendar and other products.

Pad Description <<<

Pad No.	Pad Name	I/O	Description
T.B.D	P0.0~P0.7	I/O	General input/output function.
T.B.D	P1.0~P3.7	I/O	High sink current I/O for LED segment display.
T.B.D	P4.0~P4.5	O	High drive current output for LED common display.
T.B.D	/RES	I	System reset pin (low active)
T.B.D	OSCO, OSCI	O,I	RC or crystal oscillator pins
T.B.D	X32O, X32I	O,I	32.768KHz crystal oscillator pins
T.B.D	AUD+, AUD-	O	Audio output for direct drive speaker.
T.B.D	GND	P	Ground pin
T.B.D	VDD	P	Positive power pin for CPU and RTC
T.B.D	VDD1	P	Positive power pin for high drive/sink I/O port

Block Diagram <<<



Function Description

CPU Registers

	A
	Y
	X
	P
PCH	PCL
1	S

Accumulator

The accumulator is a general-purpose 8-bit register, which stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of two data words used in these operations.

Index Register (X, Y)

There are two 8-bit index registers (X and Y), which may be used to count program steps or to provide an index value to be used in generating an effective address. When executing an instruction, which specifies indexed addressing, the CPU fetches the OP Code and the base address, and modifies the address by adding the index register to it prior to performing the desired operation. Pre- or post-index of index address is possible.

Processor Status Register (P)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N	V	1	B	D	I	Z	C

N: Signed flag, 1 = negative, 0 = positive

V: Overflow flag, 1 = true, 0 = false

B: BRK interrupt command, 1 = BRK, 0 = IRQB

D: Decimal mode, 1 = true, 0 = false

I: IRQB disable flag, 1 = disable, 0 = enable

Z: Zero flag, 1 = true, 0 = false

C: Carry flag, 1 = true, 0 = false

Program Counter (PC)

The 16-bit program counter register provides the addresses, which step the micro-controller through sequential program instructions. Each time the micro-controller fetches an instruction from program memory, the lower byte of the program counter (PCL) is placed on the low-order 8 bits of the address bus, and the higher byte of the program counter (PCH) is placed on the high-order 8 bits. The counter is incremented each time when an instruction or data is fetched from program memory.

Stack Pointer (S)

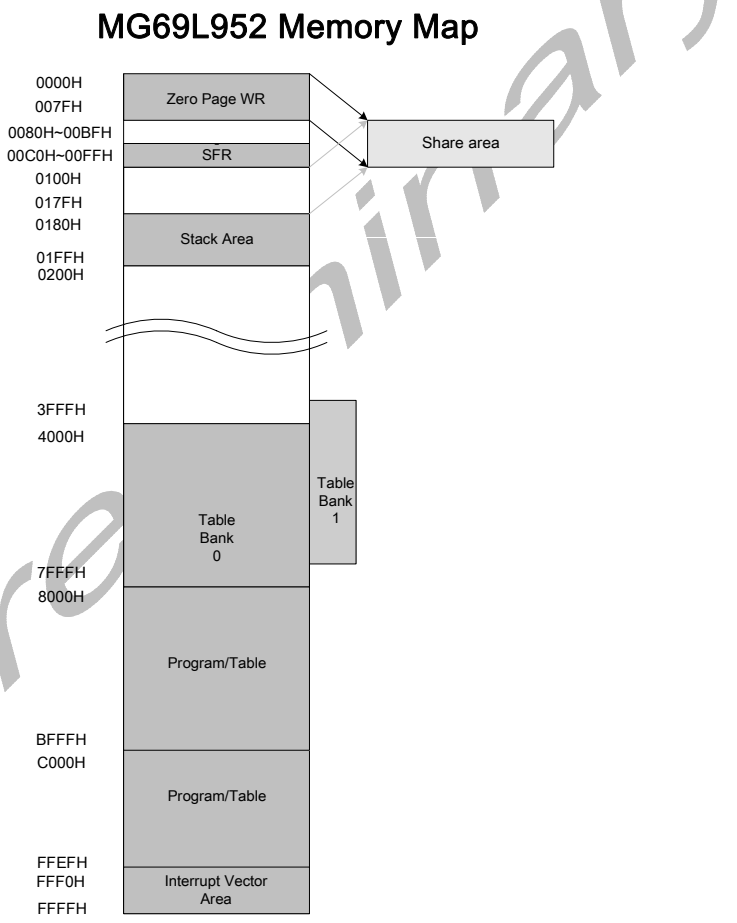
The stack pointer is an 8-bit register, which is used to control the addressing of the variable-length stack. The stack pointer is automatically incremented and decremented under control of the micro-controller to perform stack manipulations by direction of either the program or interrupts (/IRQ). The stack allows simple implementation of nested subroutines and multiple level interrupts. The stack pointer is initialized by the user's software.

Memory Map

There are 256 bytes SRAM, located in address 0000H to 007FH, in the MG69L952. They could be used as either working RAM or stacks according to application programs. For the purpose above, the location 0000H to 007FH and 0100H to 017FH are overlap. In other words, accessing any locations inside the range 0000H to 007FH is equivalent to access the corresponding ones in the range 0100 to 017FH.

All special function registers, SFRs, are located at the region 00C0H to 00FFH. Such an arrangement could benefit from the faster access time of zero-page.

Totally 64K bytes program/data ROM are built in the MG69L952. The ROM, located at 8000H to FFFFH, can store program and data. The address mapping of MG69L952 is shown as below:



Low Voltage Reset:

The MG69L952 provides low voltage reset circuit in order to monitor the supply voltage of the device. If the supply voltage of the device is within the range 0.9V ~ V_{LVR}, the LVR will automatically reset the device internally.

Special Function Register (SFR) <<<

The address 00C0H to 00FFH is reserved for special function registers (SFR). The SFR is used to control or store the status of I/O, timers, system clock and other peripheral.

SFR (special function register): 00C0H~00FFH

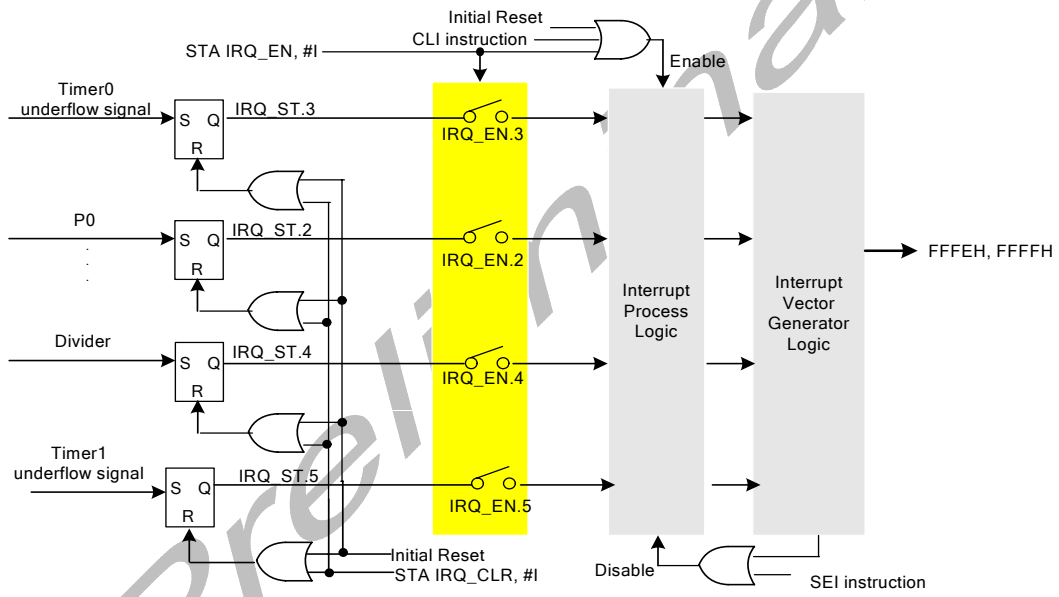
Address	Content	Default	Address	Content	Default
00C0	MCLKmgr	0-0--000	00D0		--------
00C1	SYS_STS	x-------	00D1		--------
00C2	IRQ_EN	-0000000	00D2	P0	00000000
00C3	IRQ_ST / IRQ_CLR	00000000	00D3	P0dir	00000000
00C4	RLH_EN	-0000000	00D4	P0plh	00000000
00C5		--------	00D5	P0opd	00000000
00C6		--------	00D6		--------
00C7		--------	00D7	P1	00000000
00C8	TM0	11111111	00D8	P1dir	00000000
00C9	TM0_CTL	00---000	00D9	P1plh	00000000
00CA	TM1	11111111	00DA	P1opd	00000000
00CB	TM1_CTL	00---000	00DB		--------
00CC	TM2L	11111111	00DC	P2	00000000
00CD	TM2H	11111111	00DD	P2dir	00000000
00CE	TM2_CTL	000--000	00DE	P2plh	00000000
00CF	DIV1_STL / DIV1_SEL	------00	00DF	P2opd	00000000

Address	Content	Default	Address	Content	Default
00E0	RTC00	00000000	00F0		--------
00E1		--------	00F1		--------
00E2		--------	00F2	BANK	-------0
00E3		--------	00F3	CWPR	xxxxxxxx
00E4		--------	00F4		--------
00E5		--------	00F5		--------
00E6		--------	00F6		--------
00E7		--------	00F7	CH1/ENV1	00000000
00E8	P3	00000000	00F8	CH2/ENV2	00000000
00E9	P3dir	00000000	00F9	AB_TC	0000-000
00EA	P3plh	00000000	00FA		--------
00EB	P3opd	00000000	00FB		--------
00EC	P4	--000000	00FC		--------
00ED	P4opd	--000000	00FD		--------
00EE		--------	00FE		--------
00EF		--------	00FF		--------

Interrupt Vectors

Vector Address	Item	Priority	Properties	Memo
FFFEH, FFFFH	IRQ	2	-	Interrupt vector
FFFCH, FFFDH	RESET	1	Ext.	Initial reset

There are seven kinds interrupt source is provided in MG69L952. The flag IRQ_EN and IRQ_ST are used to control the interrupts. When flag IRQ_ST is set to '1' by hardware and the corresponding bits of flag IRQ_EN has been set by software, an interrupt is generated. When an interrupt occurs, all of the interrupts are inhibited until the CLI or STA IRQ_EN, #I instruction is invoked. Executing the SEI instruction can also disable the interrupts.



Interrupt Registers

IRQ enable flag

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C2H	IRQ_EN	-	TM2	TM1	DIV	TM0	P0	VD1	RTC	√	√

Program can enable or disable the ability of triggering IRQ through this register.

0: Disable (default "0" at initialization)

1: Enable

P0: Falling edge occurs at port 0 input mode

TM0, TM1, TM2: Timer 0, 1, 2 underflow occurs

DIV: Divider selected interrupt frequency occurred

VD1: Rising or falling edge occurs at VDD1 (both edge could generate interrupt)

RTC: RTC 0.5S interrupt

IRQ status flag (same address with IRQ_CLR)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C3H	IRQ_ST	WDT	TM2	TM1	DIV	TM0	P0	VD1	RTC	√	-

When IRQ occurs, program can read this register to know which source triggering IRQ. If the interrupt triggering is enabled and the interrupt event is accepted, the correspond IRQ status flag should be cleared by program after the interrupt vector is loaded into program counter. All the interrupt behavior is same as above description

IRQ clear flag

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C3H	IRQ_CLR	WDT	TM2	TM1	DIV	TM0	P0	VD1	RTC	-	√

Program can clear the interrupt event by writing '1' into the corresponding bit.

Release halt mode enable flag

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C4H	RLH_EN	-	TM2	TM1	DIV	TM0	P0	VD1	RTC	-	√

Set IRQ_CLR register to clear the halt release event.

Release halt status flag is the IRQ_ST register.

System Status

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C1H	SYS_STS	VD1S	-	-	-	-	-	-	-	√	-

VD1S: VDD1 high/low status flag (external pull low should be added between VDD1 pin and GND pin if the VD1 interrupt is used in your application)

System Control Registers

Bank select

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00F2H	BANK	-	-	-	-	-	-	-	BK0	√	√

Program can switch the memory bank through this register. After power on reset, this register in initialized as 00H

Conditional Write Protect Register <<<

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00F3H	CWPR	PT7	PT6	PT5	PT4	PT3	PT2	PT1	PT0	-	√

PT7 ~ PT0: Conditional Write Protect Pattern

The CWPR is used to be the IRQ_CLR.7 (WDT) and MCLKmgr write protector.

To unlock the write protector, it must write pattern 58H to CWPR SFR firstly. The CWPR would be cleared by hardware automatically after the “next write action” of firmware. When the CWPR is cleared to zero, the system will back to write protect status.

Main Clock Manager <<<

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C0H	MCLKmgr	CKS7	-	IORS	-	-	CKC1	CKC0	HALT	-	√

CKS7: F_{CPU} clock source select. 0: F_{OSC}, 1:F_{X32}

IORS: IO reset selector

0: Only WDT can not reset the I/O status

1: All reset sources (/RES pin, POR, LVR, WDT) can reset the I/O status

CKC1	CKC0	System clock control
0	0	F_{OSC} enable, F_{X32} enable (Dual mode)
0	1	F_{OSC} enable, F_{X32} disable (Single mode)
1	0	F_{OSC} disable, F_{X32} enable (Slow mode)
1	1	F_{OSC} disable, F_{X32} disable (Stop mode)

Note: MCLKmgr.CKC0 is inhibited when the code option NMO F_{X32} is enabled.

HALT: F_{CPU} off-line control bit. 1: F_{CPU} off-line, 0: F_{CPU} on-line

Program can switch the normal operation mode to the power-saving mode for saving power consumption through this register. There are three power saving modes in this system.

Slow mode: *(MCLKmgr.CKC1 =1, MCLKmgr.CKC0 = 0)*

The main uC clock (F_{OSC}) stops oscillating. Only very low power is needed for uC to keep running.

Stop mode: *(MCLKmgr.CKC1 = 1, MCLKmgr.CKC0 = 1)*

All system clocks stop oscillating. The uC can be awakened from stop mode by 4-ways: port 0 interrupt, hardware reset, low voltage reset, or power-on reset. This mode is inhibited when the code option NMO F_{X32} is enabled.

Halt mode: *(MCLKmgr.HALT = 1)*

The F_{CPU} clock in off-line status. The oscillator(s) still oscillating if the MCLKmgr.CKC1, MCLKmgr.CKC0 keep low. The uC can be awakened from halt mode by 5-ways: all interrupt events (DIV, TM0, TM1, TM2, port 0, VDD1, RTC), hardware reset, low voltage reset, watchdog timer reset, or power-on reset. Before enter halt mode, the F_{CPU} must set to slow mode firstly to make the current consumption less than 10uA.

Note: Conditional Write Protect Register (CWPR) protects the contents of MCLKmgr register. When system change operation mode, the program must write 58H to CWPR and then set MCLKmgr at next write OP code.

For example, the operation of entry stop mode as below:

Example:

```
SEI
LDA    #58h
STA    CWPR          ;(F3h)
LDA    #06H          ; Fcpu = Fm
STA    C0H           ; MCLKmgr
CLI
```

DIV1 interrupt selector (If the frequency of divider 1 clock source is 32.768KHz)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00CFH	DIV1_STL	128 Hz	256 Hz	512 Hz	1024 Hz	2048 Hz	4096 Hz	8192 Hz	16384 Hz	√	-
00CFH	DIV1_SEL	-	-	-	-	-	-	CKO1	CKO0	-	√

The clock source of divider 1 is fixed to X32. The divider 1 contents can be reset to 00H by POR, LVR only.

CKO1	CKO0	Selected DIV1 frequency
0	0	F_{DIV1} / 4 (8192 Hz)
0	1	F_{DIV1} / 32 (1024 Hz)
1	0	F_{DIV1} / 64 (512 Hz)
1	1	F_{DIV1} / 128 (256 Hz)

RTC (Real Time Clock) **register** (clock source is F_{X32}/256) **<<<**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E0H	RTC00	S7	S6	S5	S4	S3	S2	S1	S0	√	√

The RTC part contains one 8-bit registers with an auto-incrementing address register, an on-chip 32.768kHz oscillator with an integrated capacitor, a frequency divider which provides the source clock for the Real-Time Clock (RTC). The RTC contents can be reset to 00H by POR only.

Program can enable or disable the ability of triggering RTC interrupt through IRQ_IEN.0 register.

Programmer can clear the IRQ_ST.0 by writing '1' into the bit 0 of IRQ_CLR.

(The example frequency is 32.768KHz)

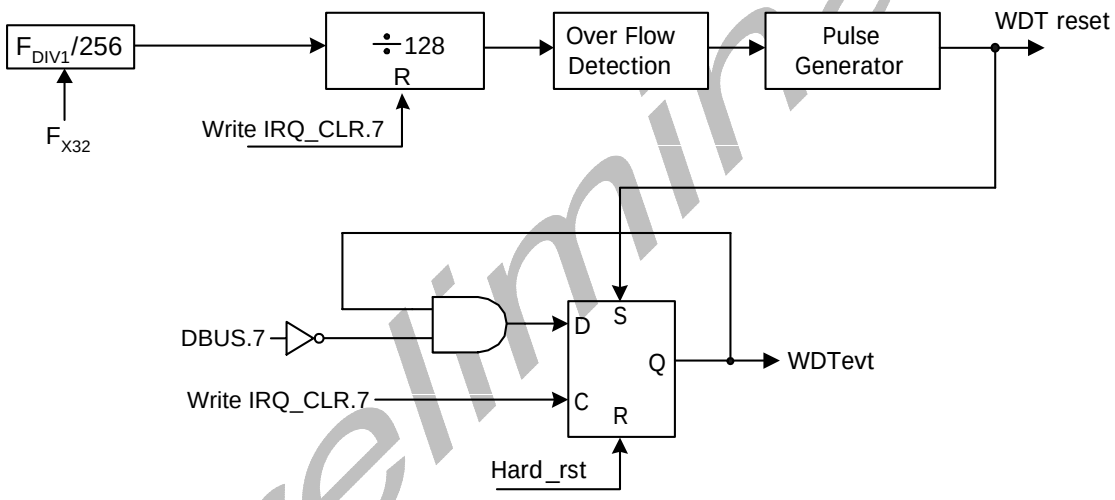
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E0H	RTC00	2S	1S	2Hz	4Hz	8Hz	16Hz	32Hz	64Hz	√	√

Watchdog Timer (WDT, The example is base on 32.768KHz/ (256x128)) **<<<**

Name		/128	/64	/32	/16	/8	/4	/2	R	W
WDT		1Hz	2Hz	4Hz	8Hz	16Hz	32Hz	64Hz	-	-

The watchdog timer time-out period is obtained by the equation: F_{X32}/(256x128).

Before watchdog timer time-out occurs, the program must clear the 7-bit WDT timer by writing 1 to IRQ_CLR.7. WDT overflow will cause system reset and set IRQ_CLR.7 to high. Before watchdog timer time-out occurs, the program must write 58H into CWPR then clear the 7-bit WDT timer by writing 1 to IRQ_CLR.7 at next write OP code. WDT overflow will cause system reset and set IRQ_ST.7 to high. The WDT register contents will be reset by hardware reset, low voltage reset and power-on reset.



Watchdog Block Diagram

The operation of clear WDT example is shown as below:

```
clear_WDT .macro
          SEI
          LDA     #58h
          STA     CWPR              ;(F3h)
          LDA     #80H
          STA     C3H               ; IRQ_CLR
          CLI
.endm
```

Timers/Counters

Timer0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C8H	TM0	T7	T6	T5	T4	T3	T2	T1	T0	√	√
00C9H	TM0_CTL	STC	RL/S	-	-	-	TKI2	TKI1	TKI0		√

STC: Start/Stop counting. 1: start and pre-load the value to counter, 0: stop timer clock

RL/S: Auto-reload disable/enable. 1: disable auto-reload, 0: enable auto-reload

TKI2	TKI1	TKI0	Selected TM0 input frequency
0	0	0	F_{OSC} / 1
0	0	1	F_{OSC} / 4
0	1	0	F_{OSC} / 16
0	1	1	F_{OSC} / 64
1	X	X	F_{X32}

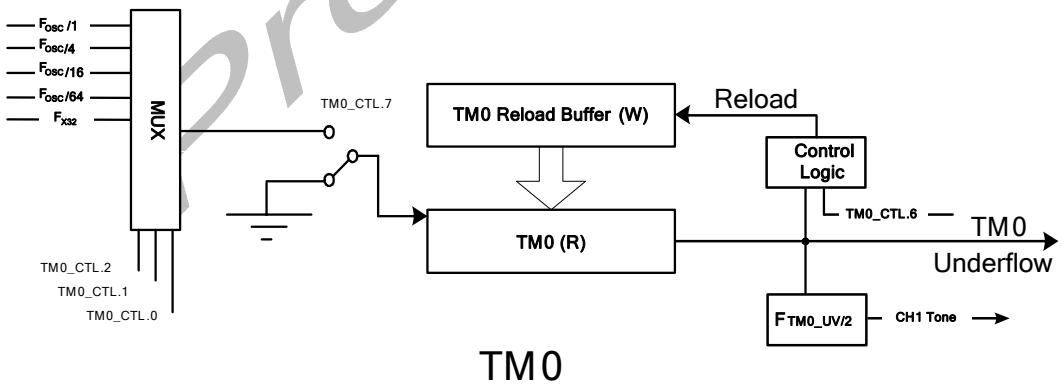
X: Don't care.

Timer 0 is an 8-bit down-count counter. The counter underflow frequency of timer 0, F_{TM0_UV}, can be calculated with the equation:

$F_{TM0\_UV} = F_{TM0} / (TM0+1)$**,** where the F_{TM0} is the timer input frequency set by TKI2, TKI1 and TKI0.

For example: (if F_{TM0} = 2.000MHz, TKI2=TKI1=TKI0=0)

TM0	Frequency
00H	Reserved
01H	1.000MHz
02H	667kHz
…	…
FFH	7.84kHz



TM0

Timer1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00CAH	TM1	T7	T6	T5	T4	T3	T2	T1	T0	√	√
00CBH	TM1_CTL	STC	RL/S	-	-	-	TKI2	TKI1	TKI0		√

STC: Start/Stop counting. 1: start and pre-load the value to counter, 0: stop timer clock

RL/S: Auto-reload disable/enable. 1: disable auto-reload, 0: enable auto-reload

TKI2	TKI1	TKI0	Selected TM1 input frequency
0	0	0	F_{OSC} / 1
0	0	1	F_{OSC} / 4
0	1	0	F_{OSC} / 16
0	1	1	F_{OSC} / 64
1	X	X	F_{X32}

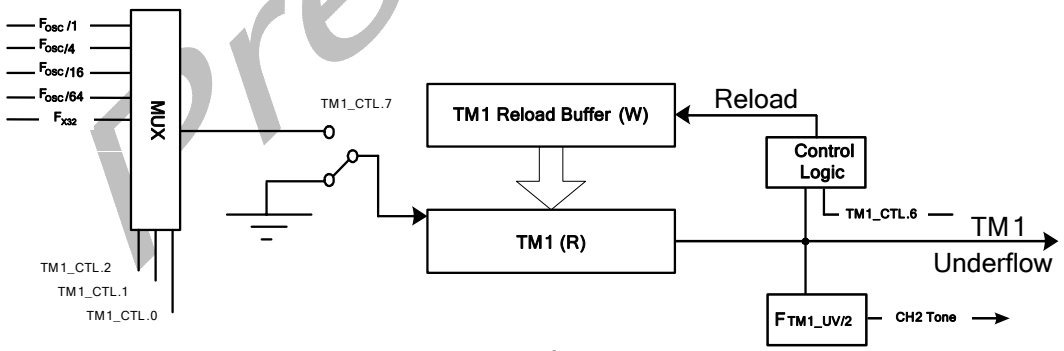
X: Don't care.

Timer 1 is an 8-bit down-count counter. The counter underflow frequency of timer 1, F_{TM1_UV}, can be calculated with the equation:

$F_{TM1\_UV} = F_{TM1} / (TM1+1)$**,** where the F_{TM1} is the timer input frequency set by TKI2, TKI1 and TKI0.

For example: (if F_{TM1} = 2.000MHz, TKI2=TKI1=TKI0=0)

TM1	Frequency
00H	Reserved
01H	1.000MHz
02H	667kHz
…	…
FFH	7.84kHz



TM1

Timer2

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00CCH	TM2L	T7	T6	T5	T4	T3	T2	T1	T0	√	√
00CDH	TM2H	T7	T6	T5	T4	T3	T2	T1	T0	√	√
00CEH	TM2_CTL	STC	RL/S	GATE	-	-	TKI2	TKI1	TKI0		√

STC: Start/Stop counting. 1: start value to counter, 0: stop timer clock

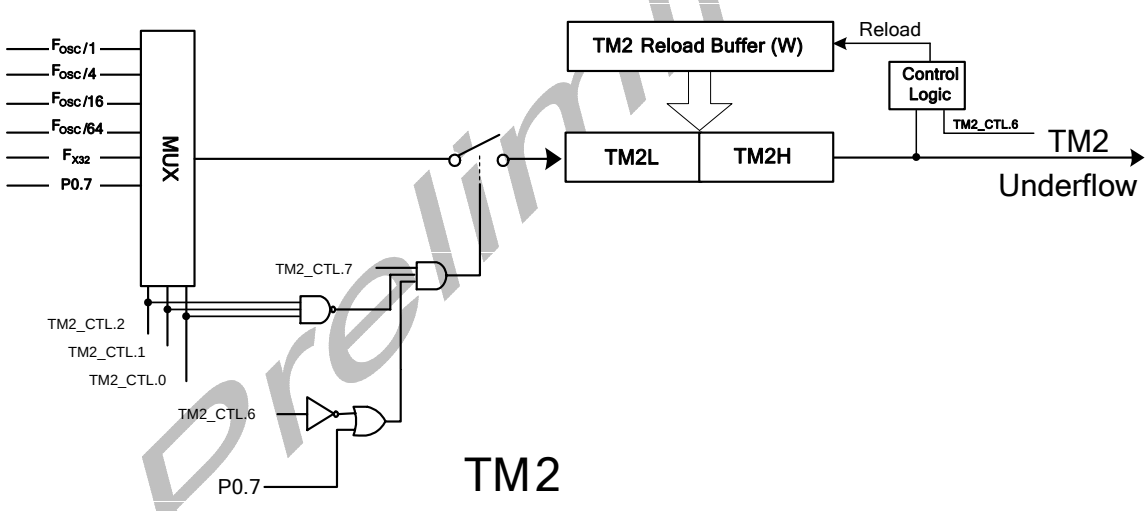
RL/S: Auto-reload disable/enable. 1: disable auto-reload, 0: enable auto-reload

Gate: Gating control. 1: Timer2 is enabled only while P0.7 is high and STC control bit is set.

0: Timer2 is enabled whenever STC control bit is set. When TKI2 to TKI0 are set to "1", the gate function will be disabled.

TKI2, TKI1, TKI0:

TKI2	TKI1	TKI0	Selected TM2 input frequency
0	0	0	F_{OSC} / 1
0	0	1	F_{OSC} / 4
0	1	0	F_{OSC} / 16
0	1	1	F_{OSC} / 64
1	0	0	F_{X32}
1	1	1	P0.7 (capture disable)



I/O Ports

Port 0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D2H	P0	P07	P06	P05	P04	P03	P02	P00	P00	√	√

Port 0 is an 8-bit I/O port; each pin can be programmed as input or output individually. However, reading P0.n would always read the logic value from pad. When port0.n is configured as an output pin, the port0.n pin would output the logic content of P0.n.

※ Bit-manipulation instructions not available on this register.

Port 0 Direction Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D3H	P0dir	DR7	DR6	DR5	DR4	DR3	DR2	DR1	DR0	-	√

P0dir (Port 0 Direction)

P0dir.n = 0: P0.n is configured as an input pin. (Default)

1: P0.n is configured as an output pin.

※ Bit-manipulation instructions not available on this register.

Port 0 Pull-high Control Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D4H	P0plh	PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0	-	√

PH0 ~ PH7: Control bit is used to enable the pull-high of P0.0 ~ P0.7 pin.

0: Disable internal pull-high (default); 1: Enable internal pull-high, the pull-high will be disable automatically when P0.n is set to output mode low state;

※ Bit-manipulation instructions not available on this register.

Port 0 Open-Drain Control Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D5H	P0opd	OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0	-	√

OD0 ~ OD7: Control bit is used to enable the open-drain of P0.0 ~ P0.7 pin.

0: Disable open-drain output (CMOS output), 1: Enable open-drain output

※ Bit-manipulation instructions not available on this register.

Port 1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D7H	P1	P17	P16	P15	P14	P13	P12	P10	P10	√	√

Port 1 is an 8-bit I/O port; each pin can be programmed as input or output individually. However, reading P1.n would always read the logic value from pad. When port1.n is configured as an output pin, the port1.n pin would output the logic content of P1.n.

※ Bit-manipulation instructions not available on this register.

Port 1 Direction Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D8H	P1dir	DR7	DR6	DR5	DR4	DR3	DR2	DR1	DR0	-	√

P1dir (Port 1 Direction)

P1dir.n = 0: P1.n is configured as an input pin. (Default)

1: P1.n is configured as an output pin.

※ Bit-manipulation instructions not available on this register.

Port 1 Pull-high Control Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D9H	P1plh	PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0	-	√

PH0 ~ PH7: Control bit is used to enable the pull-high of P1.0 ~ P1.7pin.

0: Disable internal pull-high (default); 1: Enable internal pull-high, the pull-high will be disable automatically when P1.n is set to output mode low state;

※ Bit-manipulation instructions not available on this register.

Port 1 Open-Drain Control Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00DAH	P1opd	OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0	-	√

OD0 ~ OD7: Control bit is used to enable the open-drain of P1.0 ~ P1.7 pin.

0: Disable open-drain output (CMOS output); 1: Enable open-drain output

※ Bit-manipulation instructions not available on this register.

Port 2

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00DCH	P2	P27	P26	P25	P24	P23	P22	P21	P20	√	√

Port 2 is an 8-bit I/O port; each pin can be programmed as input or output individually. However, reading P2.n would always read the logic value from pad. When port2.n is configured as an output pin, the port2.n pin would output the logic content of P2.n.

※ Bit-manipulation instructions not available on this register.

Port 2 Direction Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00DDH	P2dir	DR7	DR6	DR5	DR4	DR3	DR2	DR1	DR0	-	√

P2dir (Port 2 Direction)

P2dir.n = 0: P2.n is configured as an input pin. (Default)

1: P2.n is configured as an output pin.

※ Bit-manipulation instructions not available on this register.

Port 2 Pull-high Control Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00DEH	P2plh	PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0	-	√

PH0 ~ PH7: Control bit is used to enable the pull-high of P2.0 ~ P2.7 pin.

0: Disable internal pull-high (default); 1: Enable internal pull-high, the pull-high will be disable automatically when P2.n is set to output mode low state;

※ Bit-manipulation instructions not available on this register.

Port 2 Open-Drain Control Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00DFH	P2opd	OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0	-	√

OD0 ~ OD7: Control bit is used to enable the open-drain of P2.0 ~ P2.7 pin.

0: Disable open-drain output (CMOS output); 1: Enable open-drain output

※ Bit-manipulation instructions not available on this register.

Port 3

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E8H	P3	P37	P36	P35	P34	P33	P32	P31	P30	√	√

Port 3 is an 8-bit I/O port; each pin can be programmed as input or output individually. However, reading P3.n would always read the logic value from pad. When port3.n is configured as an output pin, the port3.n pin would output the logic content of P3.n.

※ Bit-manipulation instructions not available on this register.

Port 3 Direction Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E9H	P3dir	DR7	DR6	DR5	DR4	DR3	DR2	DR1	DR0	-	√

P3dir (Port 3 Direction)

P3dir.n = 0: P3.n is configured as an input pin. (Default)

1: P3.n is configured as an output pin.

※ Bit-manipulation instructions not available on this register.

Port 3 Pull-high Control Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00EAH	P3plh	PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0	-	√

PH0 ~ PH7: Control bit is used to enable the pull-high of P3.0 ~ P3.7pin.

0: Disable internal pull-high (default); 1: Enable internal pull-high, the pull-high will be disable automatically when P3.n is set to output mode low state;

※ Bit-manipulation instructions not available on this register.

Port 3 Open-Drain Control Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00EBH	P3opd	OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0	-	√

OD0 ~ OD7: Control bit is used to enable the open-drain of P3.0 ~ P3.7pin.

0: Disable open-drain output (CMOS output); 1: Enable open-drain output

※ Bit-manipulation instructions not available on this register.

Port 4 Buffer <<<

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00ECH	P4	-	-	P45	P44	P43	P42	P41	P40	√	√

Port4 is a 6-bit NMOS/CMOS output port and it has highly drive current up to 180mA for turn on LED array.

However, reading P4.n would always read the logic value from pad.

<< To avoid over current operation, please do not set over one bit to high and keep enough time delay for LED turn off. >>

Port4 Open-Drain Control Register<<<

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00EDH	P4opd	-	-	OD5	OD4	OD3	OD2	OD1	OD0	-	√

OD0 ~ OD7: Control bit is used to enable the open-drain of P4.0 ~ P4.5pin.

0: Disable open-drain output (CMOS output); 1: Enable open-drain output (NMOS output)

※ Bit-manipulation instructions not available on this register.

CH1, CH2 Buffer

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00F7H	CH1/ENV1	EN7	EN 6	EN 5	EN 4	EN 3	EN 2	EN 1	EN 0	-	√
00F8H	CH2/ENV2	EN7	EN 6	EN 5	EN 4	EN 3	EN 2	EN 1	EN 0	-	√

```
LDA     Voice   ; Load 8-bit voice data to accumulator
STA     F7H     ;
```

AUD buffer transfer control<<<

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00F9H	AB_TC	AEN	VTS6	TC5	TC4	-	VTS2	TC1	TC0	√	√

AB_TC is a voice or tone control register. When AEN is set as disable, the AUD+ and AUD- will be set to open drain high impendence. VTS6 and VTS2 are used to control the path of voice or tone. TC5~ TC3, TC2~TC0 are used to control the AUD buffer transfer method. Before disable all the AUD output, user must progress the fade out subroutine to avoid the noise burst.

AEN: AUD enable control. 0: disable, 1:enable

In STOP mode or halt mode, the AUD output must be turn off (set AEN to "0") to save power consumption.

VTS6: Ch 2 voice/tone control. 0: voice, 1:tone

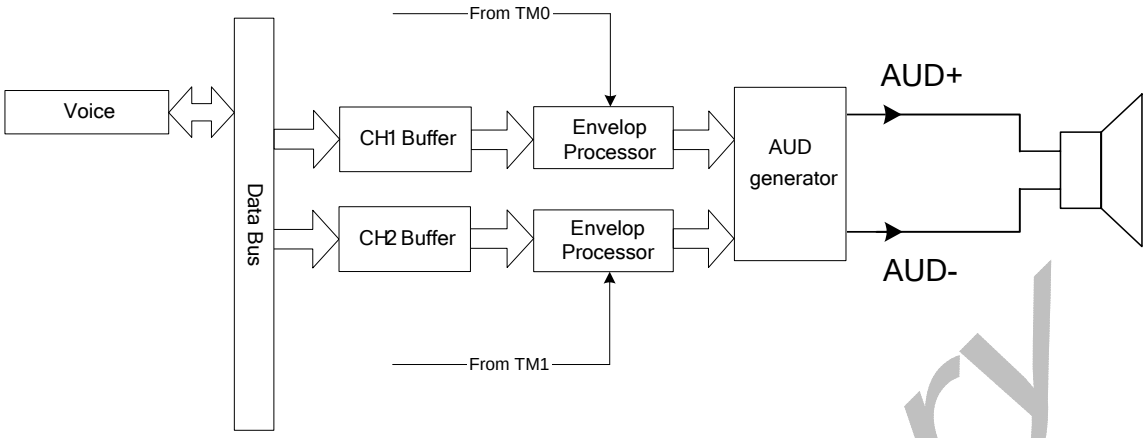
TC5	TC4	AUD buffer transfer control
0	0	Ch 2 buffer data transfer to AUD after TM0 underflow
0	1	Ch 2 buffer data transfer to AUD after TM1 underflow
1	0	Ch 2 buffer data transfer to AUD after TM2 underflow
1	1	Ch 2 buffer data transfer to AUD directly

VTS2: Ch 1 voice/tone control. 0: voice, 1:tone

TC1	TC0	AUD buffer transfer control
0	0	Ch 1 buffer data transfer to AUD after TM0 underflow
0	1	Ch 1 buffer data transfer to AUD after TM1 underflow
1	0	Ch 1 buffer data transfer to AUD after TM2 underflow
1	1	Ch 1 buffer data transfer to AUD directly

AUD output current

The drive current of AUD buffer is typically 150mA at V_{DD}=3volt. It is suit to direct drive a speaker or buzzer.

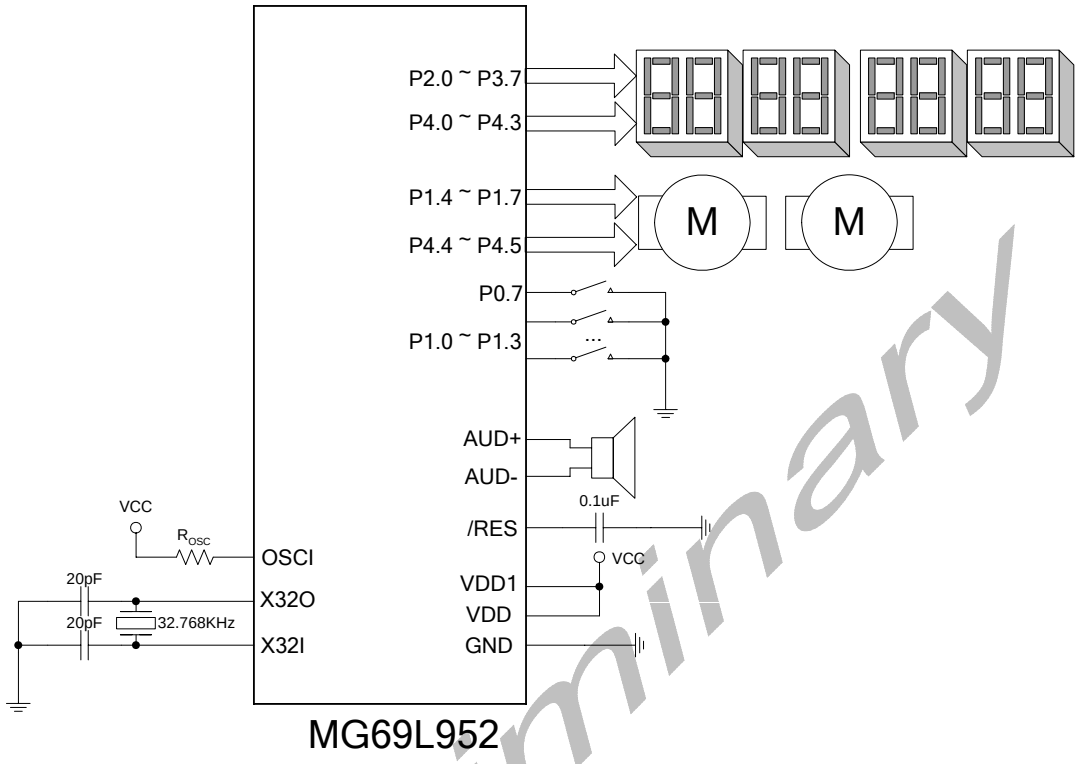


Programming Notice

The status after different reset condition is listed below:

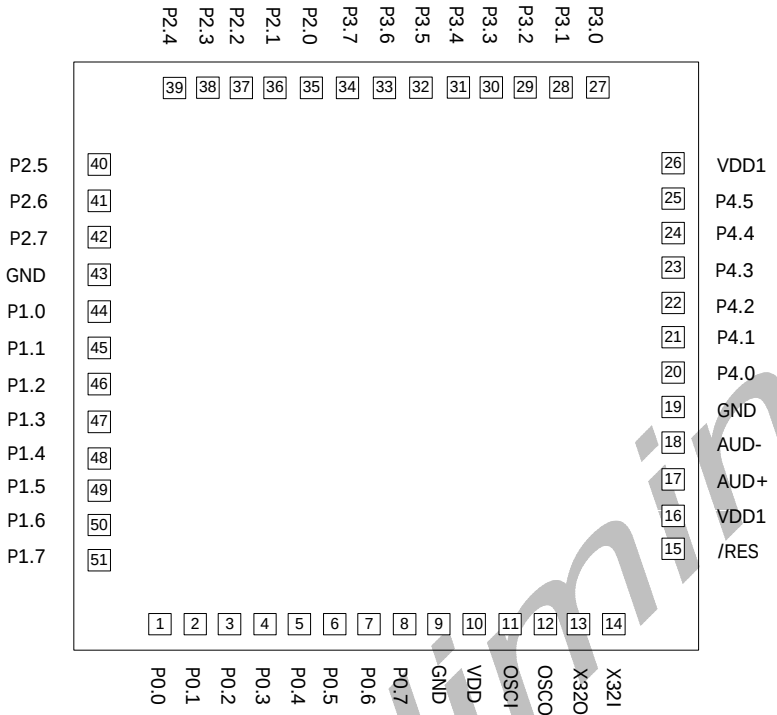
	Power on reset	CPU /RES pin reset
SRAM Data	Unknown	Unchanged
CPU Register	Unknown	Unknown
Special Function Register	Default value	Default value

Application circuit <<<



Pad Assignment <<<

T.B.D



Absolute Maximum Rating

PARAMETER	RATING	UNIT
Supply Voltage to Ground Potential	-0.3 to +4.0	V
Applied Input / Output Voltage	-0.3 to +4.0	V
Power Dissipation	800	mW
Ambient Operating Temperature	0 to +70	°C
Storage Temperature	-55 to +150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

DC Characteristics<<<

(V_{DD}-V_{SS} = 3.0 V, F_{OSC} = 4MHz, Ta = 25° C; unless otherwise specified)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Op. Voltage	V_{DD}	-	1.8	-	3.6	V
Op. Current	I_{OP}	No load (Ext.-V) In dual clock operation	-	2	5	mA
Standby Current	I_{STB1}	Slow mode, No load, F_{CPU}=32768Hz	-	30	60	μA
	I_{STB2}	Halt mode, No load, F_{CPU}=32768Hz, RTC INT on	-	3	6	μA
	I_{STB3}	Halt mode, No load, F_{CPU}=32768Hz, RTC INT off, NMO F_{X32} Disabled	-	2	4	μA
	I_{STB4}	Stop mode, No load, NMO F_{X32} Disabled	-	1	2	μA
AUD+ buffer driving current	I_{AUD+}	R load = 8 Ω	150	-	-	mA
AUD- buffer driving current	I_{AUD-}	R load = 8 Ω	150	-	-	mA
Input High Voltage	V_{IH}	-	0.7 V_{DD}	-	V_{DD}	V
Input Low Voltage	V_{IL}	-	0	-	0.3V_{DD}	V
Port 0 drive current	I_{OH0}	V_{OH} = 2.4V, V_{DD} = 3.0V	3	-	-	mA
Port 0 sink current	I_{OL0}	V_{OL} = 0.4V, V_{DD} = 3.0V	3	-	-	mA
Port 1, 2, 3 drive current	I_{OH1}	V_{OH} = 2.4V, V_{DD} = 3.0V	3	-	-	mA
Port 1, 2, 3 sink current	I_{OL1}	V_{OL} = 0.4V, V_{DD} = 3.0V	20	-	-	mA
P4.0 ~ P4.5 drive current	I_{OH4}	V_{OH} = 2.4V, V_{DD} = 3.0V	-	150	180	mA
Port 4 sink current	I_{OL4}	V_{OH} = 0.4V, V_{DD} = 3.0V	3	-	-	mA
Internal Pull-high Resistor	R_{PH}	V_{IL} = 0V	25K	50K	100K	Ω
/RES Pull-high Resistor	R_{RES}	V_{IL} = 0V	-	30K	-	Ω
Low Voltage Reset	V_{LVR}	-	-	1.8	-	V

AC Characteristics

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CPU OP. Frequency	F_{CPU}	V_{DD} = 3.0V	0.4	4	6	MHz
System Start-Up Time	T_{SST1}	Power-up, reset or wake-up from STOP mode ($F_{CPU} = F_{OSC}$)	-	16384	-	1/ F_{CPU}
	T_{SST2}	Wake-up from STOP mode ($F_{CPU} = F_{X32}$)	-	2048	-	1/ F_{CPU}

Mask Option

Item	0 / 1
F_{OSC}	RC / Crystal
WDT	Enable / Disable
NMO F_{X32}	Enable / Disable

NMO F_{X32}: Non-Maskable Oscillator X32. The X32 cannot stop oscillating by MCLKmgr.CKC0 when it is enabled.

Typical Application (with RTC and with WDT)

F_{OSC}	RC
WDT	Enable
NMO F_{X32}	Enable

Application (without both RTC and WDT, connect X32I to GND)

F_{OSC}	RC or Crystal
WDT	Disable
NMO F_{X32}	Disable

Not Recommended Selection

F_{OSC}	RC or Crystal
WDT	Enable
NMO F_{X32}	Disable

History:

V0.10: Original

V0.20: Modify the WDT and RTC control logic

V0.30: Add the CWPR and P4 open drain function

V0.40: Modify the IORS description and P4 drive current

All change will be marked with "**<<<**"