Version: 1.08

MG69P361A

Datasheet

8-Bit Micro-Controller with IR function

Version 1.08

Table of Contents

1 Features

- Single chip 8-bit CPU
- Operation voltage: 2.2V to 3.6V
- Memory:
  - ◆ OTP ROM 128K Bytes
  - ◆ Data RAM: 256 Bytes (shared with stack)
- 16 input/output pins
  - ◆ Input with pull-high resistor selection
  - ◆ NMOS/CMOS output and pull-high resistor selection
  - ◆ Scan function (operation at stop mode): P0.0~P0.7, P1.0~P1.6
  - ◆ Two PWMs output
- 8 bi-directional input/output pins
- Oscillator pads share with bi-directional input/output pins: P3.0~P3.1
- One re-loadable 8-bit timer with capture function
- One re-loadable 8-bit timer
- One re-loadable 16-bit timer
- Build-in 4MHz±2% internal oscillator
- Build-in low speed internal oscillator
- Stop mode: micro-controller no operation (oscillator stop oscillating)
- Build-in watchdog timer
- Build-in serial peripheral interface
- Build-in voltage comparator
- 1 dedicated push pull I/O combined with IR amplifier input
- Build-in low voltage detectors (2.4V) and low voltage reset (typical voltage: below 2.2V)
- Built-In Low Speed I/O scan timer (Operation at main oscillator stop mode).
- Package type
  - ◆ SOP16
  - ◆ SOP28

1.1 Application Field

General IR Controller.

2 General Description

MG69P361A integrates an 8-bit CPU core, SRAM, timer and system control circuits by a CMOS silicon gate technology. The ROM can store data table and program.

Twenty-four I/O and one large sink output pin make this chip very suitable for IR application.

3 Pin Configurations

3.1 Pad Assignment

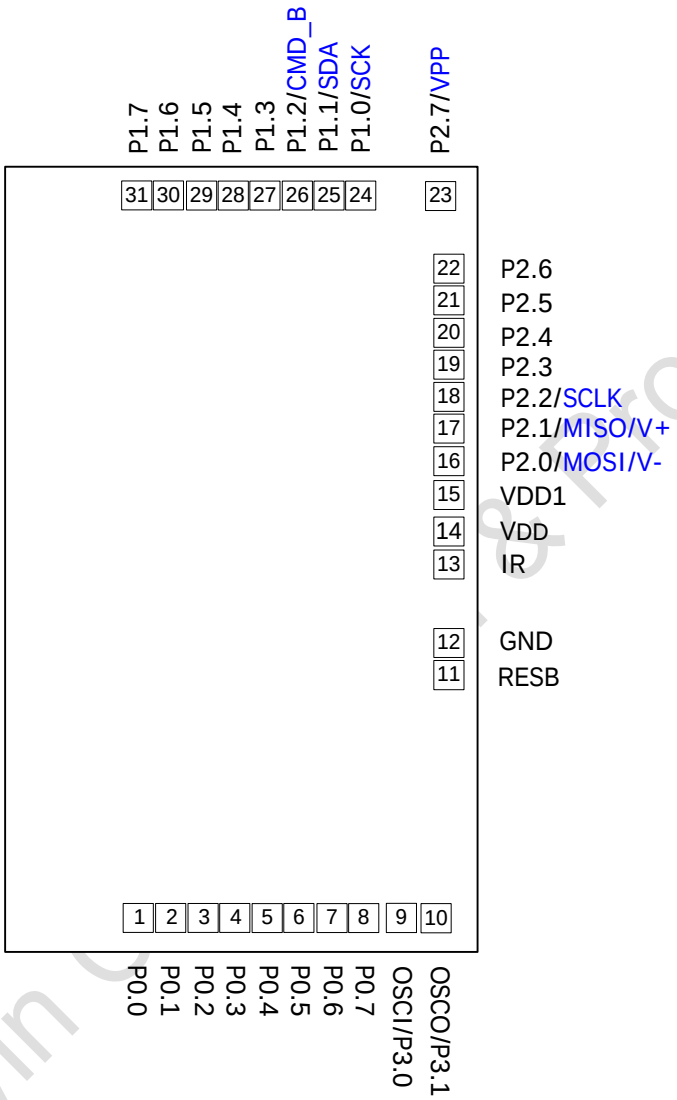


Figure 3-1 Pad Assignment

3.2 Pin Description

Table 3-1 Pin Description

Pad No.	Pad Name	I/O	Description
1 ~ 8	P0.0 ~ P0.7	B	Programmable I/O port, CMOS/NMOS output, input with pull high and interrupt function. The P0.0~P0.7 can use auto-scan function at stop mode.
9	OSCI / P3.0,	B	Resonator or crystal oscillator pin share with bi-directional I/O function
10	OSCO / P3.1	B	Resonator or crystal oscillator pin share with bi-directional I/O function
11	RESB	I	System reset pin (low active). Built in pull up 30K ohms.
12	GND	G	Ground pin
13	IR	O	IR input/output pin. Direct sink (sink current: 250mA) for IR LED. Default value is high after reset. The IR output pin is inverting bit7 of IR_CTL Buffer. So, write “1” to bit7 of the IR_CTL buffer the IR is output “0” and write “0” to bit7 of the IR_CTL buffer the IR is output “1”.
14	VDD	P	Positive power pins
15	VDD1	P	Positive power pins
16	P2.0 / MOSI / V-	B	Bi-directional I/O pins. It shares with SPI MOSI and voltage comparator inverting input pin.
17	P2.1 / MISO / V+	B	Bi-directional I/O pins. It shares with SPI MISO and voltage comparator non-inverting input pin.
18	P2.2 / SCLK	B	Bi-directional I/O pins. It shares with SPI SCLK pin.
19 ~ 22	P2.3 ~ P2.6	B	Bi-directional I/O pins.
23	P2.7 / VPP	B	Bi-directional I/O pin and share with OTP interface VPP pin
24	P1.0 / SCK	B	Programmable I/O pin, CMOS/NMOS output, input with pull high and interrupt function. The P1.0 can use auto-scan function at stop mode and shares with OTP interface SCK pin.
25	P1.1 / SDA	B	Programmable I/O pin, CMOS/NMOS output, input with pull high and interrupt function. The P1.1 can use auto-scan function at stop mode and shares with OTP interface SDA pin.
26	P1.2 / CMD_B	B	Programmable I/O pin, CMOS/NMOS output, input with pull high and interrupt function. The P1.2 can use auto-scan function at stop mode and share with OTP interface CMD_B pin.
27 ~ 31	P1.3 ~ P1.7	B	Programmable I/O pins, CMOS/NMOS output, input with pull high and interrupt function. The P1.3~P1.6 can use auto-scan function at stop mode.

Note: In the “Type” field,
“I” means input only.
“O” means output only.
“B” means bi-direction.
“P” means Power, “G” means Ground.

3.3 Pin Configuration

3.3.1 SOP16

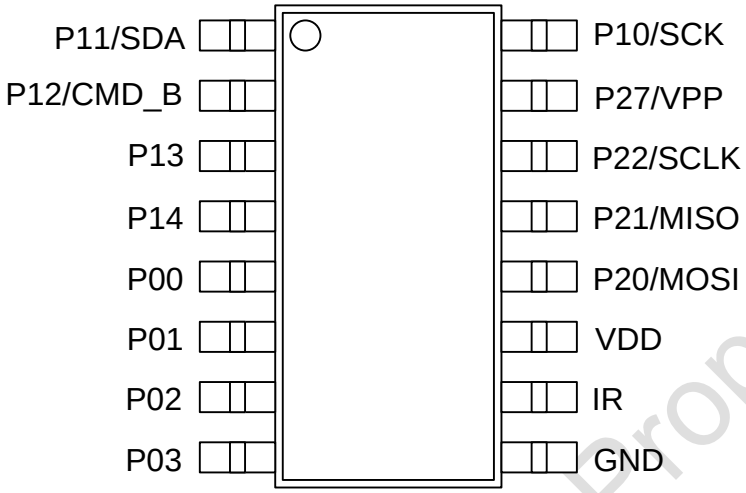


Figure 3-2 MG69P361AS16 Top View

3.3.2 SOP28

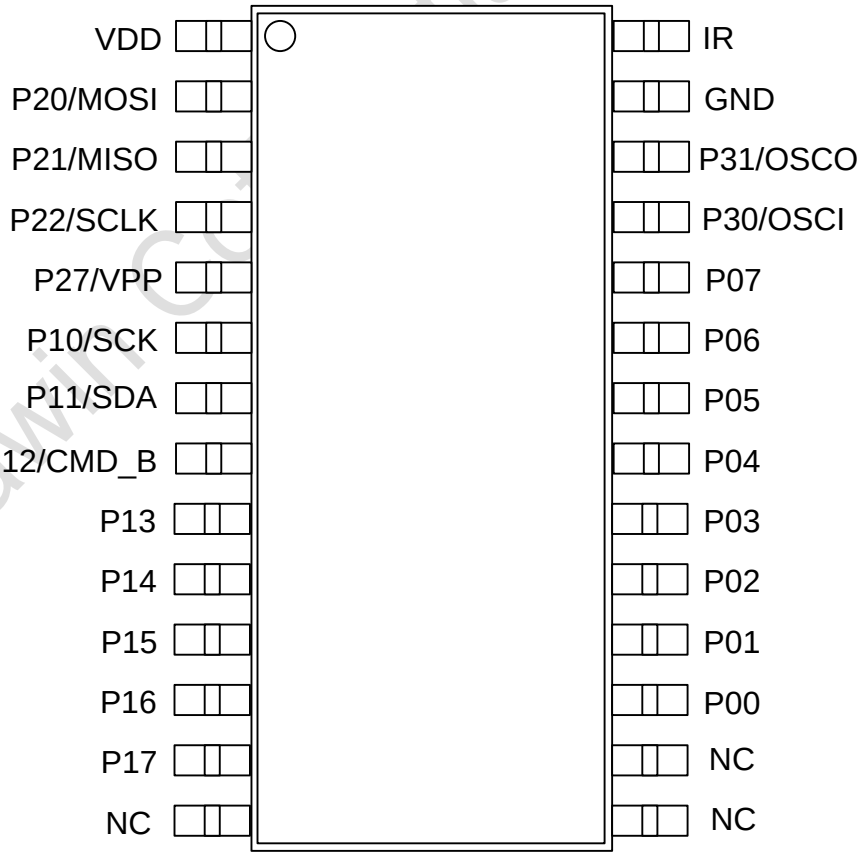


Figure 3-3 MG69P361AS28 Top View

4 Block Diagram

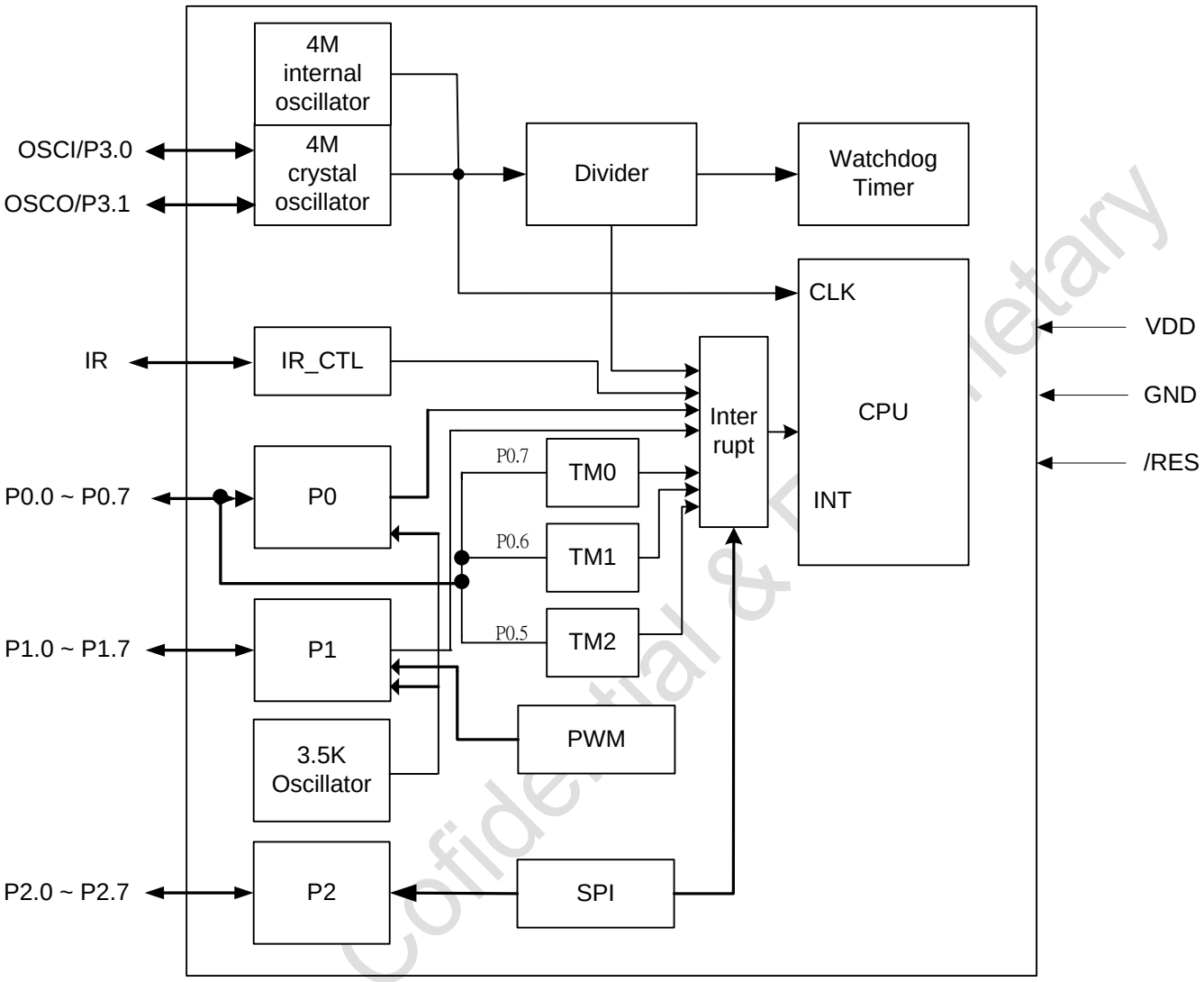


Figure 4-1 Block Diagram

5 Function Description

5.1 Registers

	A
	Y
	X
	P
PCH	PCL
1	S

5.2 Accumulator

The accumulator is a general-purpose 8-bit register, which stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of two data words used in these operations.

5.3 Index Register(X,Y)

There are two 8-bit index registers (X and Y), which may be used to count program steps or to provide an index value to be used in generating an effective address. When executing an instruction, which specifies indexed addressing, the CPU fetches the OP Code and the base address, and modifies the address by adding the index register to it prior to performing the desired operation. Pre- or post-index of index address is possible.

5.4 Processor Status Register

The 8-bit processor status register contains seven status flags. Some of the flags are controlled by the program, others may be controlled both the program and the CPU.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N	V	1	B	D	I	Z	C

N: Signed flag, 1 = negative, 0 = positive
V: Overflow flag, 1 = true, 0 = false
B: BRK interrupt command, 1 = BRK, 0 = IRQB
D: Decimal mode, 1 = true, 0 = false
I: IRQB disable flag, 1 = disable, 0 = enable
Z: Zero flag, 1 = true, 0 = false
C: Carry flag, 1 = true, 0 = false

5.5 Program Counter(PC)

The 16-bit program counter register provides the addresses, which step the micro-controller through sequential program instructions. Each time the micro-controller fetches an instruction from program memory, the lower byte of the program counter (PCL) is placed on the low-order 8 bits of the address bus and the higher byte of the program counter (PCH) is placed on the high-order 8 bits. The counter is incremented each time an instruction or data is fetched from program memory.

5.6 Stack Point(S)

The stack pointer is an 8-bit register, which is used to control the addressing of the variable-length stack. The stack pointer is automatically incremented and decremented under control of the micro-controller to perform stack manipulations under direction of either the program or interrupts (/NMI or /IRQ). The stack allows simple implementation of nested subroutines and multiple level interrupts. The stack pointer is initialized by the user's firmware.

6 Memory Organization

There are 256 bytes SRAM in MG69P361A. They are working RAM (0000H to 00BFH) and stacks (0100H to 01FFH) . The address 0100H to 1BFH are shared with address 0000H to 00BFH. The address 00C0H to 00FFH are special function registers area. Bit-manipulation instruction is available on SRAM except SFR.

There are 128K bytes program/data ROM in MG69P361A. It is combined with 32K program/data ROM and bank switching data ROM. The ROM address from 8000H to FFFFH can store program and other data. There are six banks in MG69P361A that is index by SFR. The default bank number is 00H after power on or reset. The bank select function, ranged from 4000H to 7FFFH (16Kbyte/bank), is used for extending memories if the ROM size is more than 32K bytes in MG69P361A. The address mapping of MG69P361A is shown as below.

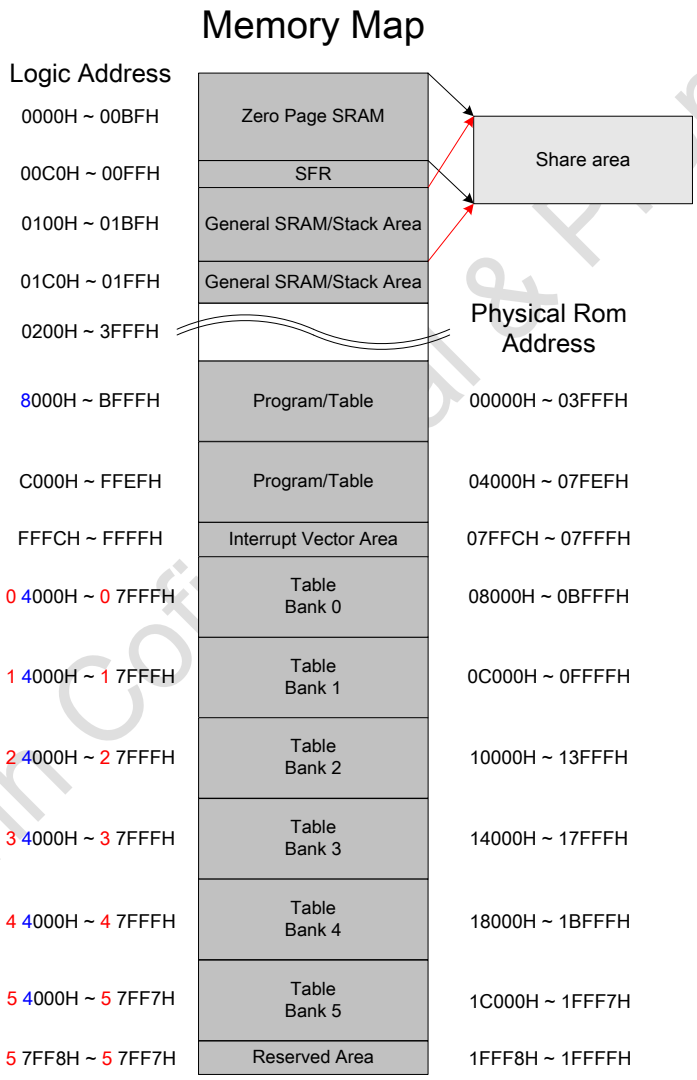


Figure 6-1 Memory Map

6.1 SFR Mapping

The addresses 00C0H to 00FFH are reserved for special function registers (SFR). The SFR is used to control or store the status of I/O, system clock and other peripheral.

※ All SFRs are not supported by bit-manipulation instructions.

※Please initialize all the SFRs after power-on.

Table 6-1 SFR Table

SFR (special function register): 00C0H~00FFH

Address	Content	Default	Address	Content	Default
00C0	RESOK	--------	00D0		
00C1			00D1	P0obuf(W)	11111111
				P0pad(R)	XXXXXXXX
00C2	IRQen	00000000	00D2	P0dir	00000000
00C3	EVTflag0/EVTclrb0	00000000	00D3	P0plh	11111111
00C4	EVTflag1/EVTclrb1	-X0-----	00D4	P0opd	00000000
00C5	TM2L	11111111	00D5		
00C6	TM2H	11111111	00D6	P1obuf(W)	11111111
				P1pad(R)	XXXXXXXX
00C7	TM2_CTL	000---00	00D7	P1dir	00000000
00C8	TM0	11111111	00D8	P1plh	11111111
00C9	TM0_CTL	00000000	00D9	P1opd	00000000
00CA	TM0_CAP	00000000	00DA		
00CB	TM0_CAPB	11111111	00DB	P2port(W)	11111111
				P2port(R)	XXXXXXXX
00CC	TM1	11111111	00DC		
00CD	TM1_CTL	000---00	00DD	P2plh	11111111
00CE			00DE	P2opd	11111111
00CF			00DF		

Address	Content	Default	Address	Content	Default
00E0	P3port(W)	------11	00F0	BANK	-----000
	P3port(R)	------XX			
00E1			00F1		
00E2			00F2		
00E3	P3mode	------11	00F3		
00E4			00F4		
00E5			00F5		
00E6			00F6		
00E7	IRO_CTL	00000000	00F7		
00E8	CMP_CTL	-------0	00F8		
00E9	SIDAT	00000000	00F9	CWPR	XXXXXXXX
00EA	SPI_CTL	000-----	00FA		
00EB			00FB	TKSCAN	1111XXXX
00EC			00FC	PWR_CR	-000---0
00ED	PWM_CTL	00111111	00FD		
00EE	PWM0	10000000	00FE	DIVlow	00000000
00EF	PWM1	10000000	00FF	DIVhigh	00000000

6.2 Condition Write Protect Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00F9H	CWPR	PT7	PT6	PT5	PT4	PT3	PT2	PT1	PT0	-	√

Condition Write Protect Register (CWPR) is used to protect WDT(EVTclrb1.bit5), OSCenb(PWR_CR.bit0), IORS(PWR_ CR.bit6) and BANK.

If users want to change WDT(EVTclrb1.bit5), OSCenb(PWR_CR.bit0), IORS(PWR_ CR.bit6) and BANK. The CWPR musts write “BEH”.

PT7~PT0: Write Protect Pattern. In MG69P361A write protect pattern is “BEH”.

Note:

1. *When CWPR is written by firmware, it would be automatically cleared by hardware after the “next write action” of firmware.*

※ Bit-manipulation instructions are not available on this register.

7 Interrupt

The MG69P361A provides 8 interrupt sources: port0, port1, Timer0, Timer1, Timer2, IRI, SPI and divider. Each of the Interrupt sources can be individually enabled or disabled by setting or clearing a bit in the IRQen and EVTclrb0. Eight interrupts share the interrupt vector FFFEH/FFFFH.

Table 7-1 Interrupt Vector Table

Vector Address	Item	Flag	Properties	Memo
FFFCH, FFFDH	POR	None	Ext.	Power-on reset
"	WDT	EVTflag1.5	Int.	Watchdog reset
"	LVR	None	Ext.	Low voltage reset
	EXT. reset	None	Ext.	/RES pad reset
FFFEH, FFFFH	P0	EVTflag0.0	Ext.	Port P0 interrupt vector
"	TM2	EVTflag0.1	Int.	TM2 underflow interrupt
"	TM1	EVTflag0.2	Int.	TM1 underflow interrupt
"	TM0	EVTflag0.3	Int.	TM0 underflow interrupt
"	DIV	EVTflag0.4	Int.	Divider carry out interrupt
"	P1	EVTflag0.5	Ext.	Port P1 interrupt vector
"	SPI	EVTflag0.6	Int.	SPI finished RX and RX data
"	IRI	EVTflag0.7	Int.	IRI interrupt vector

P0 interrupt: IRQen.0 (P0en) = 1 and EVTflag0.0 = 1.
TM2 interrupt IRQen.1 (TM2en) = 1 and EVTflag0.1 = 1.
TM1 interrupt IRQen.2 (TM1en) = 1 and EVTflag0.2 = 1.
TM0 interrupt IRQen.3 (TM0en) = 1 and EVTflag0.3 = 1.
DIV interrupt: IRQen.4 (DIVen) = 1 and EVTflag0.4 = 1.
P1 interrupt: IRQen.5 (P1en) = 1 and EVTflag0.5 = 1.
SPI interrupt IRQen.6 (SPIen) = 1 and EVTflag0.6 = 1.
IRI interrupt IRQen.7 (IRIen) =1 and EVTflag0.7 =1

7.1 Interrupt Register

IRQ enable flag

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C2H	IRQen	IRIen	SPIen	P1en	DIVen	TM0en	TM1en	TM2en	P0en	-	√

Program can enable or disable the ability of triggering IRQ through this register.
0: Disable (default "0" at initialization)
1: Enable
P0en: Falling edge occurs at port 0 (input mode)
P1en: Falling edge occurs at port 1 (input mode)
TM1en-:Timer1 underflow occurred
TM0en-:Timer0 underflow occurred
DIVen: DIV interrupt frequency occurred
P1en: Falling edge occurs at port 1 (input mode)
SPIen: SPI finished RX and RX data
IRIen: edge occurs at IRI

Event status flag 0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C3H	EVTflag0	IRI	SPI	P1	DIV	TM0	TM1	TM2	P0	√	-

When IRQ occurs, program can read this register to know which source triggering IRQ.
P0:P0 interrupt flag. Set by falling edge on any pin of port0. Clear by software.
TM2:Timer2 underflow flag. Clear by software.
TM1:Timer1 underflow flag. Clear by software.
TM0:Timer0 underflow flag. Clear by software.
DIV: Divider interrupts flag. Clear by software.
P1:P1 interrupt flag. Set by falling edge on any pin of port1. Clear by software.
SPI: SPI finished RX and RX data flag Clear by software.
IRI:IRI interrupt flag. Set by falling and rising edge on IRI (set by TM0_CTL.3). Clear by software.

Event clear flag 0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C3H	EVTclrb0	IRI	SPI	P1	DIV	TM0	TM1	TM2	P0	-	√

Program can clear the interrupt event by writing '0' into the corresponding bit.

Event status flag 1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C4H	EVTflag1	-	LVD	WDT	-	-	-	-	-	√	-

Program can read this register to know LVD and WDT occur.
LVD: Low voltage detected. 1:V_{DD} is under 2.4V. 0:V_{DD} is above 2.4V. It is set by hardware and clear by software.
WDT: WDT time-out flag. Clear flag and WDT counter by software.

Event clear flag 1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C4H	EVTclrb1	-	LVD	WDT	-	-	-	-	-	-	√

Program can clear the flag by writing '0' into the corresponding bit.

※ EVTclrb1.5 (WDT) is protected by CWPR.

7.2 Interrupt System

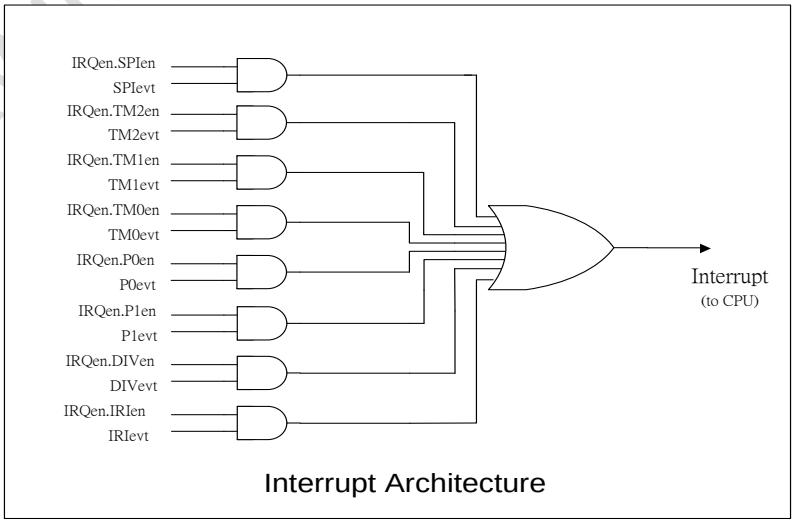
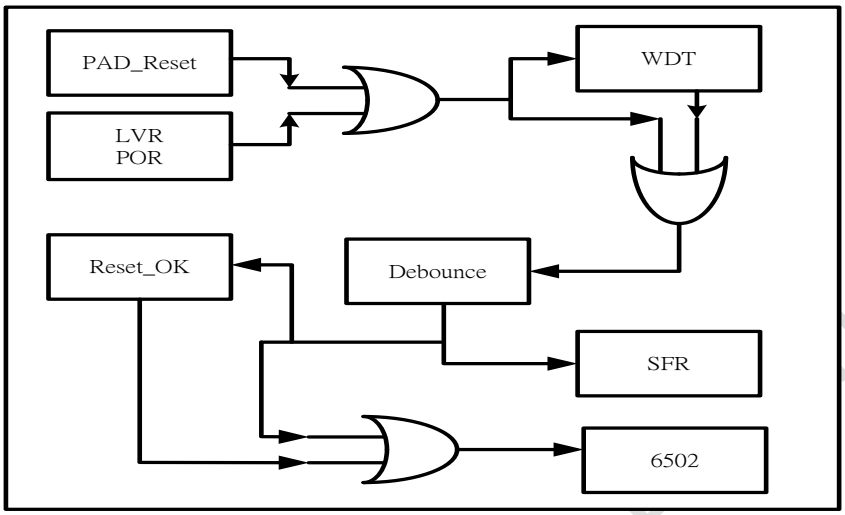


Figure 7-1 Interrupt System Diagram

8 Reset

MG69P361A have 5 kinds of Reset (PAD Reset、LVR、POR、WDT and RESET OK). The Chip reset Circuit shown below:



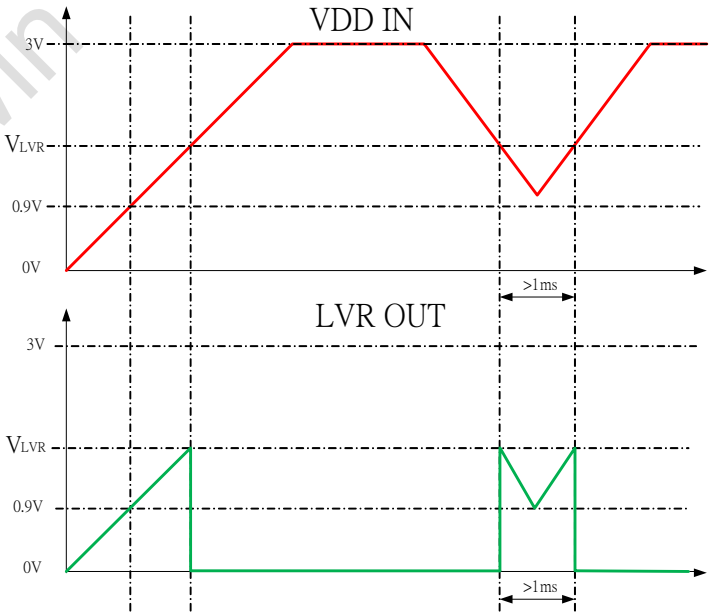
8.1 Low Voltage Reset(LVR)

The MG69P361A provides low voltage reset circuit in order to monitor the supply voltage of the device. If the supply voltage of the device is within the range 0.9V ~ VLVR , such as changing a battery, the LVR will automatically reset the device internally.

The LVR includes the following specifications:

1. The low voltage (0.9V~VLVR) has to remain in its original state to exceed 1ms. If the low voltage state does not exceed 1ms, the LVR will ignore it and do not perform a reset function.

2. In the LVR mode, the on-chip oscillator is stopped and the on-chip SRAM is held. Port0, Port1, Port2, Port3 set to floating, IR sets to output high.



8.2 Watchdog Timer(WDT)

Watchdog Timer (WDT, The example is based on 4MHz) Unit : Hz

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
WDTlow	3.8	7.6	15.2	30.5	61	122	244.1	488.2	-	-
Name								Bit 8	R	W
WDThigh	-	-	-	-	-	-	-	1.9	-	-

The watchdog timer time-out period is obtained by the equation: (Fosc / 4096) /512 or (Fscan / 4) /512. Before watchdog timer time-out occurs, the program must write BEH to CWPR then clear the 9-bit WDT timer by writing 0 to EVTclrb1.5 at next write OP code. WDT overflow will cause system reset and set EVTflag1.5 to high. WDT will reset by LVR, POR and PAD_RESET.

※ EVTclrb1.5 (WDT) is protected by CWPR.

```
Example:
clear_WDT .macro
        sei
        lda    #BEH
        sta    CWPR          ;;(F9h)
        lda    #DFH
        sta    EVTclrb1      ;;(C4h)
        cli
.endm
```

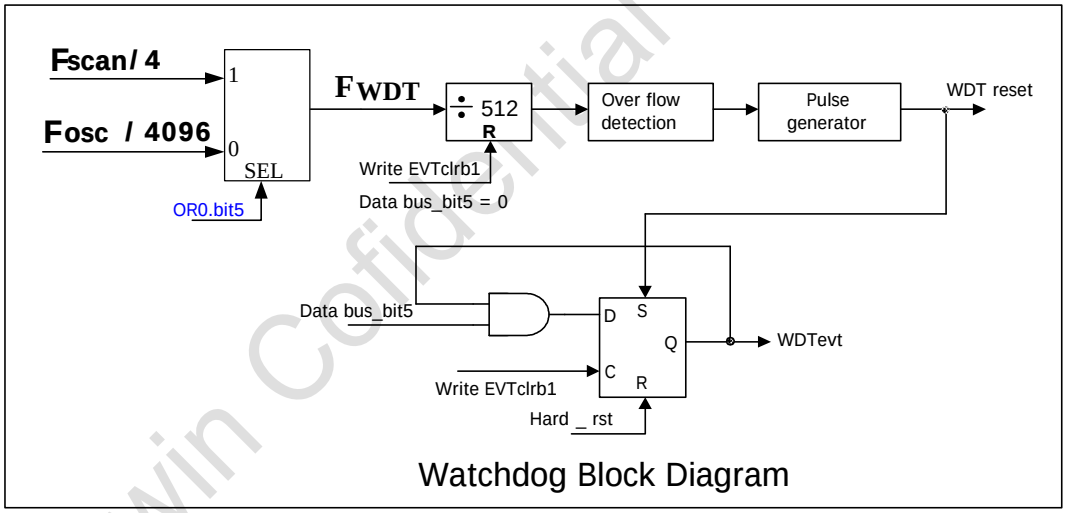


Figure 8-1 Watch Dog Diagram

8.3 Reset OK

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C0H	RESOK	RK7	RK6	RK5	RK4	-	-	-	-	-	√

RESOK (Reset OK): If the device reset OK and work well, **must** write #$90 into this register.
For example:

```
Program_start:    LDA   #10010000b
                  STA   $C0
```

8.4 Programming Notice

The status after different reset condition is listed below:

	Power on reset	CPU /RES pin reset
SRAM Data	Unknown	Unchanged
CPU Register	Unknown	Unknown
Special Function Register	Default value	Default value

9 Power Control Register

9.1 Power Saving Control

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00FCH	PWR_CR	-	IORS	DIVS1	DIVS0	-	-	-	OSCenb	-	√

OSCenb: 0: The oscillator is free run.
1: The oscillator is frozen (stop mode).

DIVS0, DIVS1: Divider interrupt frequency selector
00: The Fosc/16384 interrupt frequency is selected
01: The Fosc/8192 interrupt frequency is selected
10: The Fosc/4096 interrupt frequency is selected
11: The Fosc/2048 interrupt frequency is selected

IORS: IO reset source selector.
0: IO SFR will be reset by POR, LVR, external reset and WDT reset.
1: IO SFR will be reset by POR, LVR, and external reset.

※ OSCenb and IORS are protected by CWPR.

10 Divider

10.1 Divider

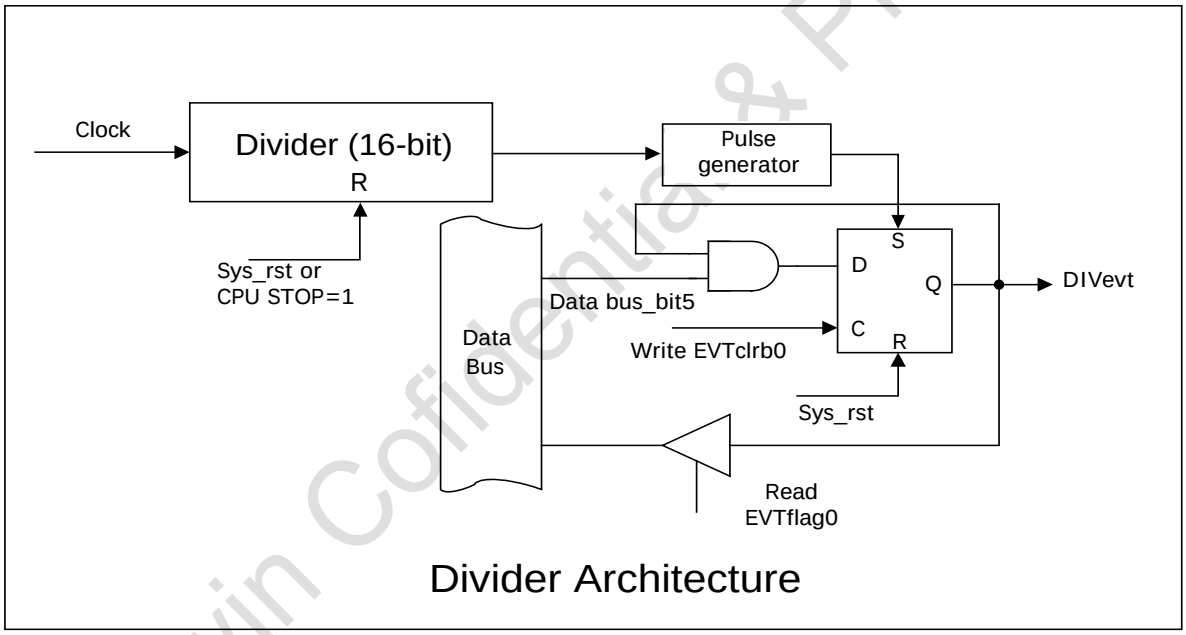
DIV interrupt selector

Divider (The example is base on 4MHz) Unit : Hz

Address	Name	/256	/128	/64	/32	/16	/8	/4	/2	R	W
00FEH	DIVlow	15625	31250	62500	125000	250000	500000	1000000	2000000	√	-
Address	Name	/65536	/32768	/16384	/8192	/4096	/2048	/1024	/512	R	W
00FFH	DIVhigh	61	122	244	488	976	1953	3906	7812	√	-

The time-out period is obtained by the equation:

PWR_CR.DIVS1	PWR_CR.DIVS0	DIV interrupt occurs status
0	0	F_{osc} / 16384
0	1	F_{osc} / 8192
1	0	F_{osc} / 4096
1	1	F_{osc} / 2048



Divider Architecture

11 Timer

11.1 Timer0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C8H	TM0	T7	T6	T5	T4	T3	T2	T1	T0	√	√
00C9H	TM0_CTL	STC	RL/S	TKES	CPS	CTKS	DTY	TKI1	TKI0		√
00CAH	TM0_CAP	CP7	CP6	CP5	CP4	CP3	CP2	CP1	CP0	√	
00CBH	TM0_CAPB	CPB7	CPB6	CPB5	CPB4	CPB3	CPB2	CPB1	CPB0	√	

※ Bit-manipulation instructions are not available on this register.

Timer 0 is a 8-bit down-count counter. The counter underflow frequency of timer 0 can be calculated with the equation: $F_{TM0\_UV} = F_{TM0} / (TM0+1)$

TM0:TM0 Counting Value at Read SFR. TM0 Underflow Value setting at writes SFR.

TM0_CAP: Capture TM0 Counting Value.

TM0_CAPB: One's Complement of TM0_CAP.

TM0_CTL:
STC: Start/Stop counting. 1: start and pre-load the value to counter, 0: stop timer clock (set this bit to 1 will be ignored when this bit already set to 1)

RL/S: Auto-reload disable/enable. 1: disable auto-reload, 0: enable auto-reload

TKES: Event or series input clock-in trigger edge selector; 0: rising edge, 1: falling edge

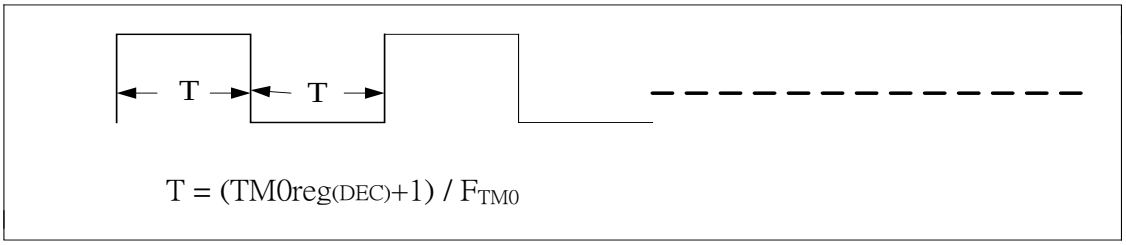
CPS: Capture TM0 Counting Value trigger source select. 1: P1.1, 0: IRI.

CTKS: Capture source trigger edge selector; 0: rising edge, 1: falling edge

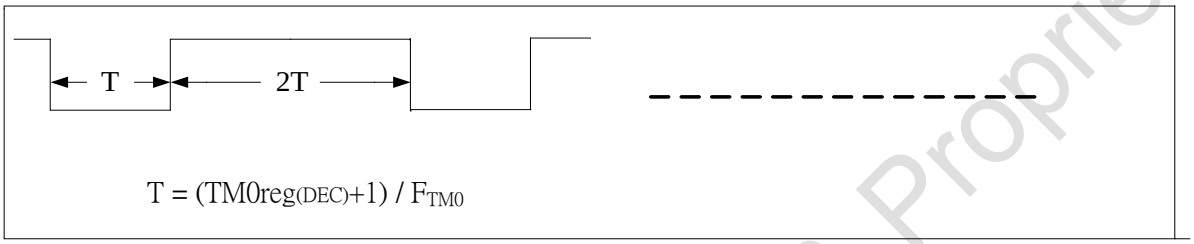
TKI1	TKI0	Selected TM0 input clock source
0	0	Fosc / 1
0	1	Fosc / 4
1	0	P1.0
1	1	TM1 underflow

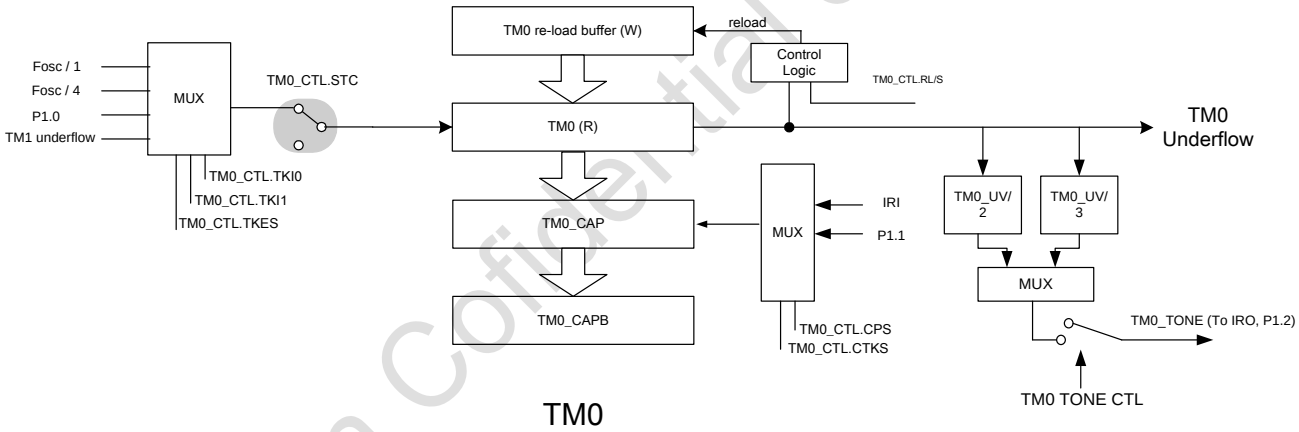
DTY: TM0 tone duty cycle selection

0 : Set Tone duty cycle is 50%(H)/50%(L)



1 : Set Tone duty cycle is 66%(H)/33%(L)





TM0

11.2 Timer1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00CCH	TM1	T7	T6	T5	T4	T3	T2	T1	T0	√	√
00CDH	TM1_CTL	STC	RL/S	TKES	-	-	-	TKI1	TKI0		√

※ Bit-manipulation instructions are not available on this register.

Timer 1 is a 8-bit down-count counter. The counter underflow frequency of timer 1 can be calculated with the equation: $F_{TM1\_UV} = F_{TM1} / (TM1+1)$

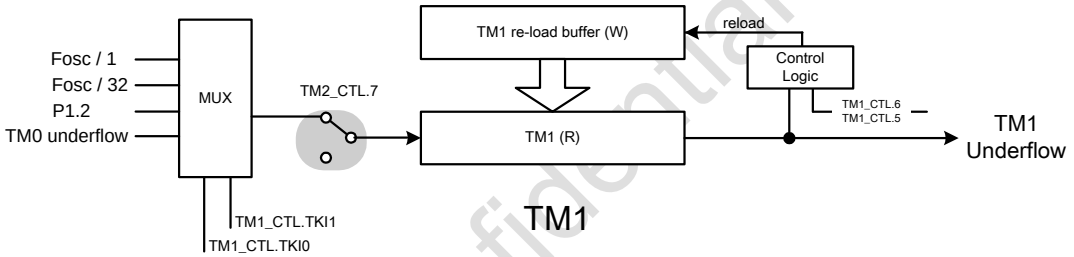
TM1:TM1 Counting Value at Read SFR. TM1 Underflow Value setting at writes SFR.

TM1_CTL:
STC: Start/Stop counting. 1: start and pre-load the value to counter, 0: stop timer clock (set this bit to 1 will be ignored when this bit already set to 1)

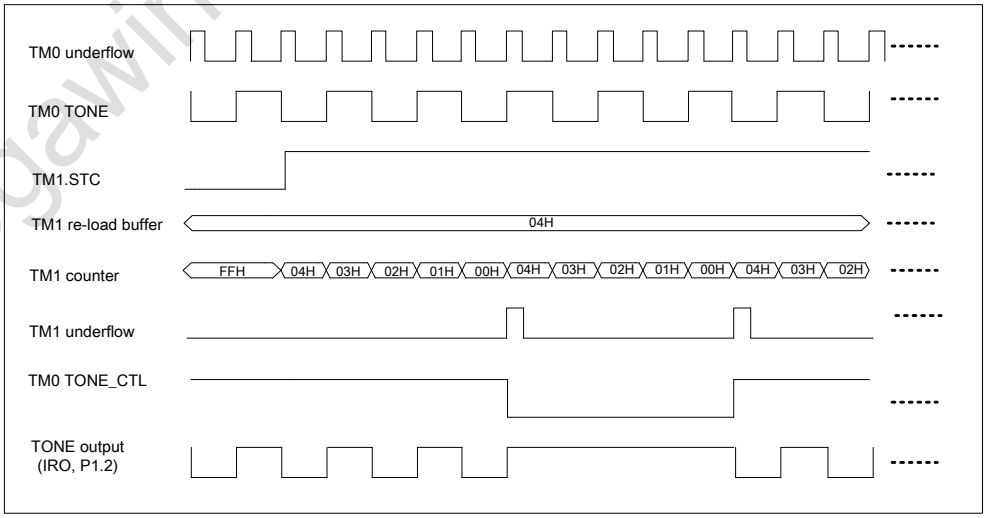
RL/S: Auto-reload disable/enable. 1: disable auto-reload, 0: enable auto-reload

TKES: Event or series input clock-in trigger edge selector; 0: rising edge, 1: falling edge

TKI1	TKI0	Selected TM1 input clock source
0	0	Fosc / 1
0	1	Fosc / 32
1	0	P1.2
1	1	TM0 underflow



When TM1 clock source use TM0 underflow (TKI1, TKI0 = 11H), the TM0 tone output would be controlled by TM0 TONE_CTL



11.3 Timer2

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C5H	TM2L	T7	T6	T5	T4	T3	T2	T1	T0	√	√
00C6H	TM2H	T15	T14	T13	T12	T11	T10	T9	T8	√	√
00C7H	TM2_CTL	STC	RL/S	TKES				TKI1	TKI0		√

※ Bit-manipulation instructions are not available on this register.

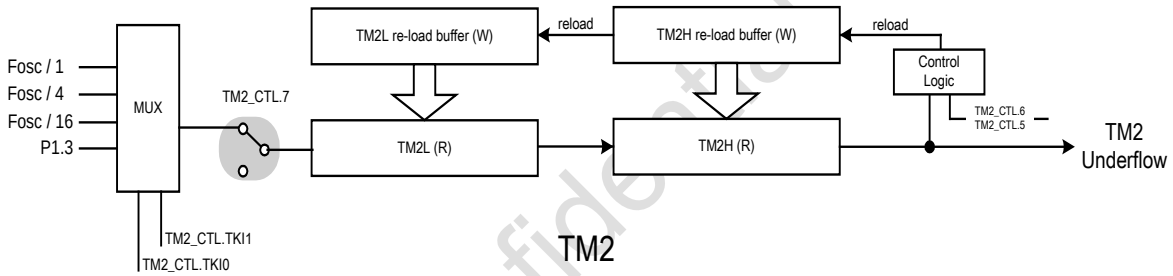
Timer 2 is a 16-bit down-count counter. The counter underflow frequency of timer 2 can be calculated with the equation: $F_{TM2\_UV} = F_{TM2} / (TM2+1)$

TM2_CTL:
STC: Start/Stop counting. 1: start and pre-load the value to counter, 0: stop timer clock (set this bit to 1 will be ignored when this bit already set to 1)

RL/S: Auto-reload disable/enable. 1: disable auto-reload, 0: enable auto-reload

TKES: Event or series input clock-in trigger edge selector; 0: rising edge, 1: falling edge

TKI1	TKI0	Selected TM2 input clock source
0	0	Fosc/1
0	1	Fosc/4
1	0	Fosc/16
1	1	P1.3



12 PWM

12.1 PWM Control Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00EDH	PWM_CTL	PWKS1	PWKS0	PWC12	PWC11	PWC10	PWC02	PWC01	PWC00	-	√

PWKS1, PWKS0: PWM0 and PWM1 clock source selection.

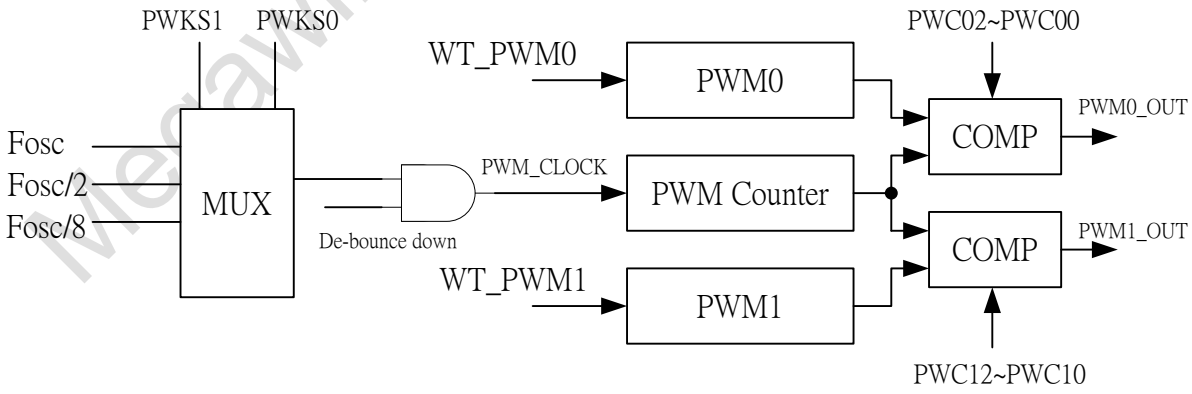
PWKS1	PWKS0	PWM0 clock source	PWM1 clock source
0	0	Fosc / 1	Fosc / 1
0	1	Fosc / 4	Fosc / 4
1	0	Fosc / 8	Fosc / 4
1	1	Fosc / 8	Fosc / 8

PWC02, PWC01, PWC00: PWM0 compare bits selection.

PWC02	PWC01	PWC00	PWM0 counter compare bits							
			Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	-	-	-	-	-	-	-	PW00
0	0	1	-	-	-	-	-	-	PW01	PW00
0	1	0	-	-	-	-	-	PW02	PW01	PW00
0	1	1	-	-	-	-	PW03	PW02	PW01	PW00
1	0	0	-	-	-	PW04	PW03	PW02	PW01	PW00
1	0	1	-	-	PW05	PW04	PW03	PW02	PW01	PW00
1	1	0	-	PW06	PW05	PW04	PW03	PW02	PW01	PW00
1	1	1	PW07	PW06	PW05	PW04	PW03	PW02	PW01	PW00

PWC12, PWC11, PWC10: PWM1 compare bits selection.

PWC12	PWC11	PWC10	PWM1 counter compare bits							
			Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	-	-	-	-	-	-	-	PW10
0	0	1	-	-	-	-	-	-	PW11	PW10
0	1	0	-	-	-	-	-	PW12	PW11	PW10
0	1	1	-	-	-	-	PW13	PW12	PW11	PW10
1	0	0	-	-	-	PW14	PW13	PW12	PW11	PW10
1	0	1	-	-	PW15	PW14	PW13	PW12	PW11	PW10
1	1	0	-	PW16	PW15	PW14	PW13	PW12	PW11	PW10
1	1	1	PW17	PW16	PW15	PW14	PW13	PW12	PW11	PW10



12.2 PWM0 Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00EEH	PWM0	PW07	PW06	PW05	PW04	PW03	PW02	PW01	PW00	√	√

The PWM0 clock source frequency is controlled by PWCTL_bit7 and PWCTL_bit6. P1.3/PWM pins produce PWM output. The PWM output duty is proportional to the code value of data buffer. Default is 1000 0000B

12.3 PWM1 Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00EFH	PWM1	PW17	PW16	PW15	PW14	PW13	PW12	PW11	PW10	√	√

The PWM1 clock source frequency is controlled by PWCTL_bit7 and PWCTL_bit6. P1.4/PWM pins produce PWM output. The PWM output duty is proportional to the code value of data buffer. Default is 1000 0000B

13 SPI

13.1 SPI Data Rx and Tx Buffer Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E9H	SIDAT:SPI_MOSI	(MSB)							(LSB)	-	√
00E9H	SIDAT:SPI_MISO	(MSB)							(LSB)	√	-

Write data to this SFR will start transfer data to serial output pad. (SPI_MOSI)
Read data from this SFR will always read data from serial input pad. (SPI_MISO)

SPI_MOSI: P2.0
SPI_MISO: P2.1
SPI_SCLK: P2.2
SPI_CS: software define by user

13.2 SPI Control Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00EAH	SPI_CTL	SPIEN	SCLK	DORD	-	-	-	-	-	√	√

Bit7 : SPIEN – SPI Mode Enable/Disable Control Register.
0 : Disable. (Default)
1 : Enable.

Bit6 : SCLK -- SPI Clock Select.
0 : 1MHz bit rate. (Default) 4MHz/4
1 : 500KHz bit rate. 4MHz/8

Bit5 : DORD, SPI data order.
0 : The MSB of the data byte is transmitted first.(Default)
1 : The LSB of the data byte is transmitted first.

14 Configurable I/O Ports

14.1 Port 0

P0.7~P0.0 have scan-key function in stop mode.

Port 0 Output Buffer

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D1H	P0obuf	P07	P06	P05	P04	P03	P02	P01	P00	-	√

When port0.n is configured as an output pin, the port0.n pin would output from the P0obuf.

※ Bit-manipulation instructions are not available on this register.

Port 0 Pad

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D1H	P0pad	P07	P06	P05	P04	P03	P02	P01	P00	√	-

When the P0.n is configured as output mode, reading P0pad.n would always read logic '1'.
When the P0.n is configured as input mode, reading P0pad.n would always read the logic value from pad.

※ Bit-manipulation instructions are not available on this register.

Port 0 Direction Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D2H	P0dir	DR7	DR6	DR5	DR4	DR3	DR2	DR1	DR0	-	√

P0dir.n = 0: P0.n is configured as an input pin. (Default)
1: P0.n is configured as an output pin.

※ Bit-manipulation instructions are not available on this register.

Port 0 Pull-high Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D3H	P0plh	PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0	-	√

PH0 ~ PH7: These control bits are used to enable the pull-high of P0.0 ~ P0.7 pin.
P0plh.n = 0: Disable internal pull-high
1: Enable internal pull-high

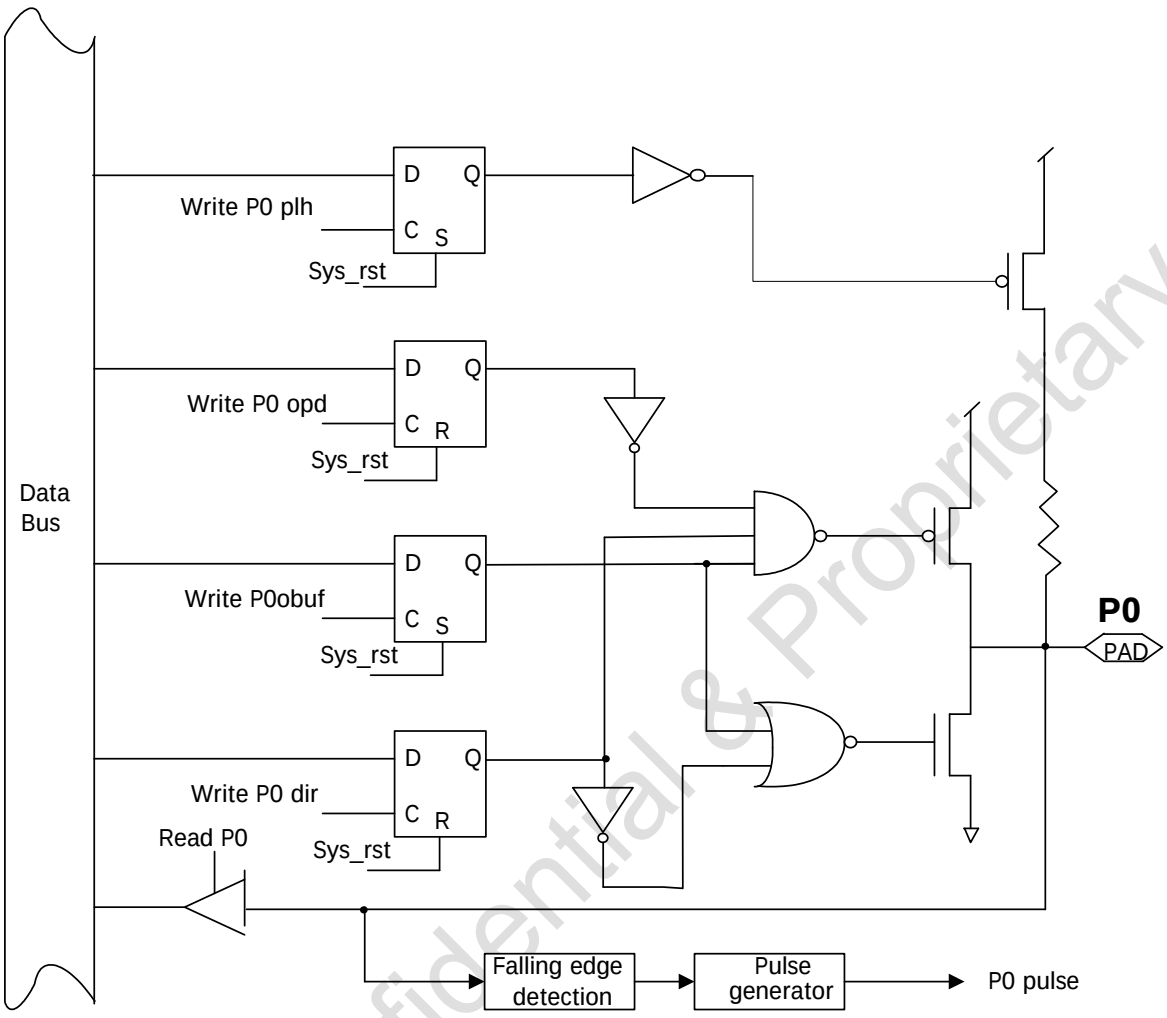
※ Bit-manipulation instructions are not available on this register.

Port 0 Open-drain Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D4H	P0opd	OD7	OD6	OD5	OD4	OD6	OD5	OD1	OD0	-	√

OD0 ~ OD7: These control bits are used to enable the open-drain of P0.0 ~ P0.7 pin.
P0opd.n = 0: Disable open-drain output (CMOS output)
1: Enable open-drain output (NMOS output)

※ Bit-manipulation instructions are not available on this register.



Port 0 Structure

14.2 Port 1

P1.6~P1.0 have scan-key function in stop mode.

Port 1 Output Buffer

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D6H	P1obuf	P17	P16	P15	P14	P13	P12	P11	P10	-	√

When port1.n is configured as an output pin, the port1.n pin would output from the P1obuf.

※ Bit-manipulation instructions are not available on this register.

Port 1 Pad

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D6H	P1pad	P17	P16	P15	P14	P13	P12	P11	P10	√	-

When the P1.n is configured as output mode, reading P1pad.n would always read logic '1'.
When the P1.n is configured as input mode, reading P1pad.n would always read the logic value from pad.

※ Bit-manipulation instructions are not available on this register.

Port 1 Direction Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D7H	P1dir	DR7	DR6	DR5	DR4	DR3	DR2	DR1	DR0	-	√

P1dir.n = 0: P1.n is configured as an input pin.
1: P1.n is configured as an output pin. (Default)

※ Bit-manipulation instructions are not available on this register.

Port 1 Pull-high Control Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D8H	P1plh	PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0	-	√

PH0 ~ PH7: These control bits are used to enable the pull-high of P1.0 ~ P1.7 pin.
P1plh.n = 0: Disable internal pull-high
1: Enable internal pull-high

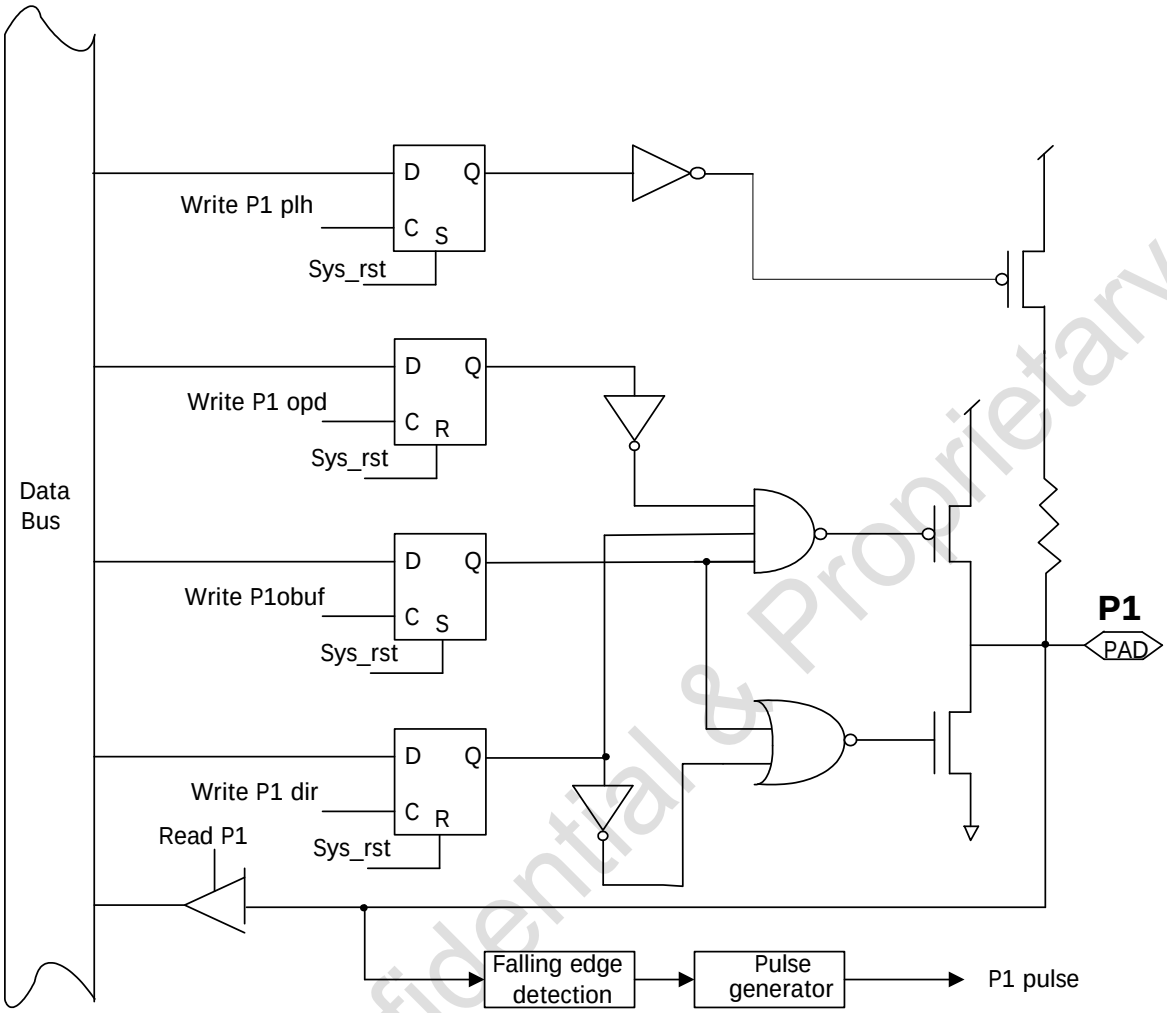
※ Bit-manipulation instructions are not available on this register.

Port 1 Open-drain Control Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D9H	P1opd	OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0	-	√

OD0 ~ OD7: These control bits are used to enable the open-drain of P1.0 ~ P1.7 pin.
P1opd.n = 0: Disable open-drain output (CMOS output)
1: Enable open-drain output (NMOS output)

※ Bit-manipulation instructions are not available on this register.



Port 1 Structure

14.3 Port 2

Port 2 Port

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00DBH	P2port	P27	P26	P25	P24	P23	P22	P21	P20	√	√

Port2 is an 8-bit bi-directional NMOS/CMOS output with internal pull-high resistors selection I/O pins. This register is used to buffer out value of P2.0 ~ P2.7. Reading P2.n would always read logic value from pad.

※ Bit-manipulation instructions are not available on this register.

Port 2 Pull-high Control Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00DDH	P2plh	PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0	-	√

PH0 ~ PH7: These control bits are used to enable the pull-high of P2.0 ~ P2.7 pin.
P2plh.n = 0: Disable internal pull-high
1: Enable internal pull-high

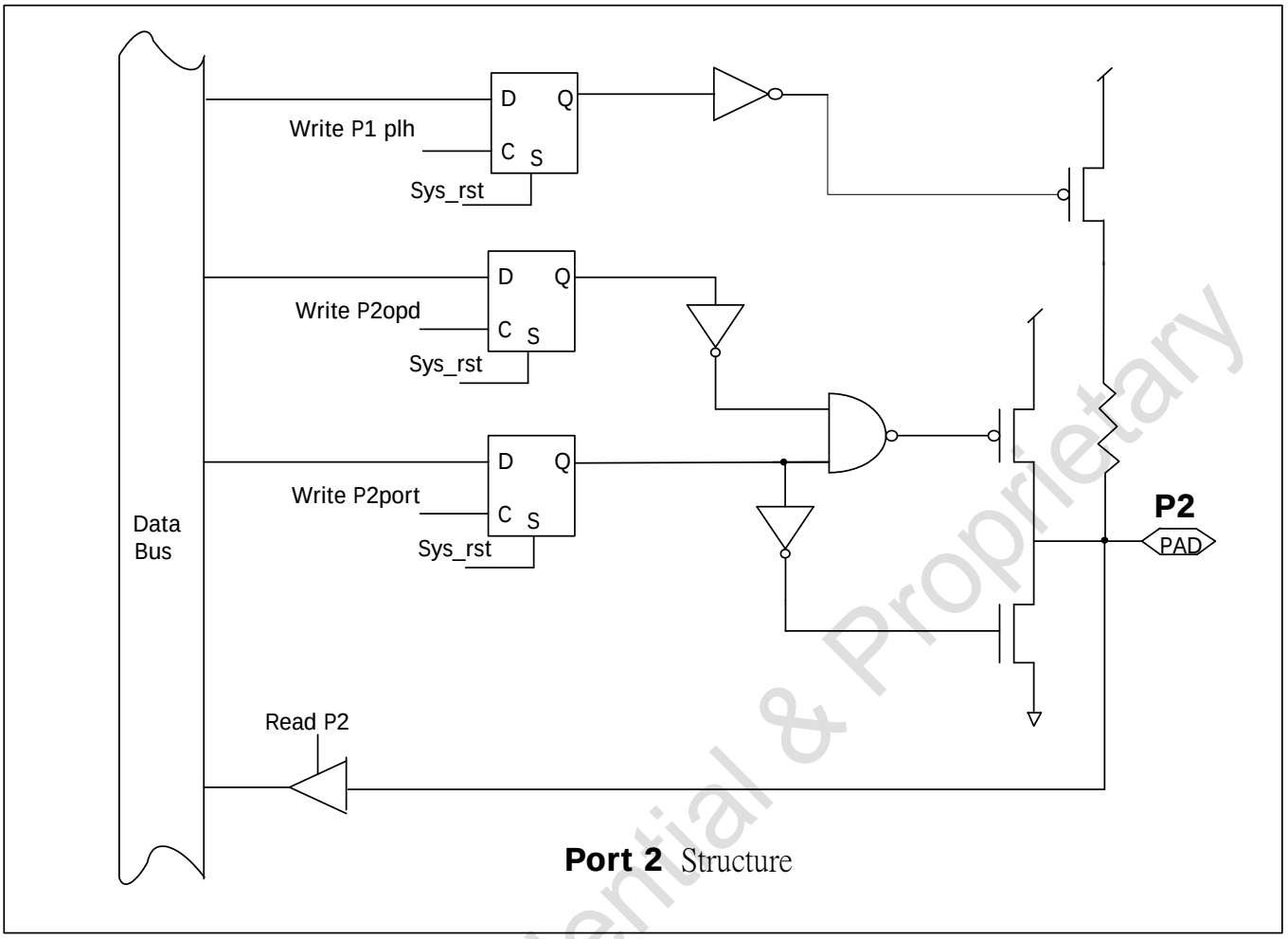
※ Bit-manipulation instructions are not available on this register.

Port 2 Open-drain Control Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00DEH	P2opd	OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0	-	√

OD0 ~ OD7: These control bits are used to enable the CMOS function of P2.0 ~ P2.7 pin.
P2od.n = 0: CMOS output
1: Open-drain

※ Bit-manipulation instructions are not available on this register.



Port 2 Structure

14.4 Port 3

Port 3 Port

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E0H	P3pad	-	-	-	-	-	-	P31	P30	√	√

Port3 is a 2-bit bi-directional NMOS/CMOS output with internal pull-high resistors selection I/O pins. This register is used to buffer out value of P3.0 ~ P3.1. Reading P3.n would always read logic value from pad.

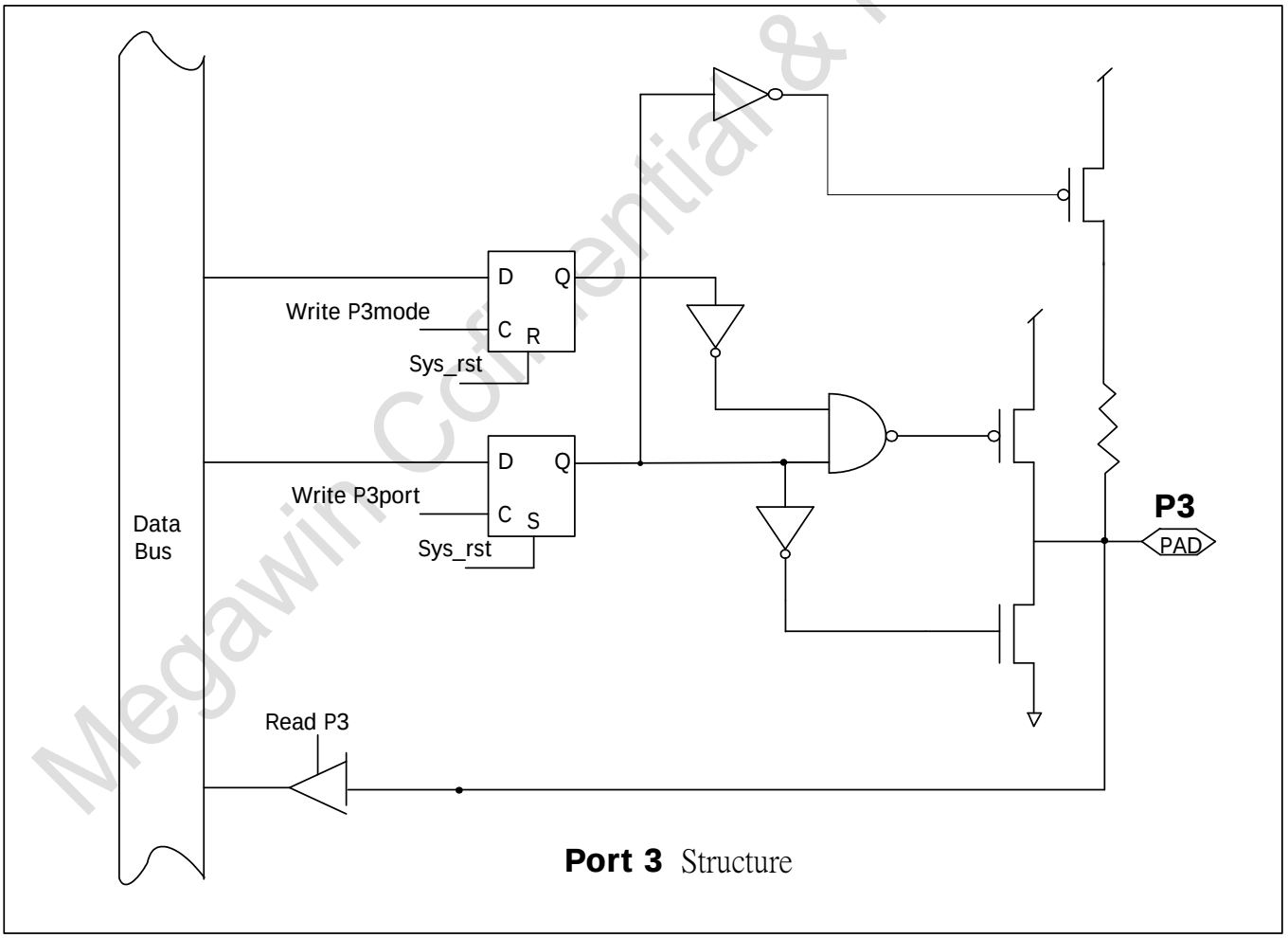
※ Bit-manipulation instructions are not available on this register.

Port 3 Open-drain Control Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E3H	P3mode	-	-	-	-	-	-	MD1	MD0	-	√

MD0 ~ MD1: These control bits are used to enable the CMOS funcrion of P3.0 ~ P3.1 pin.
P3nd.n = 0: CMOS output
1: Open-drain with pull-high resistor output

※ Bit-manipulation instructions are not available on this register.



Port 3 Structure

14.5 TK-Scan

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00FBH	TKSCAN	CI3	CI2	CI1	CI0	SO3	SO2	SO1	SO0	√	-

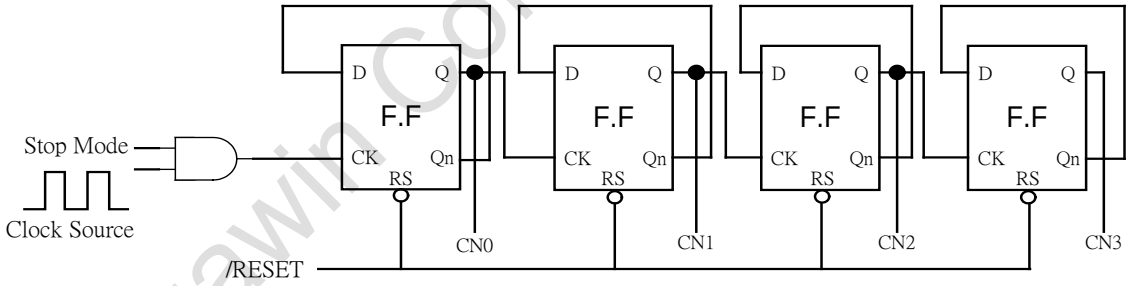
MG69P361A build-In Low Speed I/O scan timer. It can be read value by Scan SFR. And Write to SFR by scan-key hard way.
In Stop Mode, the P0.0~P0.7 or P1.0~P1.6 scan bit = 1. P0.n or P1.n is scan by Low speed ROSC. It will be output low to Pad. Use auto-scan architecture, when any key is press. uC will Wake-up by P0.n or P1.n and keep scan out key to SO0~SO3, capture scan in key to CI0~CI3. Read CI0~CI3 and SO0~SO3 to Decoder which Key is press. It will be clear by Hardware Reset.

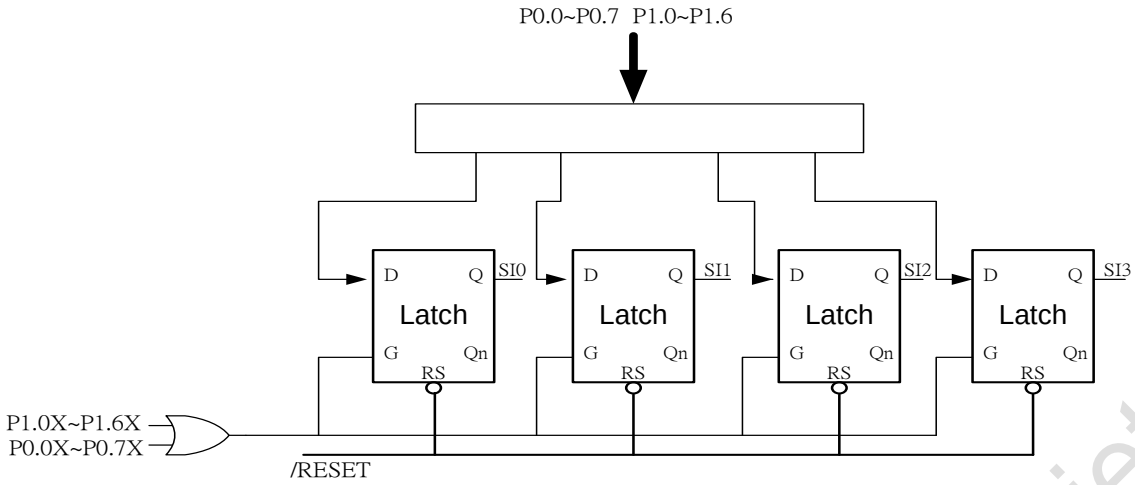
The scan output mapping table is shown as below

SO3 ~ SO0 Output Code	Output Low I/O Pin
0000	P0.0
0001	P0.1
0010	P0.2
…	…
1101	P1.5
1110	P1.6

The capture input mapping table is shown as below

CI3 ~ CI0 Output Code	Output Low I/O Pin
0000	P0.0
0001	P0.1
0010	P0.2
…	…
1101	P1.5
1110	P1.6





14.6 IR

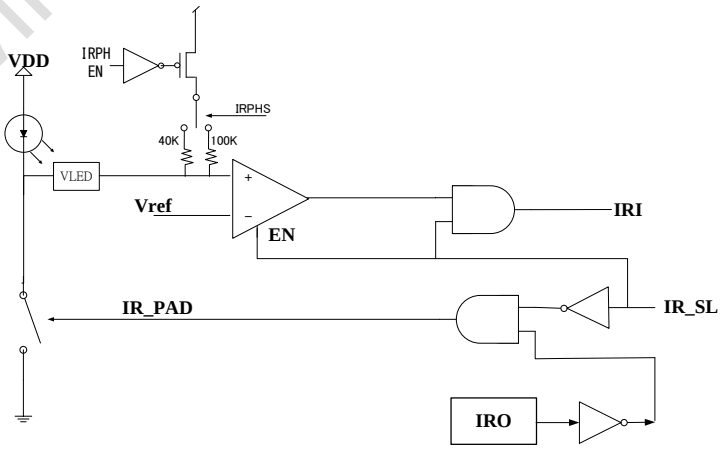
IR Control & IR Buffer

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E7H	IR_CTL	IRO	IRPHEN	IRPHS	PS4	PS3	PS2	PS1	IR_SL	-	√
00E7H	IR_CTL	IRI	-	-	-	-	-	-	-	√	-

※ Bit-manipulation instructions are not available on this register.

IR_CTL is an IR in and out control circuit.
IR_SL: IR PAD output mode or input mode select. 1: input mode , 0: output mode.
PS1: IR_PAD value (IR_SL=out) is: “0” → IRO , “1”→ TIMER0 TONE
PS2: P1.2 PAD value (P1dir.2=out) is : “0” →P1obuf.2, “1”→ TIMER0 TONE
PS3: P1.3 PAD value (P1dir.3=out) is “0” →P1obuf.3, “1”→ PWM0 OUT
PS4: P1.4 PAD value (P1dir.4=out) is “0” →P1obuf.4, “1”→ PWM1 OUT

IRPHEN: IR pull-high resistor enable control, 0 : Disable, 1 : Enable
IRPHS : IR pull-high resistor selector, 0 : 40K ohms, 1 : 100K ohms
IRO: The IR pin output status in output mode(IR_SL=0) is the inverted value of IR_CTL.7. So, write “1” to bit7 of the IR_CTL.7(IRO) the IR will output low voltage and write “0” to bit7 of the IR_CTL.7(IRO) the IR will output high voltage.
IRI: In input mode IRI can read IR_CTL.7(IRI) logic value from pad after comparator.



IR_CTL

15 Others Register

Bank selection

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00F0H	BANK	-	-	-	-	-	BK2	BK1	BK0	√	√

Program can switch the memory bank through this register. This register in initialized to 000H after power on reset. For more detailed information, please refer to memory map description.

BK2=0, BK1=0, BK0=0 ➔ BANK0
BK2=0, BK1=0, BK0=1➔ BANK1
BK2=0, BK1=1, BK0=0➔ BANK2
BK2=0, BK1=1, BK0=1➔ BANK3
BK2=1, BK1=0, BK0=0➔ BANK4
BK2=1, BK1=0, BK0=1➔ BANK5
BK2=1, BK1=1, BK0=0➔ BANK0
BK2=1, BK1=1, BK0=1➔ BANK0

※ BANK is protected by CWPR.

16 Option Register

OR0 (Option Register 0)

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OR0	-	INT_OSC_SEL	TK-SCAN	LOCK	PDLVR	WDT	-	P3_OSC

Bit6: INT_OSC_SEL
0: Fosc use 3.5K low speed oscillator. (OR0_bit1 must be '1')
1: Fosc use 4MHz. oscillator. (Default)

Bit 5: TK-SCAN
0: disable TK-SCAN function in stop mode.
1: enable TK-SCAN function in stop mode. (Default)

Bit 4: LOCK
0: dump code is locked. (Default)
1: dump code is not locked.

Bit 3: PDLVR
0: power-down LVR circuit in stop mode
1: don't power-down LVR circuit in stop mode (Default)

Bit 2: WDT
0: disable WDT function.
1: enable WDT function. (Default)

Bit 0: P3_OSC
0: disable internal oscillator.
1: enable internal oscillator. (default)

17 Application Circuit

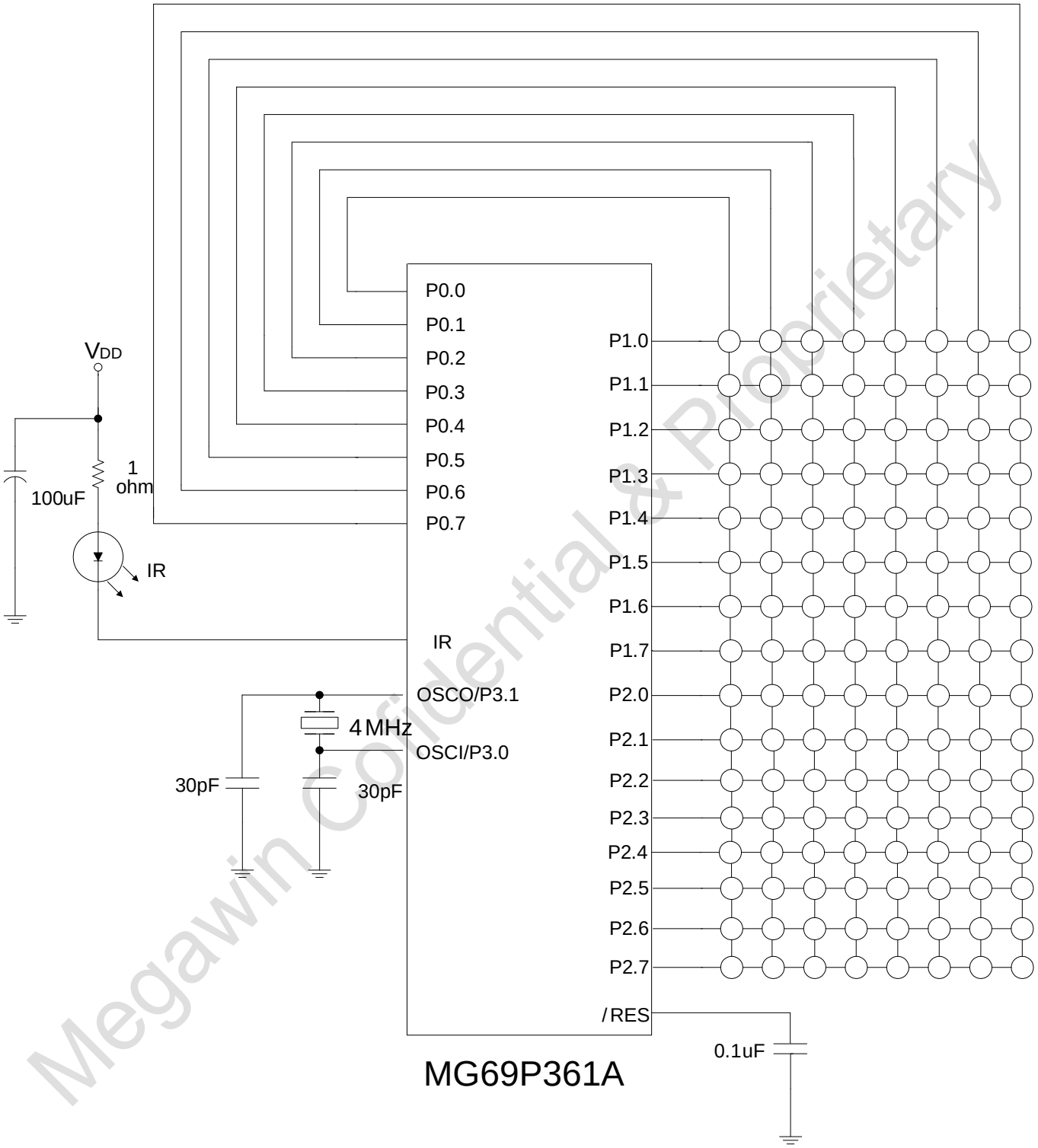


Figure 16-1 Application Circuit - Remote Controller

18 Electrical Characteristics

18.1 Absolute Maximum Rating

PARAMETER	RATING	UNIT
Supply Voltage to Ground Potential	VSS-0.3 to VSS+4.0	V
Applied Input / Output Voltage	VSS-0.3 to VDD+0.3	V
Ambient Operating Temperature	0 to +70	°C
Storage Temperature	-50 to +125	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

18.2 DC Characteristics

(VDD-VSS = 3.0 V, FOSC = 4MHz, Ta = 25° C; unless otherwise specified)

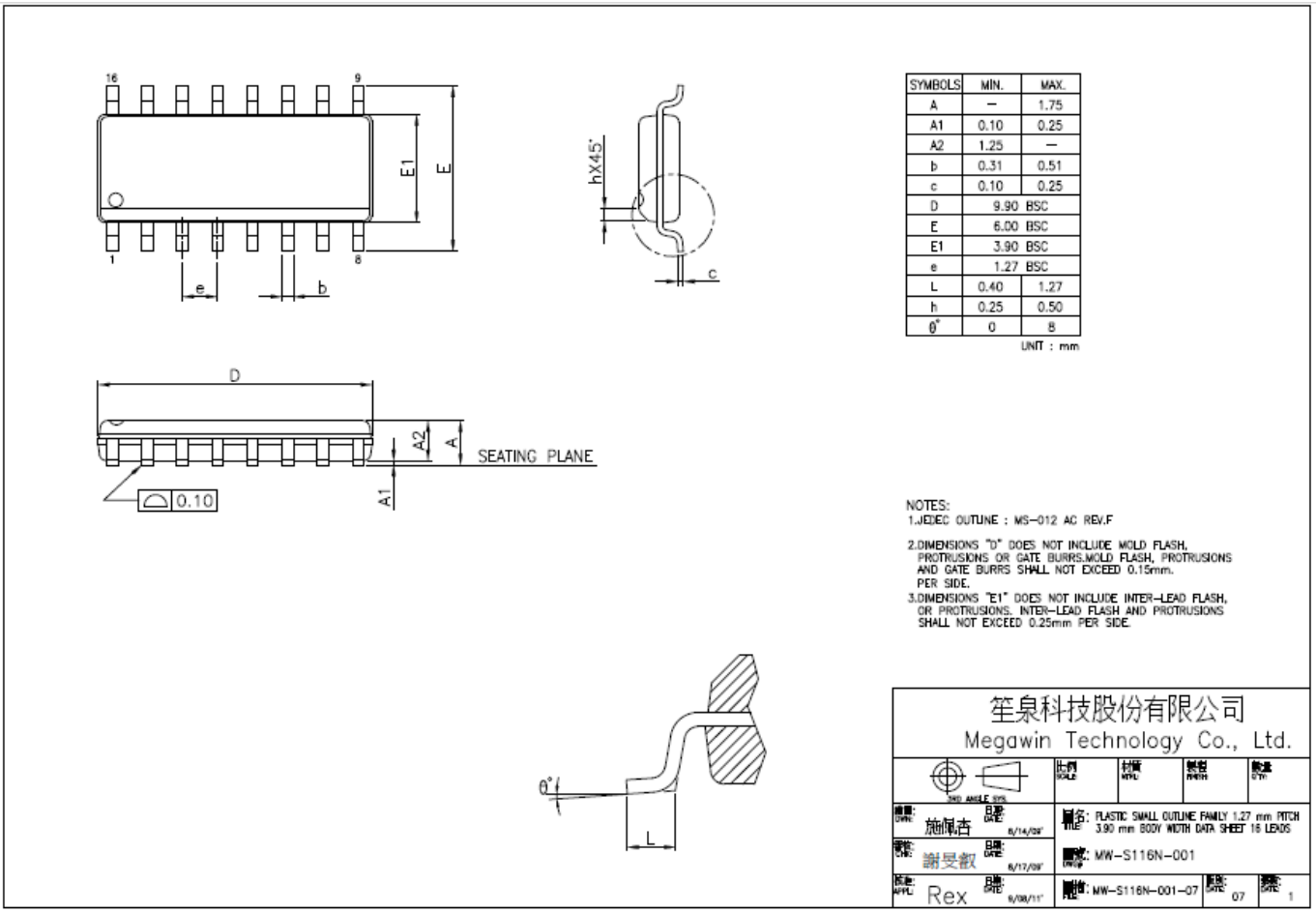
PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Op. Voltage	VDD	-	2.4	-	3.6	V
Op. Current	IOP	No load (Ext.-V) In normal operation	-	4.0	8	mA
Standby Current	ISTB	No load (Ext.-V)	-	-	3	μA
Input High Voltage	VIH	-	0.7 VDD	-	VDD	V
Input Low Voltage	VIL	-	0	-	0.3VDD	V
Port 0 ~ Port 3 Drive Current	IOH0	VOH = 2.4V, VDD = 3.0V	6	-	-	mA
Port 0 ~ Port 3 Sink Current	IOL0	VOL = 0.4V, VDD = 3.0V	10	-	-	mA
IRO Drive Current	IOH1	VOH = 2.4V, VDD = 3.0V	6	-	-	mA
IRO Sink Current	IOL1	VOL = 1V, VDD = 3.0V	250.0	-	-	mA
Port 0 ~ Port 3 Pull-high Resistor	RPH	VIL = 0V	-	100K	-	Ω
/RES Pull-high Resistor	RRES	VIL = 0V	-	30K	-	Ω
IRPH Pull-high Resistor 1	IRPHR1	VIL = 0V	-	50K	-	Ω
IRPH Pull-high Resistor 2	IRPHR2	VIL = 0V	-	100K	-	Ω
Low Voltage Detector	VLVD	VDD <2.4V	-	2.4	-	V
Low Voltage Reset	VLVR	-	-	2.2	-	V

18.3 AC Characteristics

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CPU Op. Frequency	F_{CPU}	V_{DD} = 3.0V	0.4	4	8	MHz
System Start-Up Time	T_{SST0}	Power-up or reset	-	32768	-	1/ F_{CPU}
	T_{SST1}	Wake-up from STOP mode (Fosc = 4MHz)		16384		
	T_{SST2}	Wake-up from STOP mode (Fosc = 3.5KHz)		256		
POR Duration	TPOR	FOSC = 4 MHz	10	15	50	mS

19 Package Dimension

19.1 SOP16 (Dimension 150m)



SYMBOLS	MIN.	MAX.
A	—	1.75
A1	0.10	0.25
A2	1.25	—
b	0.31	0.51
c	0.10	0.25
D	9.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.50
θ°	0	8

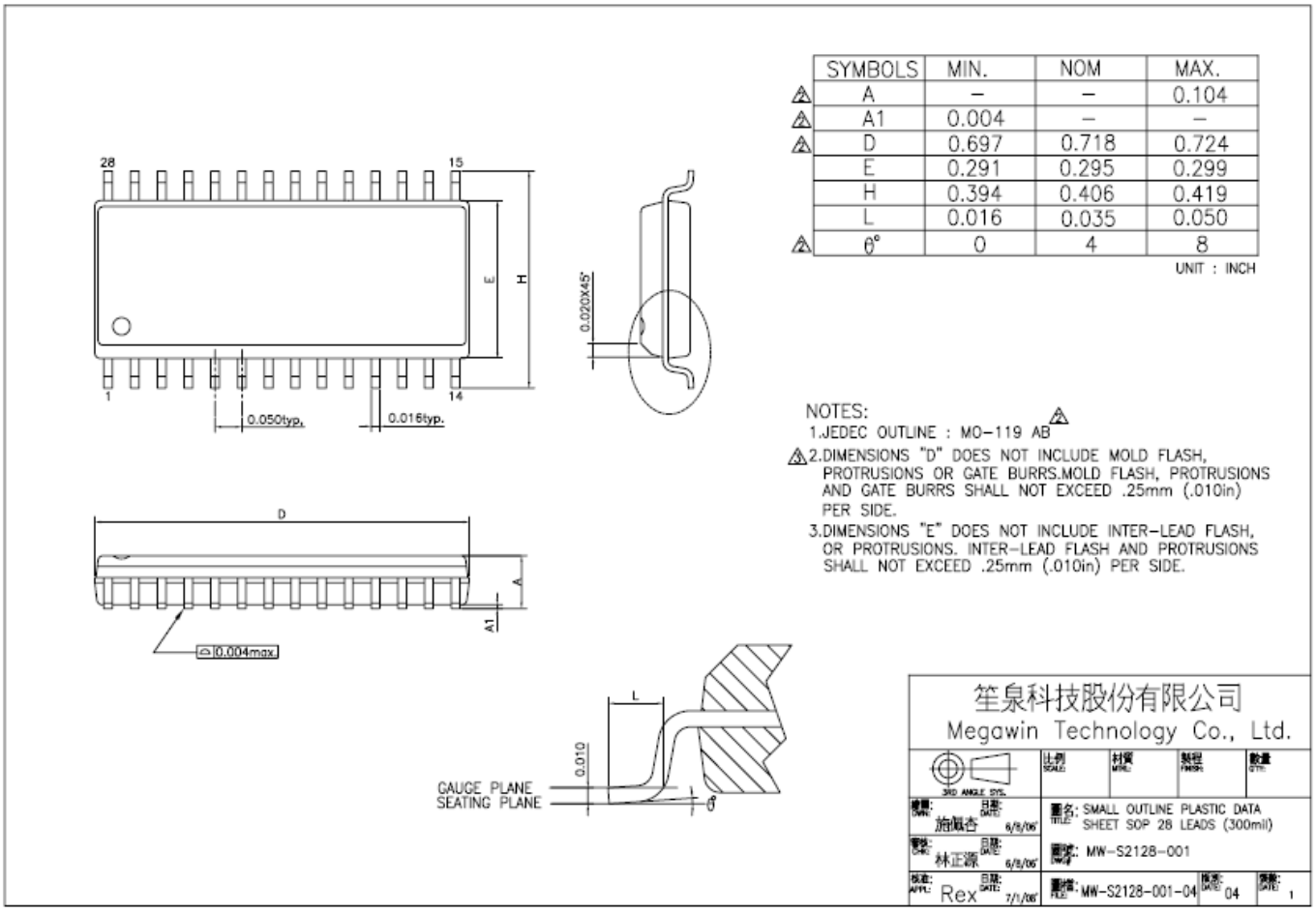
UNIT : mm

NOTES:
1.JEDEC OUTLINE : MS-012 AC REV.F
2.DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15mm. PER SIDE.
3.DIMENSIONS "E1" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25mm PER SIDE.

笙泉科技股份有限公司
Megawin Technology Co., Ltd.

DWN: 施佩吉	DATE: 8/14/09'	TITLE: PLASTIC SMALL OUTLINE FAMILY 1.27 mm PITCH 3.90 mm BODY WIDTH DATA SHEET 16 LEADS	
CHK: 謝旻叡	DATE: 8/17/09'	DWG NO: MW-S116N-001	
APPD: Rex	DATE: 9/08/11'	PART NO: MW-S116N-001-07	DATE: 07

19.2 SOP28 (Dimension 300m)



	SYMBOLS	MIN.	NOM	MAX.
⚠	A	–	–	0.104
⚠	A1	0.004	–	–
⚠	D	0.697	0.718	0.724
	E	0.291	0.295	0.299
	H	0.394	0.406	0.419
	L	0.016	0.035	0.050
⚠	θ°	0	4	8

UNIT : INCH

NOTES:
1.JEDEC OUTLINE : MO-119 AB ⚠
⚠2.DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .25mm (.010in) PER SIDE.
3.DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.

笙泉科技股份有限公司
Megawin Technology Co., Ltd.

3RD ANGLE SYS.	比例 SCALE:	材質 MTRL:	製程 FINISH: 數量 QTY:
繪圖 DRAWN: 施佩杏 6/8/06	圖名 TITLE: SMALL OUTLINE PLASTIC DATA SHEET SOP 28 LEADS (300mil)		
審核 CHKD: 林正源 6/8/06	圖號 PART NO.: MW-S2128-001		
核准 APPR: Rex 7/1/06	圖檔 FILE: MW-S2128-001-04	版次 DATE: 04	張次 DATE: 1

20 Revision History

Revision	Page	Descriptions	Date
V1.00		1. Initial release	2012/09/28
V1.01	37	1. Modify OR0 description	2012/10/08
V1.02	6,23	1. Modify TIM1 description , Modify Pin assign	2012/10/23
V1.03	6	1. Modify Pin assign	2012/10/31
V1.04	4	1. Modify feature description	2012/11/07
	27	2. Modify SPI pin assign & pull-high control function	
	32	3. Add pull-high control register of Port 2	
	40	4. Modify IOH1 SPEC.	
V1.05	14,15	1. Modify IRQen & EVTflag	2012/11/08
	22	2. Modify TM0 clock input	
	15	3. Modify DIV interrupt frequency	
V1.06	15	1. Modify DIV interrupt frequency	2012/11/13
V1.07	8	1. Add package pin configuration	2013/06/24
V1.08	26	1. PWM SFR Table & SFR Function Figure description	2016/07/18
	8	2. Add SOP16 & SOP28 package pin configuration description	
	42	3. Package Dimension	