

This product is obsolete.

This information is available for your convenience only.

For more information on Zarlink's obsolete products and replacement product lists, please visit

http://products.zarlink.com/obsolete_products/



Transmit Circuit for TDMA/AMPS

Features

- Dual RF Ports for 900MHz and 1900MHz
- AGC Amplifier with 90dB of Variable Gain, Fully Compensated for Temperature
- On-chip Active Filter. Removes the Requirement for External IF SAW Filter
- High Power 900MHz and 1900MHz Output Stages
- Quadrature Modulator

Applications

 Transmit Modulator and Up-converter in TDMA/ AMPS Mobile Phones

Absolute Maximum Ratings

Supply voltage (Vcc) 4V Control input voltage -0.6V to VCC + 0.6V Storage temperature, T_{STG} -55°C to +125°C Operating temperature -40°C to 100°C Max Junction Temperature (T_1) 150°C DS5241 ISSUE 3.0 December 2000

Ordering Information MGCT02/KG/QP1S MGCT02/KG/QP1T

The MGCT02 circuit is designed for use in dual band, dual mode cellular 900MHz/PCS1900MHz mobile phones. It can be used for TDMA/AMPS. The MGCT02 is compatible with baseband and mixed signal interface circuits from Zarlink Semiconductor and other manufacturers.

System costs have been kept to a minimum by removing the requirement for an additional SAW filter in the transmit IF path. The AGC has been split between RF and IF sections to reduce noise and a low pass filter has been included before the IF variable gain amplifier to remove spurious products produced in the modulator.

For CDMA systems the MGCT04 is recommended.

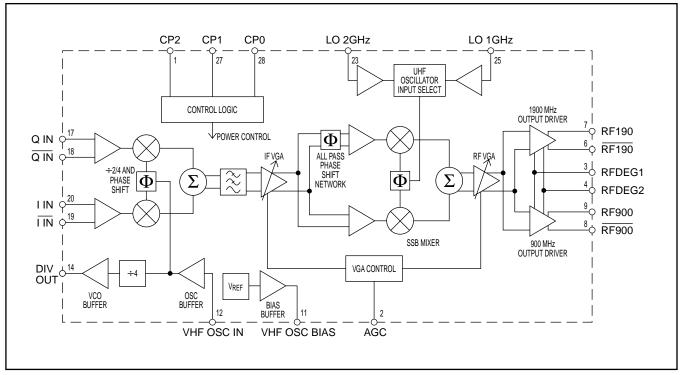


Figure 1 - MGCT02 Block Diagram

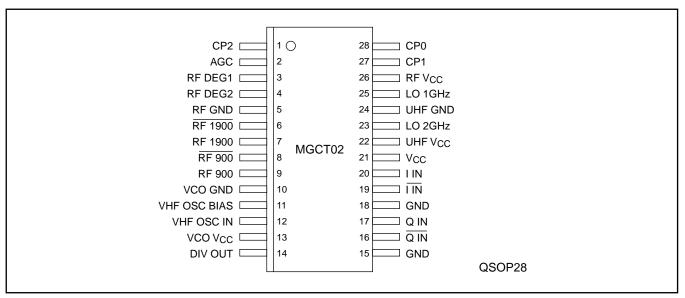


Figure 2 - Pin Connections - top view

Pin	Signal Name	Function			
1	CP2	Control pin 2. See Tables 4 and 5 for function			
2	AGC	Control voltage for IF and RF variable gain amplifiers			
3	RF DEG1	Connection to external inductor to control gain of power amplifiers			
4	RF DEG2	Connection to external inductor to control gain of power amplifiers			
5	RF GND	Ground connection to RF circuits			
6	RF 1900	Inverse output from 1900MHz differential output driver			
7	RF1900	Output from 1900MHz differential output driver			
8	RF 900	Inverse output from 900MHz differential output driver			
9	RF 900	Output from 900MHz differential output driver			
10	VCO GND	Ground connection for VHF oscillator			
11	VHF OSC BIAS	Switched bias voltage for external VHF oscillator			
12	VHF OSC IN	Input from external VHF oscillator			
13	VCO Vcc	Positive supply to VHF oscillator			
14	DIV OUT	Output from VHF oscillator divided by 4			
15	GND	Ground connection			
16	QIN	Q input			
17	Q IN	Q input			
18	GND	Ground connection			
19	IIN	l input			
20	LIN	I input			
21	Vcc	Positive supply connection			
22	UHF Vcc	Positive supply to UHF oscillator input buffers			
23	LO 2GHZ	2GHz local oscillator input			
24	GND UHF	Ground connection to UHF oscillator input buffers			
25	LO 1GHZ	1GHz local oscillator input			
26	RF Vcc	Positive supply connection to RF circuits			
27	CP1	Control pin 1. See Tables 4 and 5 for function			
28	CP0	Control pin 0. See Tables 4 and 5 for function			

Table 1 - Pin Assignments

Electrical Characteristics

Test conditions (unless otherwise stated): Tamb = -30° C to $+70^{\circ}$ C, $V_{CC} = 2.7$ V to 3.6V. UHF LO level = -15dBm (both bands), I, Q input = 1.4 volts p.p, test frequency = 849MHz (900 output) and 1910MHz (1900 output). These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Value			l luite	Conditions	
Characteristics	Min. Typ.		Max.	Units	Conditions	
Supply current						
Sleep current			75	μΑ	All circuits off	
Standby mode supply current		8	10	mA	See Tables 4 and 5	
Total supply current		118	152	mA	Maximum power PCS mode	
Standby to operating mode			10	μs		
switching time						
Logic inputs						
Logic high voltage	Vcc -0.6		VCC	V		
Logic low voltage	0		8-0	V		

Table 2 - DC Characteristics

Characteristics	Value			Unita	Conditions	
Characteristics	Min.	Тур.	Max.	Units	Conditions	
I and Q modulator						
I and Q input voltage level	1.0	1.4	2.0	Vpp	Differential	
I and Q common mode voltage		1.2		V		
I and Q differential input resistance	13.5			kΩ		
I and Q input bandwidth	2.5			MHz		
IF Vector offset	30			dB		
SSB rejection	30			dB		
VHF oscillator input and divider						
Input drive level	22	40	70	mVrms	From external VHF osc. via matching network	
VHF oscillator bias voltage		1.2		V		
Output level from prescaler	400			mVpp	6pF load	
Prescaler divide ratio		4			Drive output for synthesiser	
Variable gain amplifiers						
IF amp. operating frequency range	50		200	MHz		
RF amp. operating frequency range	750		2000	MHz		
Gain control range	60			dB	VGA=0.5 to 2.6V	
Control voltage for minimum gain	0.1			V		
Control voltage for maximum gain			2.6	V		
AGC control voltage slope	33		60	dB/V		

Table 3 - AC Characteristics

	Value				O and Pittle man	
Characteristics	Min.	Тур.	Max.	Units	Conditions	
SSB mixer and UHF oscillator						
inputs	40			ID.		
SSB rejection	18		_	dB		
Cellular band LO input level	-15	-10	-5	dBm	From external UHF osc. via matching network	
PCS band LO input level	-15	-10	-5	dBm	From external UHF osc. via matching network	
Cellular band local oscillator input frequency. (LO 1GHz)	850		1100	MHz		
PCS band local oscillator input frequency (LO 2GHz)	1500		2150	MHz		
900MHz RF output stage					Specifications assume 50 ohm load driven via a matching network (Fig. 6)	
RF amplifier operating frequency range	824		849	MHz		
Output power	+8		+19	dBm	Note 1	
ACPR (TDMA)	-45		-30	dBc	Pout = +8dBm, Offset = 30kHz	
	-90		-60	dBc	Pout = +8dBm, Offset = 60kHz	
Output power AMPS	+10	+14	+19	dBm	Note 2	
Receive band noise (869 - 894MHz)		-123	-121	dBm/ Hz	ftx = 849 MHz Pout = +8dBm	
Spurious Outputs						
LO Leakage			-18	dBc	Note 2, Pout = +8dBm	
LO Leakage			-14	dBm	Vcc = 3V, T = 25 °C Pout = +8dBm	
Image Rejection			-18	dBc	Note 2, Pout = +8dBm	
Other Spurii			-20	dBm	Note 3	
1900MHz RF output stage (PCS)					Specifications assume 50 ohm load driven via a matching network (Fig. 5)	
RF amplifier operating frequency range	1850		1910	MHz		
Output power	+8		+18	dBm	Note 1	
ACPR (TDMA)	-45		-30	dBc	Pout = +8dBm, Offset = 30kHz	
	-90		-60	dBc	Pout = +8dBm, Offset = 60kHz	
Receive band noise (1930 - 1990 MHz)		-123	-121	dBm/ Hz	ftx = 1910MHz, Pout = +8dBm	
Receive band noise (1930 - 1990MHz)		-128	-125	dBm/ Hz	ftx = 1910MHz, Pout = +3dBm Vcc = 3V, T =25°C	

Table 3 - AC Characteristics (continued)

Characteristics	Value			Unito	Conditions	
Characteristics	Min.	Тур.	Max.	Units	Conditions	
Spurious Outputs						
LO Leakage			-18	dBc	Note 2, Pout = =8dBm	
LO Leakage			-14	dBm	Vcc = 3V, T = 25 °C Pout = +8dBm	
Image Rejection			-18	dBc	Note 2, Pout = +8dBm	
Other Spurii			-20	dBm	Note 3	

Table 3 - AC Characteristics (continued)

Notes:

- 1. V (I/Q) = 1.4V differential, VHF LO = 22mV rms, UHF LO = -15dBm, VGA = 2.6volts
- 2. V(I/Q) = 1.4 V dc differential, VHF LO = 22mV rms, UHF LO = -15dBm
- 3. Frequency range 10MHz to 10*ftx except Rx and Tx bands

Circuit Description

General

The MGCT02 circuit is designed to provide the transmit function in dual band dual mode IS136/AMPS mobile phones. The circuit contains the following blocks:

- 1. Quadrature modulator
- 2. VHF voltage controlled oscillator buffer and divide by 4 prescaler
- 3. Active IF low pass filter
- 4. IF variable gain amplifier
- 5. Single sideband mixer with external UHF oscillator inputs
- 6. RF variable gain amplifier
- 900MHz and 1900MHz high power output driver stages
- 8. Power and mode control logic

Quadrature Modulator

I and Q data from a baseband circuit such as the Zarlink Semiconductor MGCM01 or MGCM02 circuit is applied to the I and Q inputs of the quadrature modulator to produce the intermediate frequency by mixing with the local oscillator frequency from the

VHF VCO. The control inputs can select either a divide by two or divide by four function between the VHF VCO and the quadrature modulator giving a choice of possible intermediate frequencies.

VHF Oscillator Input Oscillator Bias and Divider

An external VHF oscillator circuit is AC coupled to the VHF oscillator input. The oscillator drives the quadrature modulator and an internal divide by four circuit to reduce the frequency of the output signal to be sent off chip to the frequency synthesiser. This reduces the power required in the output buffer circuit and also allows a low frequency low power CMOS synthesiser to be used. An oscillator bias circuit is included on the chip so that the external VHF oscillator transistor can be switched off using the control inputs. The bias voltage is switched off in either of the sieep conditions shown in Tables 4 and 5.

Active Low Pass Filter

The output from the quadrature modulator is passed to the active low pass filter which attenuates wide band noise and spurious outputs.

IF Variable Gain Amplifier

The filtered IF signal is passed to the IF variable gain amplifier which in turn drives the single sideband mixer. An externally applied AGC control voltage allows the total circuit gain to be varied.

The AGC action is split between the IF and RF portions of the circuit and an internal AGC control circuit processes the external AGC control voltage to drive both IF and RF variable gain amplifiers and provides a near linear control characteristic over the entire AGC range.

Single Sideband Mixer

The modulated IF signal is fed to the single sideband mixer which up-converts the IF to the RF frequency to be transmitted by mixing with an RF signal from one of two external UHF oscillator input pins, seiected by an on chip multiplexer. When 1900MHz mode is programmed with the VHF oscillator in divide by four mode (Tables 4 and 5), the polarity of the quadrature oscillator drive signals to the single sideband mixer are reversed, thus selecting a low side LO for 1900MHz PCS and high side for 900MHz. This technique allows a common IF and filter to be used for both 900MHz and 1900MHz bands.

RF Variable Gain Amplifier

The SSB mixer is followed by the RF variable gain amplifier stage which provides about 23dB of the total gain variation. An additional SAW filter in the

transmit path is avoided by providing the gain variation after the mixer.

The variable gain amplifier control circuit ensures that the attenuation from maximum power is initially controlled by the RF variable gain stage thus reducing the noise contribution from the RF mixer.

Output Drivers

Separate output drive stages are provided for 900MHz and 1900MHz operation. A differential design is used for both amplifiers to improve power efficiency and to ease power supply decoupling problems. The 900MHz output stage provides a linear output of 8dBm for TDMA operation, but is over-driven in AMPS mode to obtain a typical output of 11dBm. In both power driver stages the DC current is backed off as the RF and IF gain is reduced, improving efficiency when less than maximum output power is required.

Control Inputs

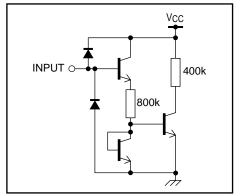
Three control inputs are provided to select different operating modes for the chip; the various modes selected by the control pins are shown in Tables 4 and 5.

CP2	CP1	CP0	Function				
0	0	0	Sleep mode. All circuits powered down				
0	0	1	Quadrature modulator on. 1900MHz mode. Low side UHF LO. IF = VHF VCO ÷ 4				
0	1	0	Quadrature modulator on. 900MHz mode. high side UHF LO. IF = VHF VCO ÷ 4				
0	1	1	Standby mode. VHF oscillator input buffer, oscillator bias and divider on. All other circuits powered down				

Table 4 - Control pin functions; VHF LO in divide-by-four mode

CP2	CP1	CP0	Function
1	0	0	Sleep mode. All circuits powered down
1	0	1	Quadrature modulator on. 1900MHz mode. Low side UHF LO. IF = VHF VCO ÷ 2
1	1	0	Quadrature modulator on. 900MHz mode. high side UHF LO. IF = VHF VCO ÷ 2
1	1	1	Standby mode. VHF oscillator input buffer, oscillator bias and divider on. All other circuits powered down

Table 5 - Control pin functions; VHF LO in divide-by-two mode



VCC 600 OSC BIAS VREF 1.2V

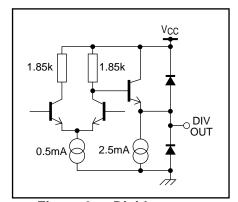
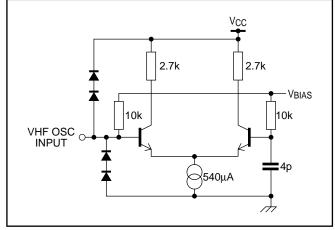


Figure 3a - Control inputs CP0, CP1 and CP2

Figure 3b - Oscillator bias buffer

Figure 3c - Divider ouput circuit



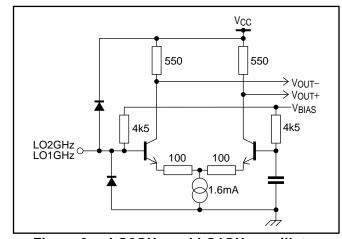


Figure 3d - VHF oscillator input buffer

Figure 3e - LO2GHz and LO1GHz oscillator inputs

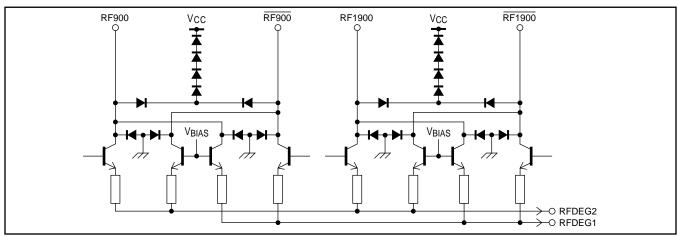


Figure 3f - 900MHz and 1900MHz outputs

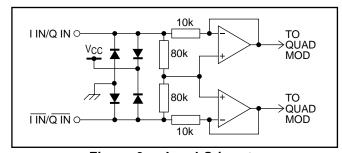


Figure 3g - I and Q inputs

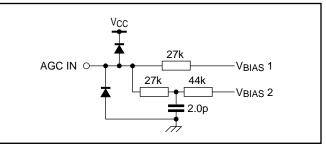


Figure 3h - AGC input

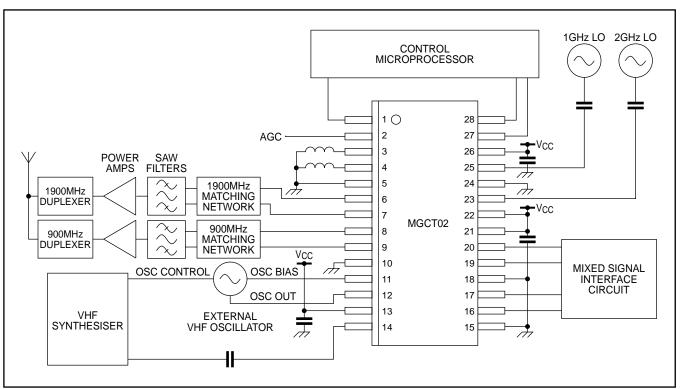


Figure 4 - Typical application circuit

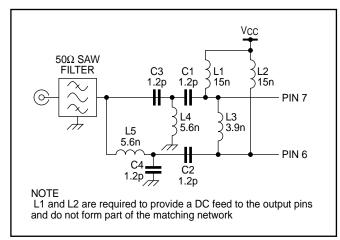


Figure 5 - Typical 1900MHz output matching network

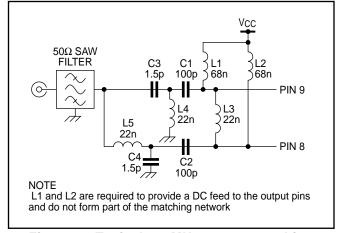


Figure 6 - Typical 900MHz output matching network

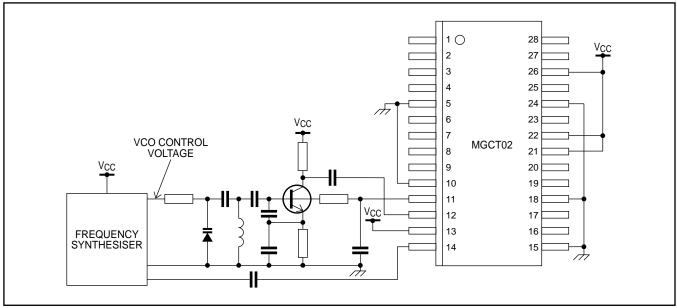


Figure 7 - Typical circuit showing connection of external VHF oscillator

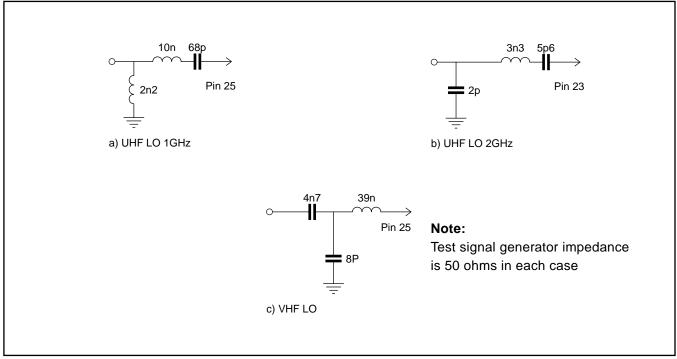
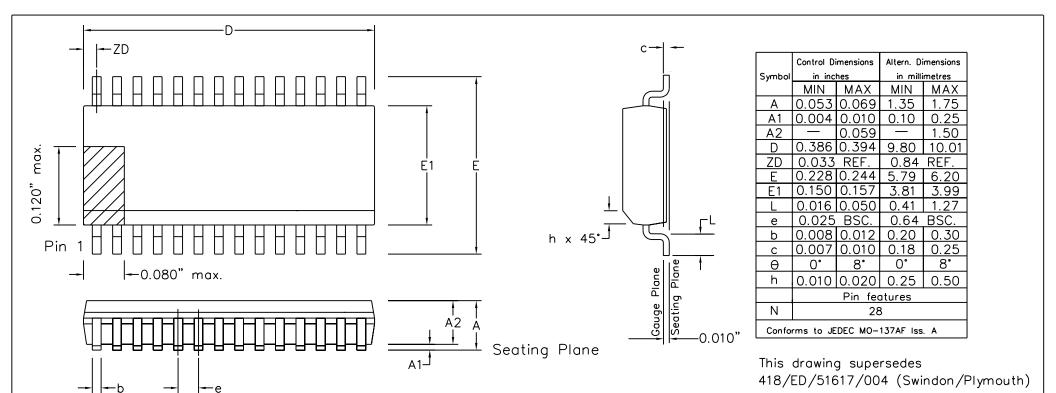


Figure 8 - LO Input Test Circuits



Notes:

- 1. The chamfer on the body is optional. If it is not present, a visual index feature, e.g. a dot, must be located within the cross—hatched area.
- 2. Controlling dimensions are in inches.
- 3. Dimension D do not include mould flash, protrusion or gate burrs. These shall not exceed 0.006" per side.
- 4. Dimension E1 do not include inter-lead flash or protrusion. These shall not exceed 0.010" per side.
- 5. Dimension b does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.004" total in excess of b dimension.

© Zarlink Semiconductor 2002 All rights reserved.							Package Code
ISSUE	1	2	3			Previous package codes	Package Outline for 28 lead
ACN	201930	207316	212476		ZARLINK SEMICONDUCTOR	QP / Q	Package Outline for 28 lead QSOP (0.150" Body Width)
DATE	27Feb97	24Aug99	3Apr02		JEMILEGINGOCION	·	
APPRD.							GPD00292



For more information about all Zarlink products visit our Web Site at www.zarlink.com

Information relating to products and services furnished herein by Zarlink Semiconductor Inc. or its subsidiaries (collectively "Zarlink") is believed to be reliable. However, Zarlink assumes no liability for errors that may appear in this publication, or for liability otherwise arising from the application or use of any such information, product or service or for any infringement of patents or other intellectual property rights owned by third parties which may result from such application or use. Neither the supply of such information or purchase of product or service conveys any license, either express or implied, under patents or other intellectual property rights owned by Zarlink or licensed from third parties by Zarlink, whatsoever. Purchasers of products are also hereby notified that the use of product in certain ways or in combination with Zarlink, or non-Zarlink furnished goods or services may infringe patents or other intellectual property rights owned by Zarlink.

This publication is issued to provide information only and (unless agreed by Zarlink in writing) may not be used, applied or reproduced for any purpose nor form part of any order or contract nor to be regarded as a representation relating to the products or services concerned. The products, their specifications, services and other information appearing in this publication are subject to change by Zarlink without notice. No warranty or guarantee express or implied is made regarding the capability, performance or suitability of any product or service. Information concerning possible methods of use is provided as a guide only and does not constitute any guarantee that such methods of use will be satisfactory in a specific piece of equipment. It is the user's responsibility to fully determine the performance and suitability of any equipment using such information and to ensure that any publication or data used is up to date and has not been superseded. Manufacturing does not necessarily include testing of all functions or parameters. These products are not suitable for use in any medical products whose failure to perform may result in significant injury or death to the user. All products and materials are sold and services provided subject to Zarlink's conditions of sale which are available on request.

Purchase of Zarlink's I²C components conveys a licence under the Philips I²C Patent rights to use these components in and I²C System, provided that the system conforms to the I²C Standard Specification as defined by Philips.

Zarlink, ZL and the Zarlink Semiconductor logo are trademarks of Zarlink Semiconductor Inc.

Copyright Zarlink Semiconductor Inc. All Rights Reserved.

TECHNICAL DOCUMENTATION - NOT FOR RESALE