ZARLINK SEMICONDUCTOR

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MGCT04

Transmit Circuit for TDMA/AMPS and CDMA/AMPS

Preliminary Information

DS5424 ISSUE 1.1 March 2001

Features

- Dual RF Ports for 900MHz and 1900MHz
- AGC Amplifier with 90dB of Variable Gain, Fully Compensated for Temperature
- On-chip Active Filter. Removes the Requirement for External IF SAW Filter
- High Power 900MHz and 1900MHz Output Stages
- Quadrature Modulator
- Small Scale MLF Package

Ordering Information

MGCT04/KG/LH1S
MGCT04/KG/LH1T

Applications

- Transmit Modulator and Up-converter in TDMA/AMPS Mobile Phones
- Transmit Up-converter in CDMA/AMPS Mobile Phones

The MGCT04 circuit is designed for use in dual band, dual mode cellular 900MHz/PCS1900MHz mobile phones. It can be used for both TDMA/AMPS or CDMA/AMPS systems. The MGCT04 is compatible with baseband and mixed signal interface circuits from Zarlink Semiconductor and other manufacturers.

System costs have been kept to a minimum by removing the requirement for an additional SAW filter in the transmit IF path. The AGC has been split between RF and IF sections to reduce noise and a low pass filter has been included before the IF variable gain amplifier to remove spurious products produced in the modulator.

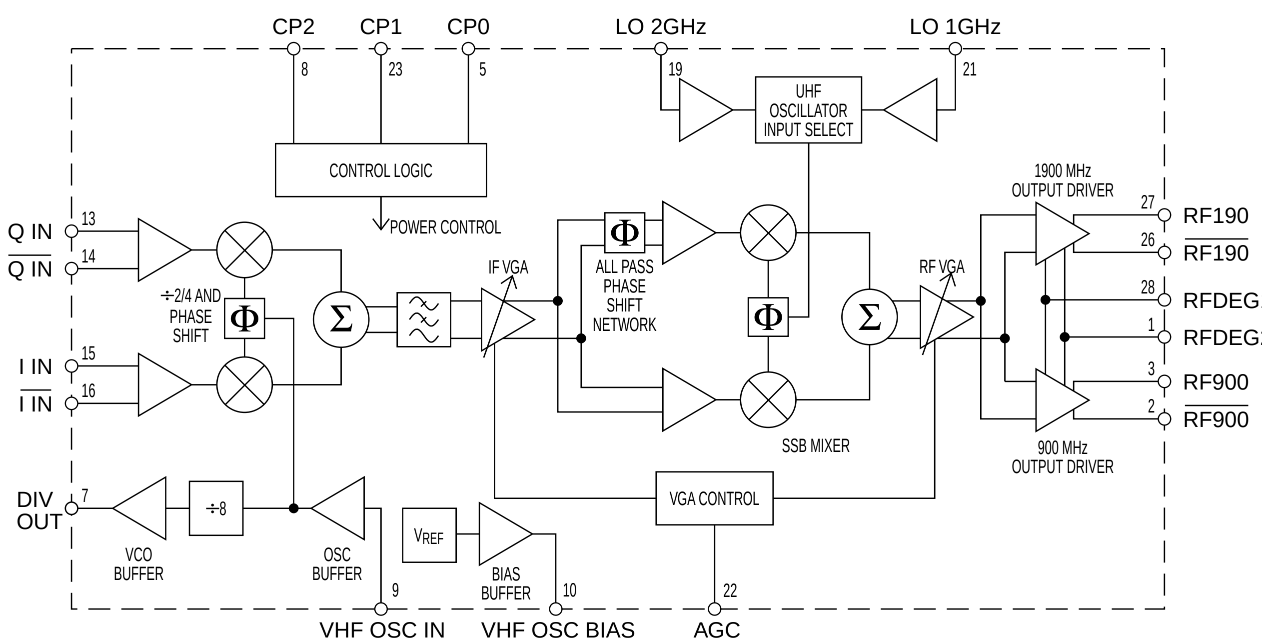
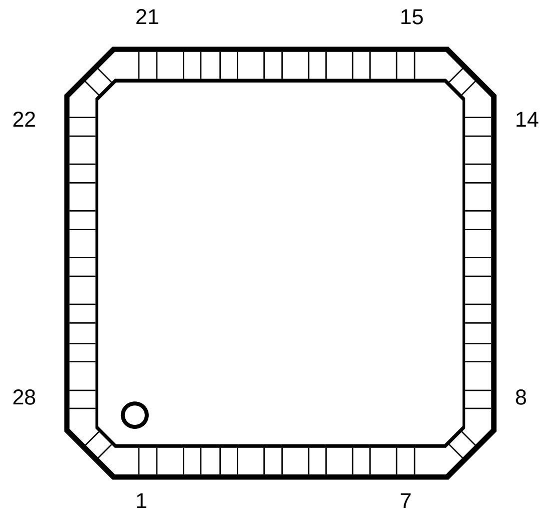


Figure 1 - MGCT04 Block Diagram



Note:
Corner Pads are connected to ground

Figure 2 - Pin Connections - top view

Pin	Signal Name	Function
1	RF DEG2	Connection to external inductor to control gain of power amplifiers
2	RF 900B	Inverse output from 900MHz differential output driver
3	RF 900	Output from 900MHz differential output driver
4	RF GND	Ground to RF circuits
5	CP0	Control pin 0. See tables 2 & 3 for function
6	VCO GND	Ground for VHF oscillator
7	DIV OUT	Output from VHF oscillator divided by 8
8	CP2	Control pin 2. See tables 2 & 3 for function
9	VHF OSC IN	Input from external VHF oscillator
10	VHF OSC BIAS	Switched bias voltage for external VHF oscillator
11	VCO V_{CC}	Positive supply to VHF oscillator
12	GND	Ground
13	Q IN	Q +input
14	Q INB	Q -input
15	I IN	I +input
16	I INB	I -input
17	V_{CC}	Positive supply
18	UHF V_{CC}	Positive supply to UHF LO input buffers
19	LO 2GHZ	2GHz local oscillator input
20	GND UHF	Ground to UHF oscillator input buffers
21	LO 1GHZ	1GHz local oscillator input
22	AGC	Control voltage for IF and RF variable gain amplifiers
23	CP1	Control pin 1. See tables 2 & 3 for function
24	RF V_{CC}	Positive supply to RF circuits
25	RF GND	Ground to RF circuits
26	RF 1900B	Inverse output from 1900MHz differential output driver
27	RF 1900	Output from 1900MHz differential output driver
28	RF DEG1	Connection to external inductor to control gain of power amplifiers

Table 1 - Pin Assignments

Absolute Maximum Ratings

Supply voltage (V_{CC})	4V	Operating temperature	-40˚C to 100˚C
Control input voltage	-0.6V to V_{CC} + 0.6V	Max Junction Temperature (T_J)	150˚C
Storage temperature, T_{STG}	-55˚C to +125˚C		

Electrical Characteristics

Test conditions (unless otherwise stated): Tamb = -30°C to +70°C, V_{CC} = 2·7V to 3·6V. UHF LO level = -15dBm (both bands), I, Q input = 1.4 volts p.p, test frequency = 849MHz (900 output) and 1910MHz (1900 output).These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current					
Sleep current			75	µA	All circuits off
Standby mode		8	10	mA	See Tables 4 and 5
Standby Mode - Prescaler disabled		4		mA	Pin 7 connected to V_{CC}
Total supply current		118	160	mA	Maximum power PCS mode
Standby to operating mode switching time			10	µs	
Logic inputs					
Logic high voltage	V_{CC} -0.6		V_{CC}	V	
Logic low voltage	0		0·8	V	

Table 2 - DC Characteristics

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
I and Q modulator					
I and Q input voltage level	1.0	1.4	2.0	Vpp	Differential
I and Q common mode voltage		1.2		V	
I and Q differential input resistance	13.5			kΩ	
I and Q input bandwidth	2.5			MHz	
IF Vector offset	25			dB	Pout = +8dBm
SSB rejection	30			dB	Pout = + 8dBm
VHF oscillator input and divider					
Input drive level	22	40	70	mVrms	From external VHF osc. via matching network
VHF oscillator bias voltage		1.2		V	
Output level from prescaler	400			mVpp	6pF load
Prescaler divide ratio		8			Drive output for synthesiser

Table 3 - AC Characteristics

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Variable gain amplifiers					
IF amp. operating frequency range	50		200	MHz	
RF amp. operating frequency range	750		2000	MHz	
Overall gain control range	84	90		dB	Voltage gain
Control voltage for minimum gain	0.1			V	
Control voltage for maximum gain			2.6	V	
AGC control voltage slope	33		60	dB/V	
SSB mixer and UHF oscillator inputs					
Cellular band LO input level	-15	-10	-5	dBm	From external UHF osc. via matching network
PCS band LO input level	-15	-10	-5	dBm	From external UHF osc. via matching network
Cellular band local oscillator input frequency. (LO 1GHz)	850		1100	MHz	
PCS band local oscillator input frequency (LO 2GHz)	1500		2150	MHz	
900MHz RF output stage					Specifications assume 50 ohm load driven via a matching network (Fig. 6)
RF amplifier operating frequency range	824		849	MHz	
Output power	+8		+19	dBm	Note 1
ACPR (CDMA)	-66		-52	dBc	Pout = +3dBm Vcc = 3V
ACPR (TDMA)	-45		-30	dBc	Pout = +8dBm, Offset = 30kHz Vcc = 3V
	-90		-60	dBc	Pout = +8dBm, Offset = 60kHz Vcc = 3V
Output power AMPS	+10	+14	+19	dBm	Note 2
Receive band noise		-128		dBm/Hz	At duplex frequency, offset 45MHz Pout = +3dBm
Receive band noise (869 - 894MHz)		-123	121	dBm/Hz	ftx = 849 MHz Pout = +8dBm
Spurious Outputs					
LO Leakage		-30	-20	dBc	Pout = +8dBm
Image Rejection		-30	-20	dBc	Pout = +8dBm
Other Spurii			-20	dBm	Note 3

Table 3 - AC Characteristics (continued)

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
1900MHz RF output stage (PCS)					Specifications assume 50 ohm load driven via a matching network (Fig. 5)
RF amplifier operating frequency range	1850		1910	MHz	
Output power	+8		+18	dBm	Note 1
ACPR (CDMA)	-66		-52	dBc	Pout = +3dBm Vcc = 3V
ACPR (TDMA)	-45		-30	dBc	Pout = +8dBm, Offset = 30kHz Vcc = 3V
	-90		-60	dBc	Pout = +8dBm, Offset = 60kHz Vcc = 3V
Receive band noise		-128		dBm/Hz	At duplex frequency, offset 80MHz Pout = +3dBm
Receive band noise (1930 - 1990 MHz)		-123	-121	dBm/Hz	ftx = 1910MHz, Pout = +8dBm
Spurious Outputs					
LO Leakage		-30	-20	dBc	Pout = +8dBm
Image Rejection		-30	-20	dBc	Pout = +8dBm
Other Spurii			-20	dBm	Note 3

Table 3 - AC Characteristics (continued)

Notes:

1. V (I/Q) = 1.4V differential, VHF LO = 22mV rms, UHF LO = -15dBm, VGA = 2.6volts
2. V (I/Q) = 1.4 V dc differential, VHF LO = 22mV rms, UHF LO = -15dBm, VGA = 2.6 volts
3. Frequency range 10MHz to 10*ftx except Rx and Tx bands

Circuit Description

General

The MGCT04 circuit is designed to provide the transmit function in dual band dual mode CDMA/AMPS IS136/AMPS mobile phones. The circuit contains the following blocks:

1. Quadrature modulator
2. VHF voltage controlled oscillator buffer and divide by 8 prescaler
3. Active IF low pass filter
4. IF variable gain amplifier
5. Single sideband mixer with external UHF oscillator inputs
6. RF variable gain amplifier
7. 900MHz and 1900MHz high power output driver stages
8. Power and mode control logic

Quadrature Modulator

I and Q data from a baseband circuit such as the Zarlink Semiconductor MGCM02 or MGCM03 circuit is applied to the I and Q inputs of the quadrature modulator to produce the intermediate frequency by mixing with the local oscillator frequency from the VHF VCO. The control inputs can select either a divide by two or divide by four function between the VHF VCO and the quadrature modulator giving a choice of possible intermediate frequencies.

VHF Oscillator Input Oscillator Bias and Divider

An external VHF oscillator circuit is AC coupled to the VHF oscillator input. The oscillator drives the quadrature modulator and an internal divide by eight circuit to reduce the frequency of the output signal to be sent off chip to the frequency synthesiser. This reduces the power required in the output buffer circuit and also allows a low frequency low power CMOS synthesiser to be used. The divider can be disabled if not required by connecting the output pin (DIV OUT - pin 7) to the positive power supply. This reduces the total supply current by typically 4mA. An oscillator bias circuit is included on the chip so that the external VHF oscillator transistor can be switched off using the control inputs. The bias voltage is switched off in either of the sleep conditions shown in Tables 4 and 5.

Active Low Pass Filter

The output from the quadrature modulator is passed to the active low pass filter which attenuates wide band noise and spurious outputs.

IF Variable Gain Amplifier

The filtered IF signal is passed to the IF variable gain amplifier which in turn drives the single sideband mixer. An externally applied AGC control voltage allows the total circuit gain to be varied over a minimum 84dB range.

The AGC action is split between the IF and RF portions of the circuit and an internal AGC control circuit processes the external AGC control voltage to drive both IF and RF variable gain amplifiers and provides a near linear control characteristic over the entire AGC range.

Single Sideband Mixer

The modulated IF signal is fed to the single sideband mixer which up-converts the IF to the RF frequency to be transmitted by mixing with an RF signal from one of two external UHF oscillator input pins, seiected by an on chip multiplexer. When 1900MHz mode is programmed with the VHF oscillator in divide by four mode (Tables 4 and 5), the polarity of the quadrature oscillator drive signals to the single sideband mixer are reversed, thus selecting a low side LO for 1900MHz PCS and high side for 900MHz. This technique allows a common IF and filter to be used for both 900MHz and 1900MHz bands.

RF Variable Gain Amplifier

The SSB mixer is followed by the RF variable gain amplifier stage which provides about 23dB of the total gain variation. An additional SAW filter in the transmit path is avoided by providing the gain variation after the mixer.

The variable gain amplifier control circuit ensures that the attenuation from maximum power is initially controlled by the RF variable gain stage thus reducing the noise contribution from the RF mixer.

Output Drivers

Separate output drive stages are provided for 900MHz and 1900MHz operation. A differential design is used for both amplifiers to improve power efficiency and to ease power supply decoupling problems. The 900MHz output stage provides a linear output of 3 to 5 dBm for CDMA and 8 dBm for TDMA operation, but is over-driven in AMPS mode to obtain a typical output of 11dBm. In both power driver stages the DC current is backed off as the RF and IF gain is reduced, improving efficiency when less than maximum output power is required.

Control Inputs

Three control inputs are provided to select different operating modes for the chip; the various modes selected by the control pins are shown in Tables 4 and 5.

CP2	CP1	CP0	Function
0	0	0	Sleep mode. All circuits powered down
0	0	1	Quadrature modulator on. 1900MHz mode. Low side UHF LO. IF = VHF VCO ÷ 4
0	1	0	Quadrature modulator on. 900MHz mode. high side UHF LO. IF = VHF VCO ÷ 4
0	1	1	Standby mode. VHF oscillator input buffer, oscillator bias and divider on. All other circuits powered down

Table 4 - Control pin functions; VHF LO in divide-by-four mode

CP2	CP1	CP0	Function
1	0	0	Sleep mode. All circuits powered down
1	0	1	Quadrature modulator on. 1900MHz mode. High side UHF LO. IF = VHF VCO ÷ 2
1	1	0	Quadrature modulator on. 900MHz mode. high side UHF LO. IF = VHF VCO ÷ 2
1	1	1	Standby mode. VHF oscillator input buffer, oscillator bias and divider on. All other circuits powered down

Table 5 - Control pin functions; VHF LO in divide-by-two mode

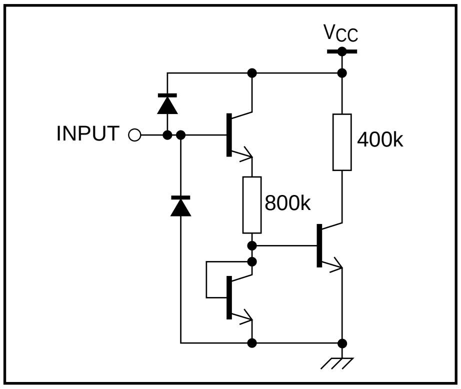


Figure 3a - Control inputs CP0, CP1 and CP2

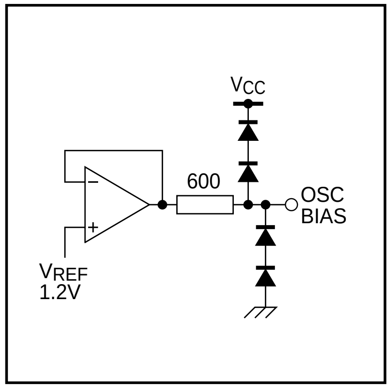


Figure 3b - Oscillator bias buffer

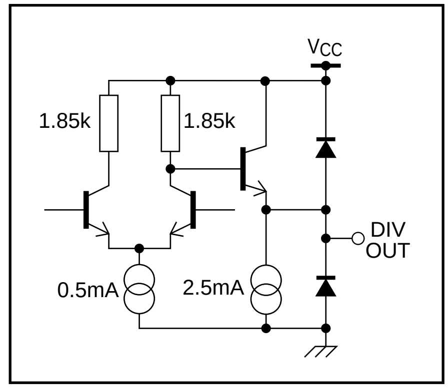


Figure 3c - Divider ouput circuit

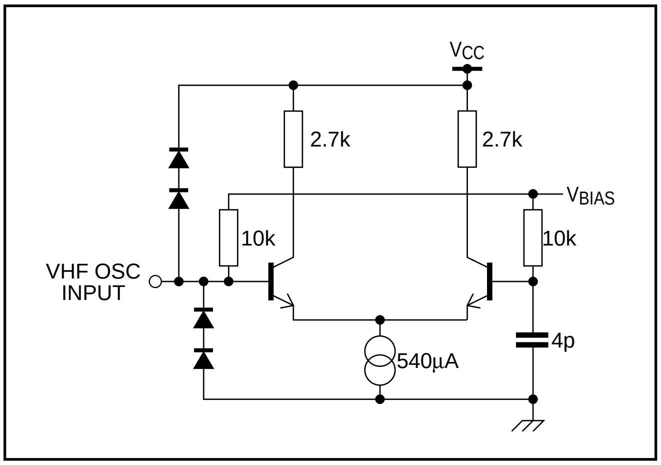


Figure 3d - VHF oscillator input buffer

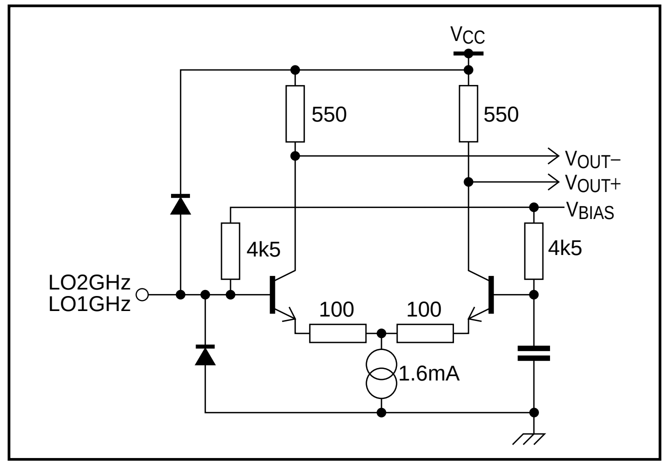


Figure 3e - LO2GHz and LO1GHz oscillator inputs

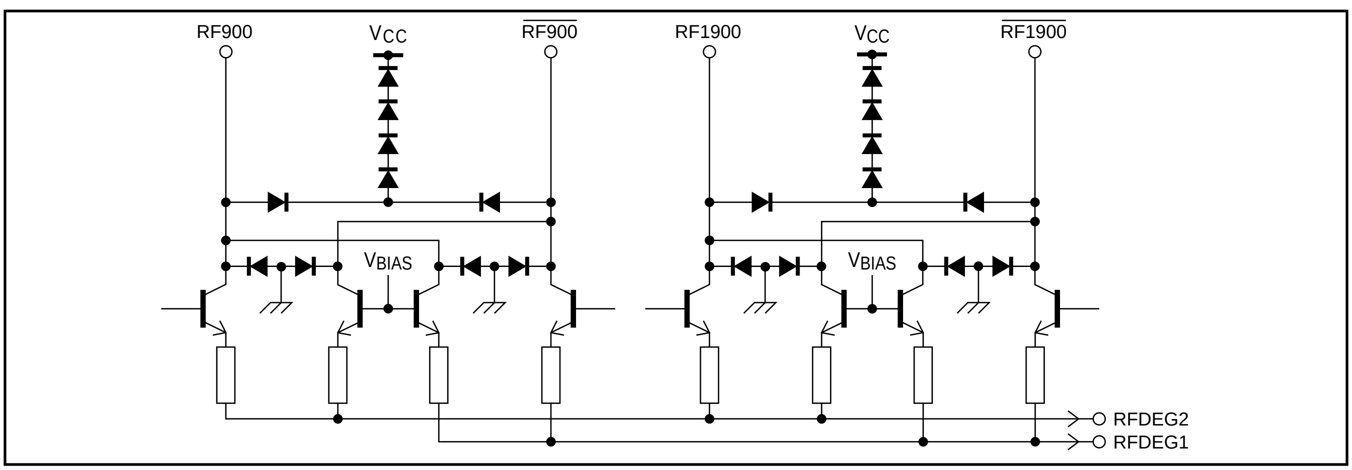


Figure 3f - 900MHz and 1900MHz outputs

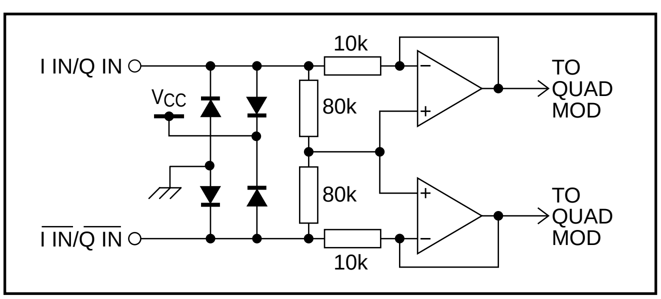


Figure 3g - I and Q inputs

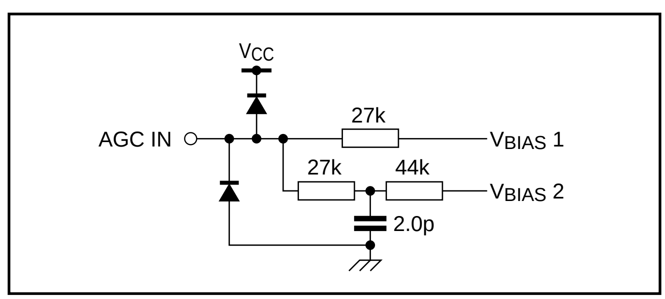


Figure 3h - AGC input

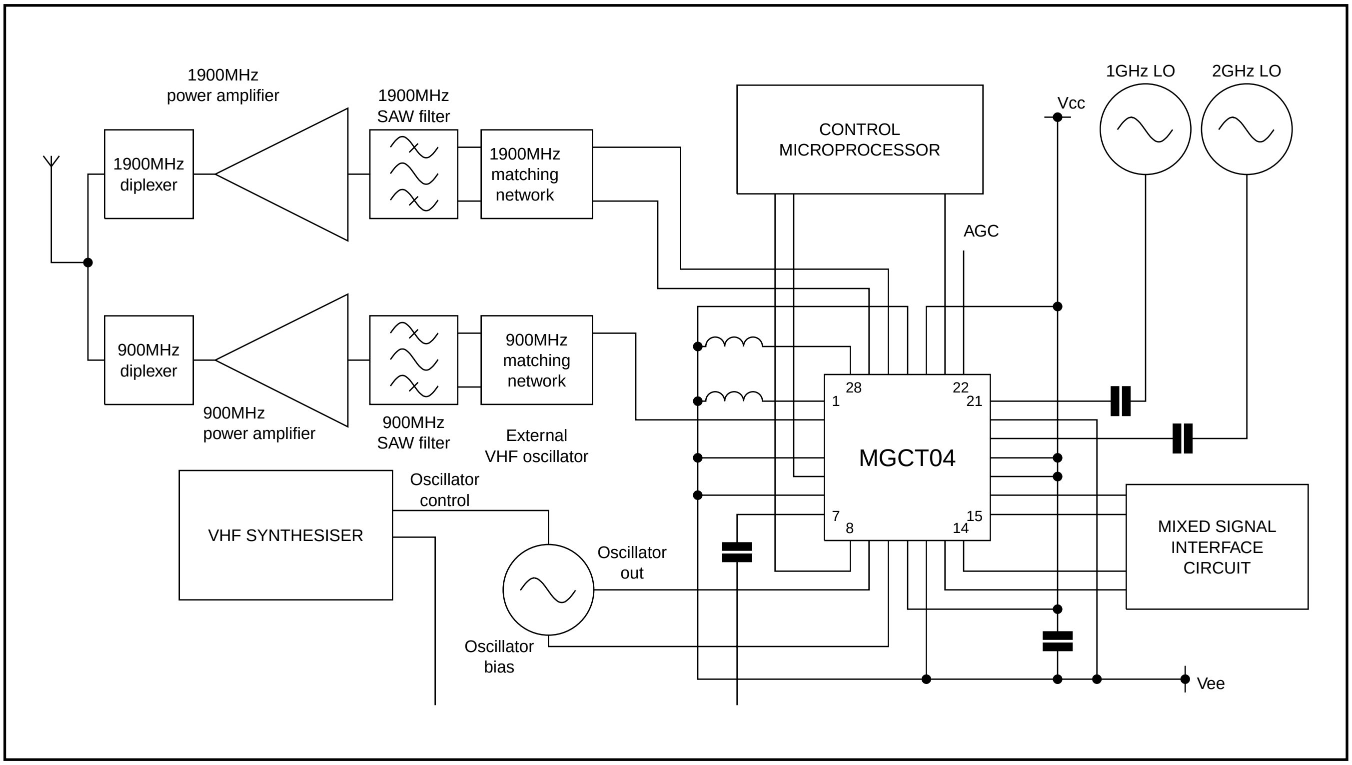


Figure 4 - Typical application circuit

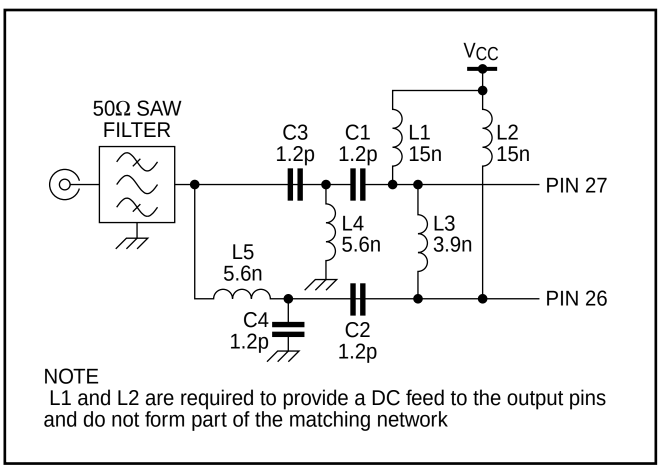


Figure 5 - Typical 1900MHz output matching network

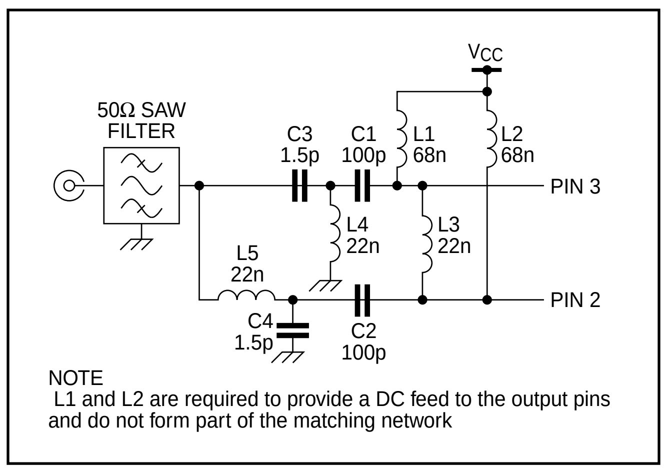


Figure 6 - Typical 900MHz output matching network

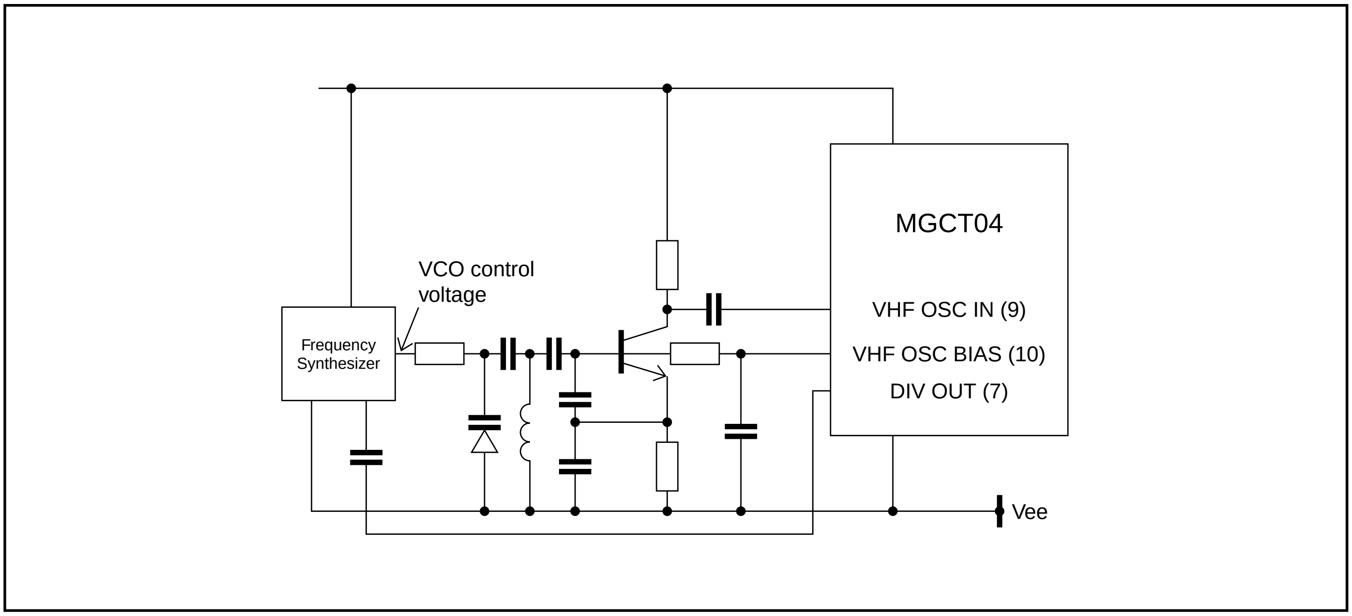


Figure 7 - Typical circuit showing connection of external VHF oscillator

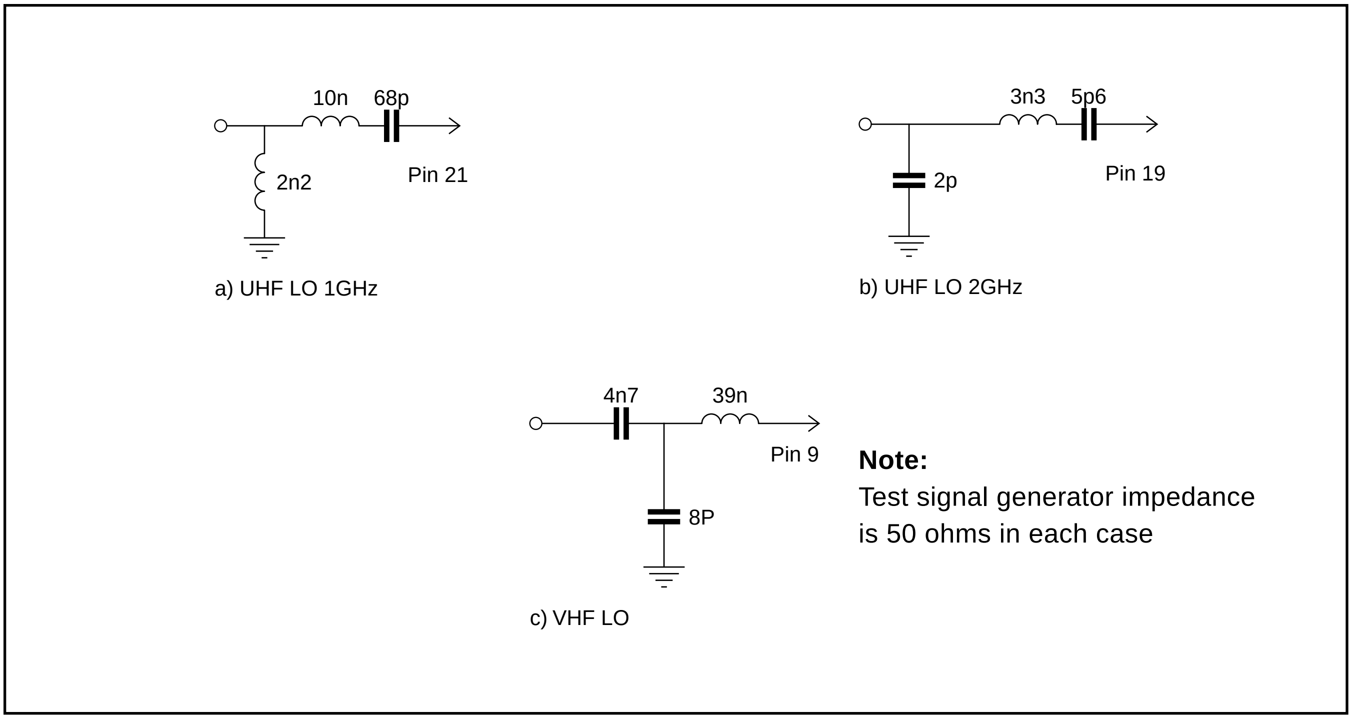
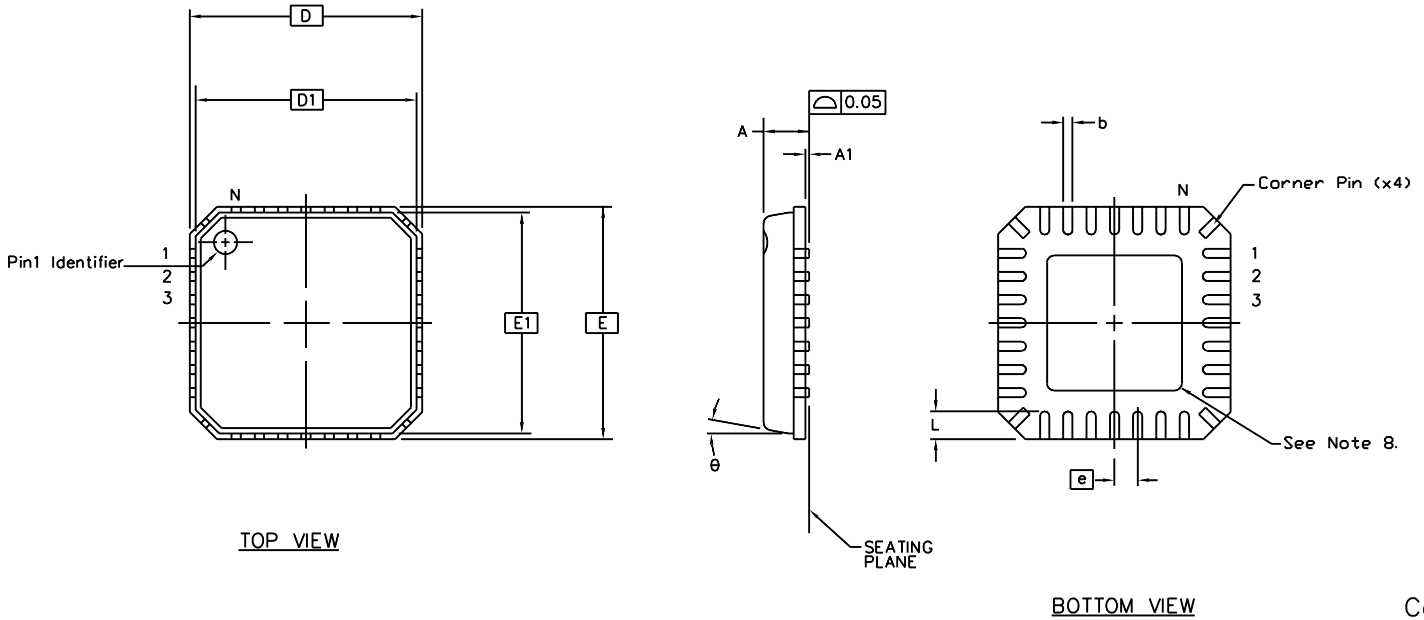


Figure 8 - LO Input Test Circuits



SYMBOL	COMMON DIMENSIONS	
	MIN.	MAX.
A	–	1.00
A1	0.00	0.05
b	0.18	0.30
D	5.00 BSC	
D1	4.75 BSC	
E	5.00 BSC	
E1	4.75 BSC	
N	28	
Nd	7	
Ne	7	
e	0.50 BSC	
L	0.50	0.75
θ	0°	12°

Conforms to JEDEC MO-220 WHHD-1 iss A

NOTES:
1. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
2. N IS THE NUMBER OF TERMINALS.
   Nd & Ne ARE THE NUMBER OF TERMINALS IN X & Y DIRECTION RESPECTIVELY.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.10 AND 0.25mm FROM TERMINAL.
4. ALL DIMENSIONS ARE IN MILLIMETERS.
5. LEAD COUNT IS 28 PLUS 4 CORNER LEADS.
6. PACKAGE WARPAGE MAX 0.05mm.
7. NOT TO SCALE.
8. DIMENSION OF THE EXPOSED METAL PAD MAY BE UPTO 0.20MM SMALLER THAN THE NOMINAL DIE PAD DIMENSION – SEE LEADFRAME DRAWING FOR SPECIFIC PADDLE DIMENSION.

ISSUE	2	3	4	5
ACN	208382	208538	212490	CDCA
DATE	17Feb00	16Mar00	8Apr02	17Dec03
APPRD.				

ZARLINK SEMICONDUCTOR

Package Code LD

Previous package codes LH

Package Outline for Stamped 28 (+4) Lead QFN (5x5mm)

GPD00632

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