Memory/Clock Drivers

MH0013/MH0013C two phase MOS clock driver

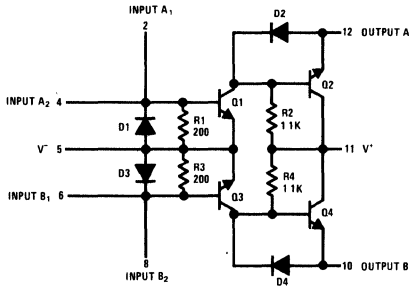
general description

The MH0013/MH0013C is a general purpose clock driver that is designed to be driven by DTL or TTL line drivers or buffers with high output current capability. It will provide fixed width clock pulses for both high threshold and low threshold MOS devices. Two external input coupling capacitors set the pulse width maximum, below which the output pulse width will closely follow the input pulse width or logic control of output pulse width may be obtained by using larger value input capacitors and no input resistors.

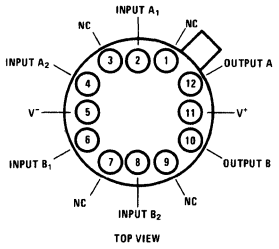
features

- High Output Voltage Swings—up to 30V
- High Output Current Drive Capability—up to 500 mA
- High Repetition Rate—up to 5.0 MHz
- Pin Compatible with the MH0009/MH0009C
- "Zero" Quiescent Power

schematic and connection diagrams

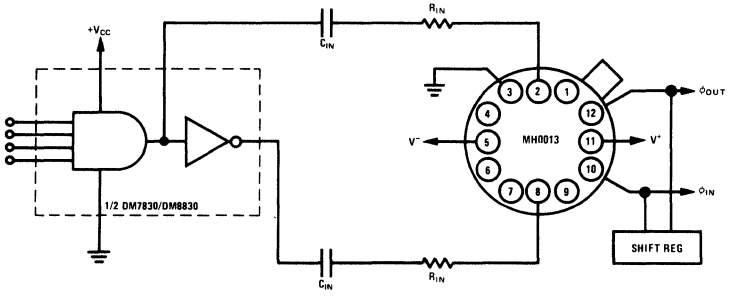


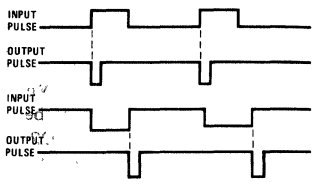
12-Lead TO-8 Package



Order Number MH0013G or MH0013CG
See Package 6

typical applications





absolute maximum ratings

$(V^+ - V^-)$ Voltage Differential	30V
Input Current (Pin 2, 4, 6 or 8)	±75 mA
Peak Output Current	±600 mA
Power Dissipation (Figure 7)	1.5W
Storage Temperature	−65°C to +150°C
Operating Temperature MH0013	−55°C to +125°C
MH0013C	0°C to +85°C
Lead Temperature (Soldering, 10 sec 1/16" from Case)	300°C

electrical characteristics (Note 1 and Figure 8)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "0" Output Voltage	I_{OUT} = −50 mA I_{IN} = 1.0 mA	$V^+ - 3.0$	$V^+ - 1.0$		V
	I_{OUT} = −10 mA I_{IN} = 1.0 mA		$V^+ - 0.7$	$V^+ - 0.5$	V
Logical "1" Output Voltage	I_{OUT} = 50 mA I_{IN} = 10 mA		$V^- + 1.5$	$V^- + 2.0$	V
					V
Power Supply Leakage Current	$(V^+ - V^-)$ = 30V $I_{OUT} = I_{IN}$ = 0 mA		1.0	100	μA
Negative Input Voltage Clamp	I_{IN} = −10 mA	$V^- - 1.2$	$V^- - 0.8$		V
$t_{d\,ON}$			20	35	ns
t_{rise}			35	50	ns
$t_{d\,OFF}$ (Note 2)	C_{IN} = 0.0022 μF R_{IN} = 0Ω		30	60	ns
t_{fall} (Note 2)	C_L = 0.001 μF	40	50	80	ns
t_{fall} (Note 3)		40	70	120	ns
Pulse Width (50% to 50%) (Note 3)		340	420	490	ns
t_{rise}	C_{IN} = 500 pF		15		ns
t_{fall}	R_{IN} = 0Ω		20		ns
Pulse Width (50% to 50%) (Note 3)	C_L = 200 pF		110		ns
Positive Output Voltage Swing			$V^+ - 0.7V$		V
Negative Output Voltage Swing			$V^- + 0.7V$		V

Note 1: Min/Max limits apply over guaranteed operating temperature range of −55°C to +125°C for MH0013 and 0°C to +85°C for MH0013C, with V^- = −20V and V^+ = 0V unless otherwise specified. Typical values are for 25°C

Note 2: Parameter values apply for clock pulse width determined by input pulse width.

Note 3: Parameter values apply for input pulse width greater than output clock pulse width

TABLE I. Typical Drive Capability of One Half MH0013 at 70°C Ambient

$(V_2 - V_3)$ VOLTS	FREQUENCY MHz	PULSE WIDTH ns	TYPICAL R_{IN} Ω	TYPICAL C_{IN} pF	OUTPUT DRIVE CAPABILITY IN pF[1]	RISE TIME LIMIT ns[2]
28					50	–
20	4.0	100	0	750	200	7
16					350	10
28					100	5
20	2.0	200	10	1600	400	14
16					700	19
28					400	19
20	1.0	200	0	2300	1000	34
16					1700	45
28					2800	130
20	0.5	500	10	4000	5500	183
16					9300	248

Note 1: Output load is the maximum load that can be driven at 70°C without exceeding the package rating under the given conditions.

Note 2: The rise time given is the minimum that can be used without exceeding the peak transient output current for the full rated output load.

circuit operation

Input current forced into the base of Q1 through the coupling capacitor C_{IN} causes Q1 to be driven into saturation, swinging the output to $V^- + V_{CE}(SAT) + V_{DIODE}$.

When the input current has decayed, or has been switched, such that Q1 turns off, Q2 receives base drive through R2, turning Q2 on. This supplies current to the load and the output swings positive to $V^+ - V_{BE}$.

It may be noted that Q1 always switches off before Q2 begins to supply current; hence, high internal transient currents from V^+ to V^- cannot occur.

typical performance characteristics

FIGURE 1. Output Load vs Voltage Swing

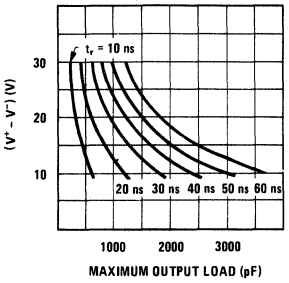


FIGURE 2. Transient Power vs Rep. Rate vs C_L

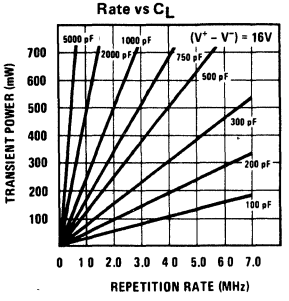


FIGURE 3. Transient Power vs Rep. Rate vs C_L

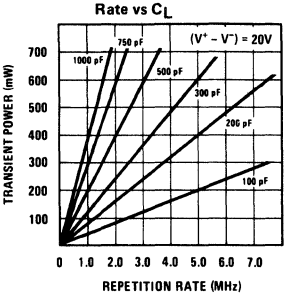


FIGURE 4. Average Internal Power vs Output Swing vs Duty Cycle

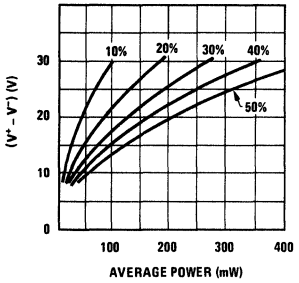


FIGURE 5. Typical Clock Pulse Variations vs Ambient Temperature

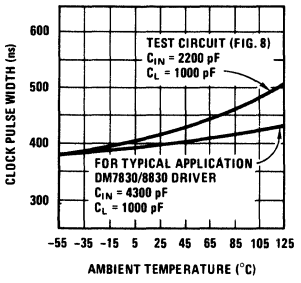


FIGURE 6. R_{IN} vs C_{IN} vs Pulse Width

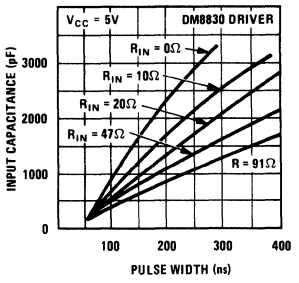
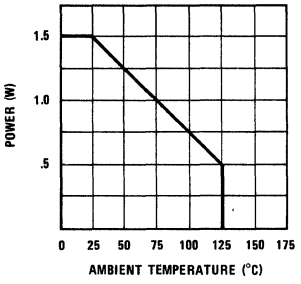
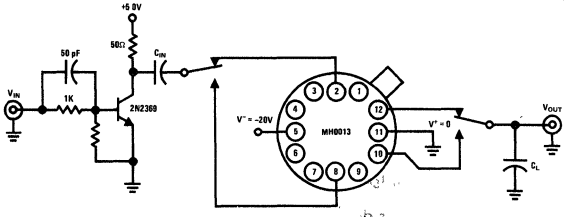


FIGURE 7. Package Power Derating



ac test circuit



V_{IN} = 0 to 5V pulse, f = 500 kHz, DC = 50%, t_r and $t_f \lesssim 10$ ns

timing diagram

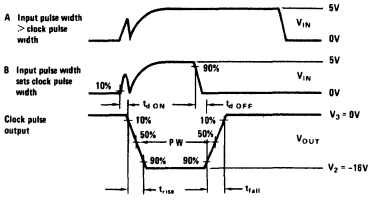


Figure 8

pulse width

Maximum output pulse width is a function of the input driver characteristics and the coupling capacitance and resistance. After being turned on, the input current must fall from its initial value I_{IN} peak to below the input threshold current I_{IN} min $\simeq V_{BE}/R1$ for the clock driver to turn off. For example, referring to the test circuit of Figure 8, the output pulse width, 50% to 50%, is given by

$$pw_{OUT} \cong \frac{1}{2}(t_{rise} + t_{fall}) + R_O C_{IN} \ln \frac{I_{IN}\ peak}{I_{IN}\ min} \cong 400\ ns.$$

For operation with the input pulse shorter than the above maximum pulse width, the output pulse width will be directly determined by the input pulse width.

$$pw_{OUT} = pw_{IN} + t_{d\,OFF} + t_{d\,ON} + \frac{1}{2}(t_{fall} + t_{rise})$$

Typical maximum pulse width for various C_{IN} and R_{IN} values are given in Figure 6.

fan-out calculation

The drive capability of the MH0013 is a function of system requirements, i.e., speed, ambient temperature, voltage swing, drive circuitry, and stray wiring capacity.

The following equations cover the necessary calculations to enable the fan-out to be calculated for any system condition. Some typical fan-outs for conditions are given in Table 1.

Transient Current

The maximum peak output current of the MH0013 is given as 600 mA. Average transient current required from the driver can be calculated from:

$$I = \frac{C_L (V^+ - V^-)}{T_R} \qquad (1)$$

This can give a maximum limit to the load.

Figure 1 shows maximum voltage swing and capacitive load for various rise times

1. *Transient Output Power*

The average transient power (P_{AC}) dissipated is equal to the energy needed to charge and discharge the output capacitive load (C_L) multiplied by the frequency of operation (F)

$$P_{AC} = C_L \times (V^+ - V^-)^2 \times F \qquad (2)$$

Figures 2 and 3 show transient power for two different values of $(V^+ - V^-)$ versus output load and frequency.

2. *Internal Power*

"0" State

Negligible (<3 mW)

"1" State

$$P_{INT} = \frac{(V^+ - V^-)^2}{R_2} \times \text{Duty Cycle.} \qquad (3)$$

Figure 4 gives various values of internal power versus ouptut voltage and duty cycle.

3 *Input Power*

The average input power is a function of the input current and duty cycle. Due to input voltage clamping, this power contribution is small and can therefore be neglected. At maximum duty cycle of 50%, at 25°C, the average input power is less than 10 mW per phase for $R_{IN}C_{IN}$ controlled pulse widths For pulse widths much shorter than $R_{IN}C_{IN}$, and maximum duty cycle of 50%, input power could be as high as 30 mW, since I_{IN} peak is maintained for the full duration of the pulse width

4 *Package Power Dissipation*

Total Average Power = Transient Output Power + Internal Power + Input Power

Typical Example *Calculation for One Half MH0013C*

How many MM506 shift registers can be driven by an MH0013C driver at 1 MHz using a clock pulse width of 400 ns, rise time 30–50 ns and 16 volts amplitude over the temperature range 0–70°C?

Power Dissipation

From the graph of power dissipation versus temperature, Figure 7, it can be seen that an MH0013C at 70°C can dissipate 1W without a heat sink, therefore, each half can dissipate 500 mW.

Transient Peak Current Limitation

From Figure 1 (equation 1), it can be seen that at 16V and 30 ns, the maximum load that can be driven is limited to 1140 pF.

Average Internal Power

Figure 4 (equation 3) gives an average power of 102 mW at 16V 40% duty cycle.

Input power will be a maximum of 8 mW

Transient Output Power

For one half of the MH0013C

500 mW = 102 mW + 8 mW + transient output power

390 mW = transient output power

Using Figure 2 (equation 2) at 16V, 1 MHz and 390 mW, each half of the MH0013C can drive a 1520 pF load. This is, however, in excess of the load derived from the transient current limitation (Figure 1, equation 1), and so a maximum load of 1140 pF would prevail.

From the data sheet for the MM506, the average clock pulse load is 80 pF. Therefore the number of devices driven is $\frac{1140}{80}$ or 14 registers.

For nonsymmetrical clock widths, drive capability is improved.