Memory/Clock Drivers

MH7803/MH8803 two phase oscillator/clock driver

general description

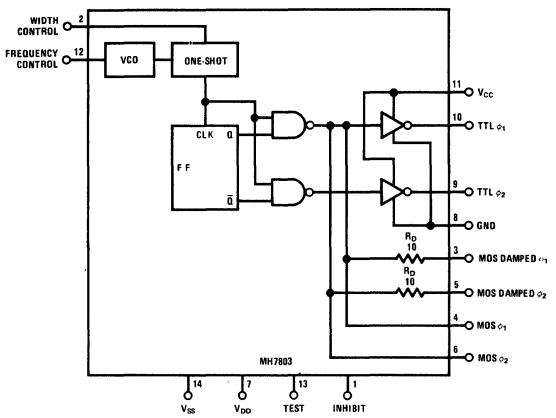
The MH7803 is a self contained two phase oscillator/clock driver. It requires no external components to generate one of three primary oscillator frequencies and pulse widths. Other frequencies can easily be obtained by programming input voltages. Three sets of outputs are provided: damped and un-damped MOS outputs and TTL monitor outputs. The MOS outputs easily drive 500 pF loads with less than 150 ns rise and fall times. In addition the outputs have current limiting to protect against momentary shorts to the supplies.

The MH7803 and MH8803 are available in a 14 lead cavity DIP. The MH8803 is also available in a 14 pin molded DIP.

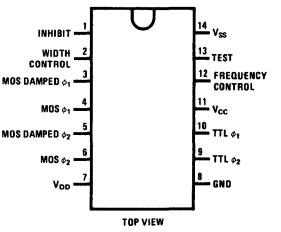
features

- Two phase non-overlapping outputs
- No external timing components required
- Frequency adjustable from 100 kHz to 500 kHz
- Pulse width adjustable from 260 ns to 1.4μs
- Damped and un-damped MOS outputs
- TTL monitor outputs

block and connection diagrams



Dual-In-Line Package



Order Number MH7803J or MH8803J
See Package 16
Order Number MH8803N
See Package 22

absolute maximum ratings

$V_{SS} - V_{DD}$	22V	Operating Temperature Range	
$V_{CC} - GND$	7.0V	MH7803	−55°C to +125°C
Pulse Width Adjust Voltage	V_{SS} + 0.5V	MH8803	0°C to +70°C
Frequency Adjust Voltage	V_{SS} + 0.5V	Storage Temperature Range	−65°C to +150°C
$V_{SS} - V_{DD}$ Minimum	14V	Lead Temperature (Soldering, 10 seconds)	300°C
Test and Inhibit Input Voltages	V_{SS}		

electrical characteristics (Note 1)

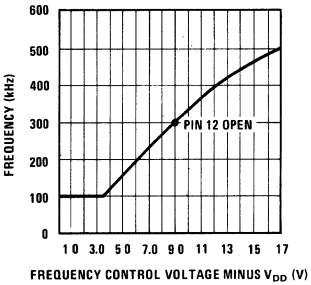
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency	Pin 12 at 17V, T_A = 25°C	300	500	600	kHz
	Pin 12 Open, T_A = 25°C	175	300	350	kHz
	Pin 12 at 0V, T_A = 25°C	60	100	150	kHz
Frequency Change from 25°C					
MH7803	Pin 12 at 17V		±20	±30	%
MH8803	Pin 12 at 17V		±10	±15	%
Pulse Width (Note 2)	Pin 2 at 17V, T_A = 25°C	0 2	0.26	0.4	μs
	Pin 2 Open, T_A = 25°C	0.5	0.75	1.3	μs
	Pin 2 at 0V, T_A = 25°C	1.0	1.4	2.6	μs
Pulse Width Change from 25°C					
MH7803	Pin 2 at 17V		±20	±30	%
MH8803	Pin 2 at 17V		±10	±15	%
MOS V_{OH}	I_{OH} = −100μA	V_{SS}−1 1	V_{SS}−0.8		V
MOS V_{OL}	I_{OL} = 2.0 mA		V_{DD}+0.15	V_{DD}+0.5	V
TTL V_{OH}	I_{OH} = −200μA	2.4	3 7		V
TTL V_{OL}					
MH7803	I_{OL} = 2.0 mA		0.17	0.3	V
MH8803	I_{OL} = 3 2 mA		0 2	0.4	V
TTL I_{OS}		3.0	8.0	15	mA
MOS Output Current Limit			70		mA
I_{SS}	Pins 2, 12, 13 at 0V, and Pin 1 at −0.3V		10	17	mA
I_{CC}	Pins 2, 12, at 0V, and Pin 1 at −0.3V		0.75	1.1	mA
R_D					
MH7803		7.0	10	13	Ω
MH8803		5.0	10	15	Ω
MOS t_R, t_f	C_L = 500 pF, T_A = 25°C		100	150	ns
	C_L = 50 pF, T_A = 25°C		20	30	ns

Note 1: These specifications apply for the MH7803 at $V_{SS} - V_{DD}$ = 17V ±10% and over −55°C to +125°C; for the MH8803 at $V_{SS} - V_{DD}$ = 17V ±5% and over 0°C to +70°C unless otherwise specified.

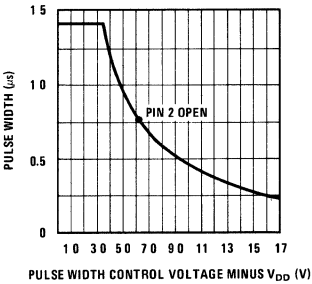
Note 2: The duty cycle can not physically exceed 50% at any output. At high frequencies the frequency adjust pin will affect the pulse width by limiting the duty cycle to slightly less than 50%. Under this condition the pulse width spec does not apply.

typical performance characteristics

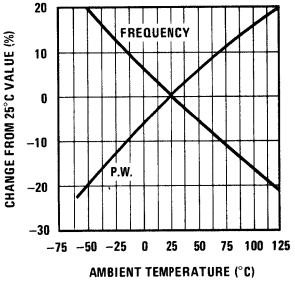
Frequency Control Voltage



Pulse Width Control Voltage

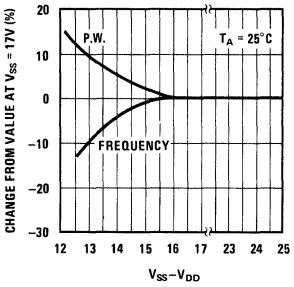


Frequency and Pulse Width vs Temperature

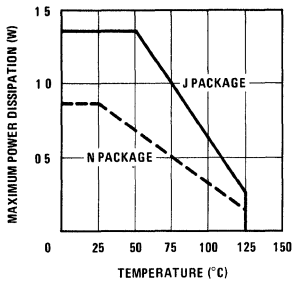


typical performance characteristics (con't)

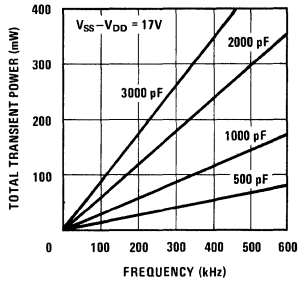
Frequency and Pulse Width vs $V_{SS}-V_{DD}$



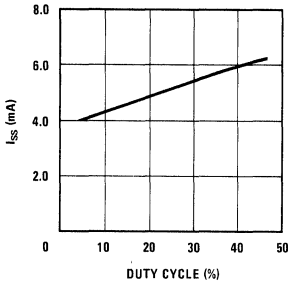
Maximum Package Dissipation



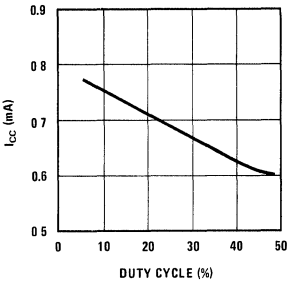
Total Transient Power vs Frequency vs Total C_L



I_{SS} vs Duty Cycle



I_{CC} vs Duty Cycle



applications information

TTL MONITOR OUTPUTS

The TTL outputs are extra functions provided for monitor or synchronization applications. In some systems these outputs may not be required. For these cases the V_{CC} pin may be left open and the TTL circuitry power consumption will be virtually zero.

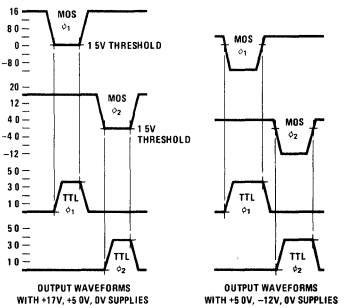
The TTL outputs are slaved to the MOS outputs. Thus the TTL outputs start to switch when the MOS outputs cross the TTL threshold voltage (about 1.5V above ground). Figure 1 depicts the effect of different supply voltages on the TTL waveform when the MOS outputs are driving capacitive loads.

DAMPED MOS OUTPUTS

An extra set of MOS outputs provides a 10 ohm resistor in series with each output line. These resistors give the output pulses an R-C rolloff which tends to minimize ringing or peaking problems associated with board layout.

INHIBIT AND TEST INPUTS

The INHIBIT and TEST inputs are designed to facilitate testing of the device. They were not included in the IC for system use.



(A) (B)

FIGURE 1.

Typically they perform as follows:

INHIBIT Input: in the low state prevents pulses from being initiated on either phase output.

High Level Input:

$$V_{IH} \geq V_{DD} + 2.0V$$

Low Level Input:

$$V_{DD} + 0.2V \geq V_{IL} \geq V_{DD} - 0.5V$$

applications information (con't)

TEST Input: in the low state forces a ONE state on all outputs. The test input should only be used with the INHIBIT input also in the low state.

High Level:

$$V_{IH} \geq V_{DD} + 8.0V$$

Low Level:

$$V_{DD} + 0.5V \geq V_{IL} \geq V_{DD}$$

A pull-up resistor is connected from the TEST pin to V_{SS} internally.

POWER CONSIDERATIONS

Internal power dissipation is affected by three factors:

- dc power
- ac power
- package dissipation capability

The total average power dissipation is the summation of the dc power and ac power. This sum must be less than the maximum package dissipation capability at the particular operating temperature to insure safe operation, i.e.:

$$P_{DISS} = P_{AC} + P_{DC} \leq P_{MAX}$$

Where

$$P_{AC} = P_{AC\,TTL} + P_{AC\,MOS}$$

$$P_{AC} = [(V_{CC} - GND)^2 \times f \times C_L]_{TTL} + [(V_{SS} - V_{DD})^2 \times f \times C_L]_{MOS}$$

And

$$P_{DC} = (I_{CC}) \times (V_{CC} - GND) + (I_{SS}) \times (V_{SS} - V_{DD})$$

for I_{CC} and I_{SS} selected at the appropriate duty cycle.

For practical cases the $P_{AC\,TTL}$ can be neglected as being very small compared to $P_{AC\,MOS}$.

Thus P_{DISS} is the sum of the MOS transient power (total for both sides of the MH7803) and the standby power of the TTL and MOS sections of the MH7803.

DECOUPLING

It is recommended that each device be decoupled with a 0.1μF capacitor from V_{SS} to V_{DD}. If there is noise on the supply lines, better frequency and pulse width stability can be obtained by connecting a 0.001μF capacitor from the frequency control pin to V_{DD} and another 0.001μF capacitor from the pulse width control pin to V_{DD}.

Memory/Clock Drivers

MH8808 dual high speed MOS clock driver

general description

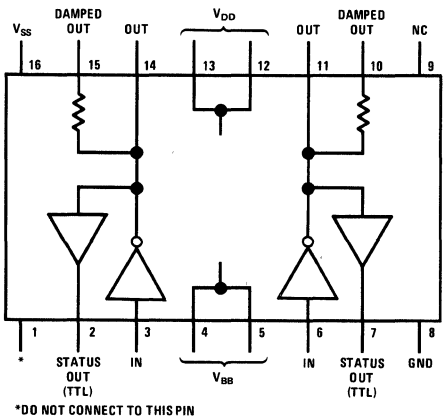
The MH8808 is a high speed dual MOS clock driver intended to drive the two phases of a memory array of 500 pF per phase at rates up to 4 MHz. The design includes output current limiting for controlled rise and fall times, and thermal shutdown which protects the chip against excessive power dissipation or accidental output shorts. Two DTL/TTL compatible status outputs monitor clock outputs and provide a corresponding TTL logic level for status indication. Both direct and internally damped outputs are available for each phase to suit the particular application. It is ideally suited for driving MM5262 2k RAMs.

features

- High Speed: 18 ns typ delay and 20 ns typ rise and fall times with 500 pF load
- Current limited outputs ±450 mA typ
- Direct and damped outputs available
- Thermal shutdown protection
- TTL compatible status outputs
- 1W dissipation capability at 25°C T_A
- 16 pin cavity dual-in-line package
- Output high level clamped to +5V

connection diagram

Dual-In-Line Package



*DO NOT CONNECT TO THIS PIN

TOP VIEW

Order Number MH8808J
See Package 17

Order Number MH8808N
See Package 23