# Memory/Clock Drivers

## MH8808 dual high speed MOS clock driver

### general description

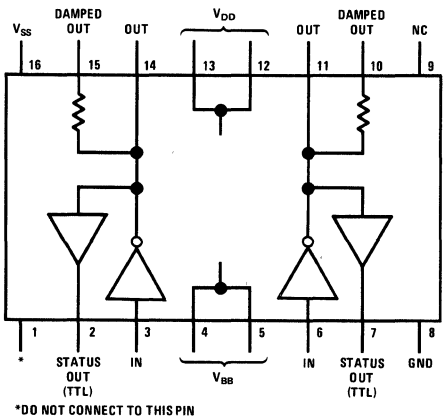
The MH8808 is a high speed dual MOS clock driver intended to drive the two phases of a memory array of 500 pF per phase at rates up to 4 MHz. The design includes output current limiting for controlled rise and fall times, and thermal shutdown which protects the chip against excessive power dissipation or accidental output shorts. Two DTL/TTL compatible status outputs monitor clock outputs and provide a corresponding TTL logic level for status indication. Both direct and internally damped outputs are available for each phase to suit the particular application. It is ideally suited for driving MM5262 2k RAMs.

### features

- High Speed: 18 ns typ delay and 20 ns typ rise and fall times with 500 pF load
- Current limited outputs ±450 mA typ
- Direct and damped outputs available
- Thermal shutdown protection
- TTL compatible status outputs
- 1W dissipation capability at 25°C $T_A$
- 16 pin cavity dual-in-line package
- Output high level clamped to +5V

### connection diagram

**Dual-In-Line Package**




*DO NOT CONNECT TO THIS PIN

TOP VIEW

**Order Number MH8808J**
**See Package 17**

**Order Number MH8808N**
**See Package 23**

## absolute maximum ratings

| | |
|---|---|
| $V_{SS}$ | +7V |
| $V_{BB} - V_{DD}$ | 26V |
| Total Power Dissipation (Note 1) | 1W |
| Operating Temperature Range | 0°C to +70°C |

## electrical characteristics

The following apply for $V_{BB}$ = +7V, $V_{SS}$ = +5V, $V_{DD}$ = −15V, $T_A$ = 25°C unless otherwise stated

| PARAMETER | CONDITIONS | MIN | MAX | UNITS |
|---|---|---|---|---|
| Input Current | $V_{IN}$ = −9V (Note 2) | | 10 | mA |
| Output Low Voltage | $I_{OUT}$ = +1 mA, $V_{IN}$ = −10V (Note 2) | −14 | | V |
| Output High Voltage | $I_{OUT}$ = −1 mA, $V_{IN}$ = −14V | 4 5 | 5 3 | V |
| Status "1" Voltage | $I_{OUT}$ = −250 μA, $V_{IN}$ = −14V | 3 | | V |
| Status "0" Voltage | $I_{OUT}$ = 20 mA, $V_{IN}$ = −10V (Note 2) | | 0 5 | V |
| Output Leakage Current | $V_{BB}$ = +8 5V, $V_{SS}$ = 5V<br>$V_{DD}$ = −17 5V, $V_{OUT}$ = +8 5V<br>$V_{IN}$ = open | | 100 | μA |
| Damping Resistor | | 4 | | Ω |
| $I_{BB}$ | $V_{IN}$ = −11 5V<br>$V_{SS}$ = +6 5V, $V_{DD}$ = −17 5V<br>$V_{BB}$ = +8 5V (Note 2) | | 32 | mA |
| $I_{SS}$ | $V_{IN}$ = −11 5V<br>$V_{SS}$ = +6 5V, $V_{DD}$ = −17 5V<br>$V_{BB}$ = +8 5V (Note 2) | | 23 | mA |
| $I_{DD}$ | $V_{IN}$ = −11 5V<br>$V_{SS}$ = +6 5V, $V_{DD}$ = −17 5V<br>$V_{BB}$ = +8 5V (Note 2) | | −55 | mA |
| Output Rise Time | $C_L$ = 500 pF | | 26 | ns |
| Output Fall Time | $C_L$ = 500 pF | | 26 | ns |
| Delay to Negative-Going Output | $C_L$ = 500 pF | 7 | 22 | ns |
| Delay to Positive-Going Output | $C_L$ = 500 pF | 10 | 25 | ns |

**Note 1:** Maximum junction temperature is +125°C. For operation above +25°C derate at +80°C/W $\theta_{JA}$ for still air.
**Note 2:** Test only one input high (more positive) at a time.