MH89792

E1 Line Interface Unit (LIU)

Data Sheet

DS5712 Issue 4 March 2002

Features

- Complete primary rate 2048kbit/s E1line driver and receiver with clock recovery
- Meets ETSI requirements (ETSI ETS 300 011, NET 5)
- Onboard pulse transformers for transmit and receive
- No external crystal required for clock recovery
- Loss of signal indication
- Programmable polarity of extracted clock and receive data
- Compatible with MT8979, MT9079 and other E1 framers
- Single +5V operation
- Single In-Line (SIL) package occupying only 490mm^2 area

Applications

- Primary rate ISDN network Interfaces
- Multiplexer equipment

Ordering Information

MH89792-1	20 Pin SIL Package
MH89792-2	20 Pin SIL Package

-40°C to 85°C

- E1 Digital Loop Carrier (DLC) equipment
- Digital Cross-connect Systems (DCS)

Description

The Zarlink MH89792 is an E1 line interface unit (LIU) designed to meet the requirements of G.703 2048 kbit/s transmission. It incorporates all of the analog front-end components necessary to realize a complete, fully compliant short-haul E1 analog termination. These include, clock extractor, line driver/receiver, impedance matching resistors, and line transformers. No external components, such as crystals, inductors or transformers are required. An external clock reference is also not required. Two line impedance versions are available for 75Ω and 120Ω applications. See ordering information for details.

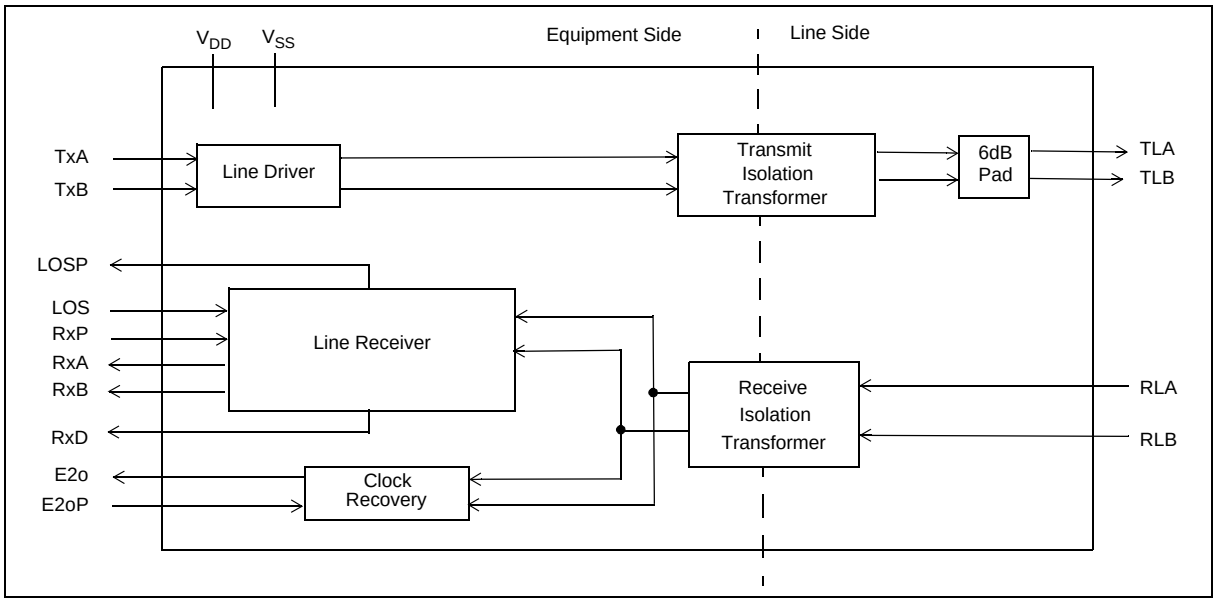

Figure 1 - Functional Block Diagram

The MH89792 is compatible with the Zarlink MT8979 and MT9079 E1 digital framers, as well as other commercially available E1 framers. The MH89792 requires only a single +5 volt supply. The device is manufactured in a 20 pin Single In-Line (SIL) package. This package uses minimal board space area, making it optimal for high density E1 line card designs.

Pin Connections

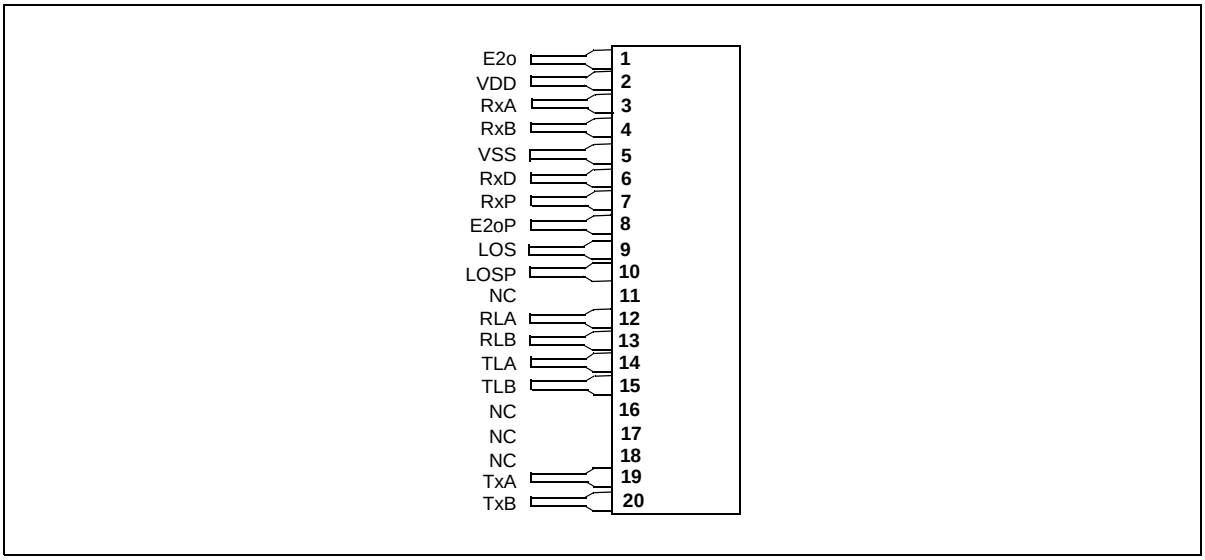

Figure 2 - Pin Connections

Pin Description

Pin #	Name	Description
1	E2o	**2048kHz Extracted clock (Output).** This clock is extracted by the device from the received signal. It is used internally to clock in data received from RLA and RLB.
2	V_{DD}	**Positive Power Supply (Input).** +5V supply
3	RxA	**Receiver A (Output).** The E1 signal received by the device at the RLA and RLB inputs is converted to return to zero (RZ) format and output at this pin. This output should be connected to the RxA or $\overline{RxA}$ of the E1 framer.
4	RxB	**Receiver B (Output).** The E1 signal received by the device at the RLA and RLB inputs is converted to return to zero (RZ) format and output at this pin. This output should be connected to the RxB or $\overline{RxB}$ of the E1 framer.
5	V_{SS}	**Negative Power supply (Input).** Ground.
6	RxD	**Received Data (Output).** This signal is the logically “OR” ed product of the RxA and RxB signals and should be connected to RxD of the MT8979.
7	RxP	**RxA/RxB Polarity Select (Input).** A logic low applied to this pin will invert the outputs RxA and RxB (MT8979 application). A logic high should be applied if no inversion is required (MT9079 application).
8	E2oP	**Clock Polarity Select (Input).** A logic low selects E2o with a falling edge in the centre of RxD. A logic high selects E2o with a rising edge in the centre of RxD.
9	LOS	**Loss of Signal (Output).** This pin goes low when 128 consecutive zeros are received on the RLA and RLB inputs. If a loss of signal condition is detected (LOS is low) then RxA and RxB are forced high if RxP is low. RxA and RxB are forced low if RxP is high. When 64 ones are received in 512 a bit period, the LOS condition is cleared (LOS is high).

Pin Description (continued)

Pin #	Name	Description
10	LOSP	**Loss of Signal Polarity Select (Input).** A logic low applied to this pin will invert the polarity of the LOS output signal.
11	NC	**No connection.** This pin is not fitted.
12	RLA	**Received Line A (Input)**. The A wire or Tip Connection of the E1 receive line should be connected to this pin.
13	RLB	**Receive Line B (Input).** The B wire or Ring connection of the E1 receive line should be connected to this pin.
14	TLA	**Transmit Line A(Output).** The A wire or Tip connection of the E1 transmit line should be connected to this pin.
15	TLB	**Transmit Line B (Output).** The B wire or Ring connection of the E1 transmit line should be connected to this pin.
16	NC	**No Connection.** This pin is not fitted.
17	NC	**No Connection.** This pin is not fitted.
18	NC	**No Connection.** This pin is not fitted.
19	TxA	**Transmit A (Input).** This input should be connected to the TxA output of the framer. This signal must be a return to zero (RZ) form of the transmit data.
20	TxB	**Transmit B (Input).** This input should be connected to the TxB output of the framer. This signal must be a return to zero (RZ) form of the transmit data.

Functional Description

The MH89792 is an E1 digital trunk interface, which when used with an MT8979 and MT9079 framer will conform to CCITT recommendation G.703 for PCM30 and I.431 for ISDN. The functions provided include line driver and receiver circuitry, clock recovery, loss of signal indication, as well as data and clock polarity selection.

Bipolar Line Receiver

The MH89792 receiver interfaces to the transmission line through an internal pulse transformer, which isolates the line side from the equipment side of the circuit. These two signals are combined by internal logic to form a new signal, which represents the received data, RxD. The signals RxA and RxB may be inverted where required by applying a logic low signal permanently to pin 7, (RxP). RxD will not be affected by use of this pin.

The input impedance of the MH89792 receiver is nominally 120Ω when using the -1 variant (twisted pair applications), and nominally 75Ω when using the -2 variant (coaxial cable applications).

The receiver input sensitivity exceeds G.703 requirements.

Clock Extractor

The MH89792 contains a clock extraction circuit which generates the E2o clock from the received data without the use of an external crystal or tunable inductor.

The edge of the E2o extracted clock aligns approximately with the centre of the received data pulse and can be configured as either a rising or falling edge format by the use of pin 8 (E2oP).

During a loss of signal condition, the E2o clock output will free-run at a nominal frequency of 2.048 kHz ± 200 ppm.

The input jitter tolerance of the MH89792 exceeds the minimum jitter tolerance as specified in CCITT I.431 and G.823 (see Figure 3).

Loss of Signal

The circuitry on the MH89792 is capable of detecting 128 continuous ZEROs received on RLA and RLB and indicating this condition as a logic low on pin 9, (LOS). If a loss of signal condition is detected (LOS is low) then RxA and RxB are forced high if RxP is low. RxA and RxB are forced low if RxP is high. LOS will not reset until 64 ONEs are received in a 512 bit period. The action of LOS may be inverted by applying a logic low to pin 10 (LOSP).

A zero level is defined by voltage on the line, being less than 1.5V.

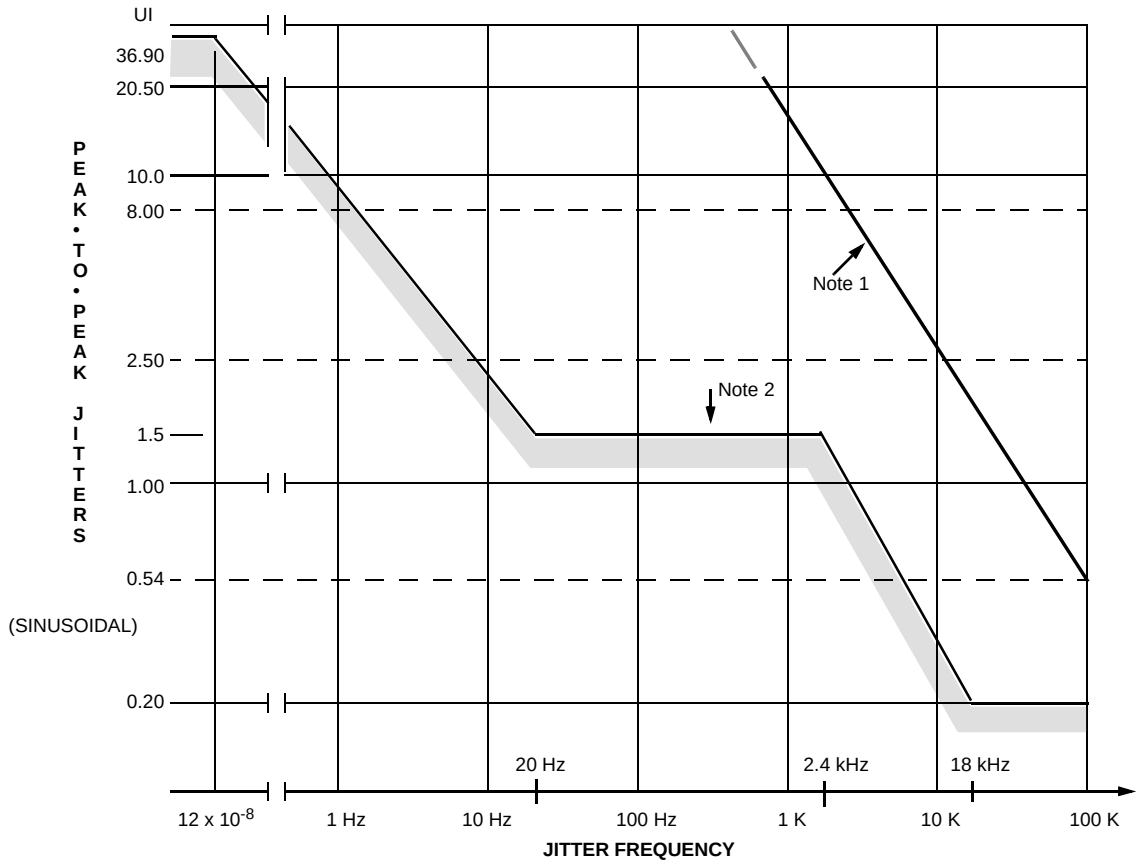

Figure 3 - Typical Input Jitter Tolerance of MH89792

Note 1 - Typical jitter tolerance of receiver

Note 2 - Minimum jitter tolerance specified by G.823 and I.431

Bipolar Line Transmitter

The MH89792 transmitter interfaces to the transmission line through an internal pulse transformer which combines the TxA and TxB data into an AMI line coded signal. This is then passed through the 6dB pad prior to being applied to the line to meet return loss requirements.

Functional timing for the transmitter is shown in Figure 4.

The template for the transmitted pulse is shown in Figure 5. The nominal peak voltage of a mark is 3 volts for 120Ω twisted pair applications and 2.37 volts for 75Ω coax applications. The ratio of the amplitude of the positive and negative pulses of the transmit signals is between 0.95 and 1.05.

No jitter is added by the transmitter circuitry.

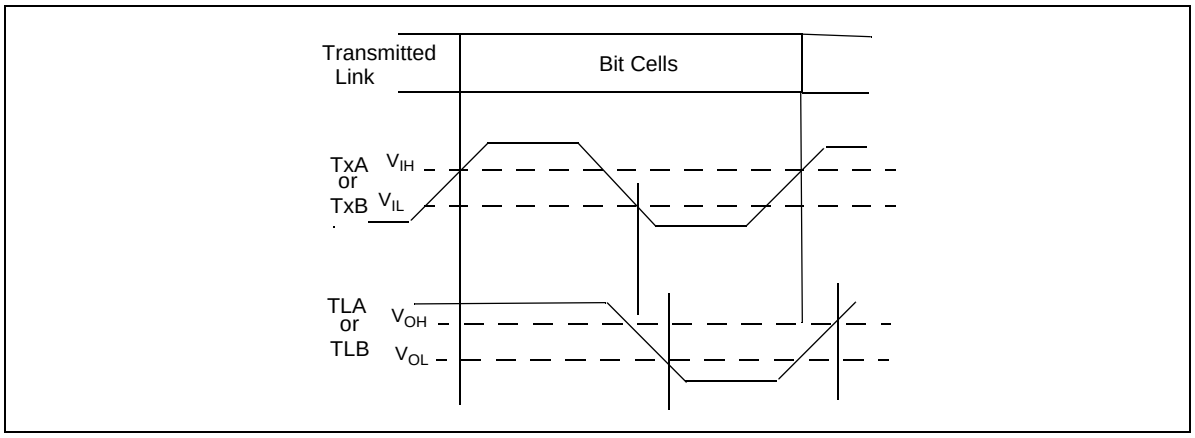

Figure 4 - Functional Timing for Transmitter

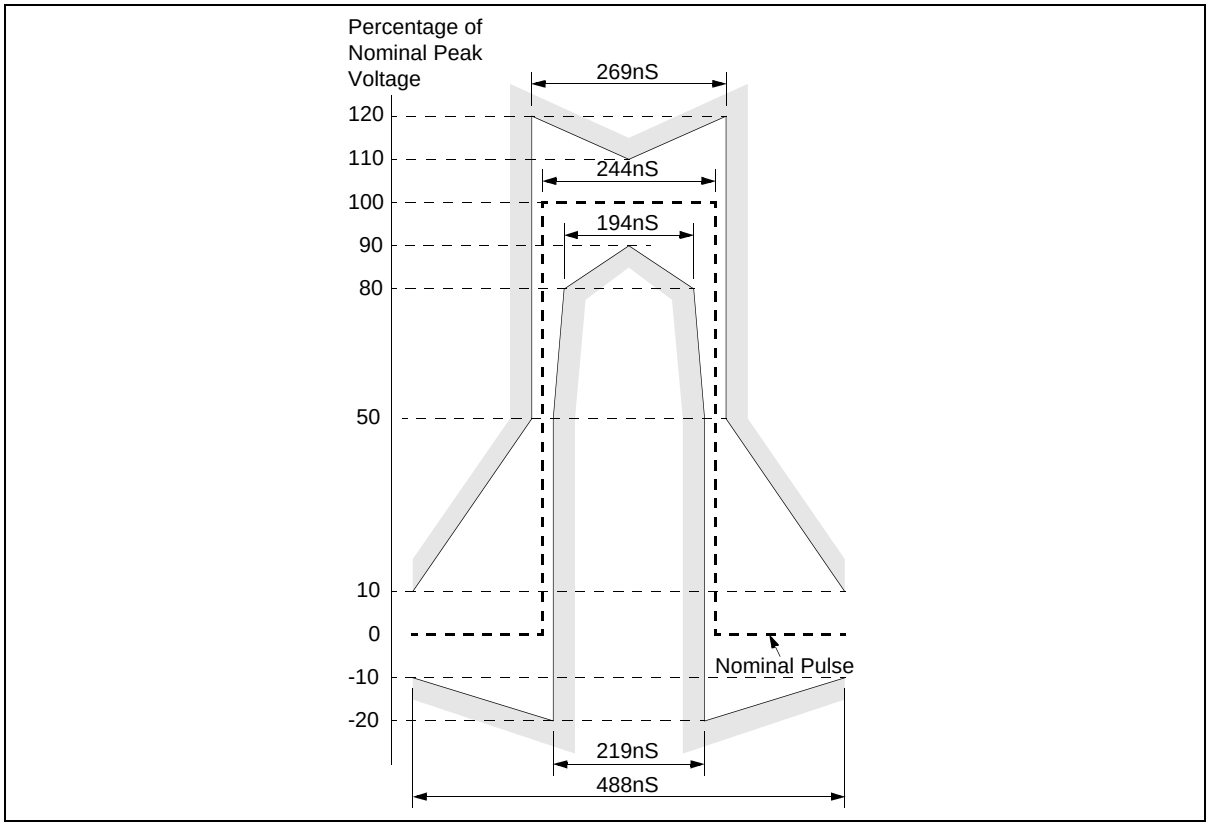

Figure 5 - Pulse Template (CCITT G.703)

Applications

Three typical 2.048 MHz E1/CEPT application are shown in Figures 6 and 7. Figure 6 shows the MH89792-1(120Ω) with the MT8979 framer . Figure 7 shows the MH89792-1 (120Ω) with the MT9079 advanced framer. Figure 8 shows the configuration of MH89792-2 (75Ω).

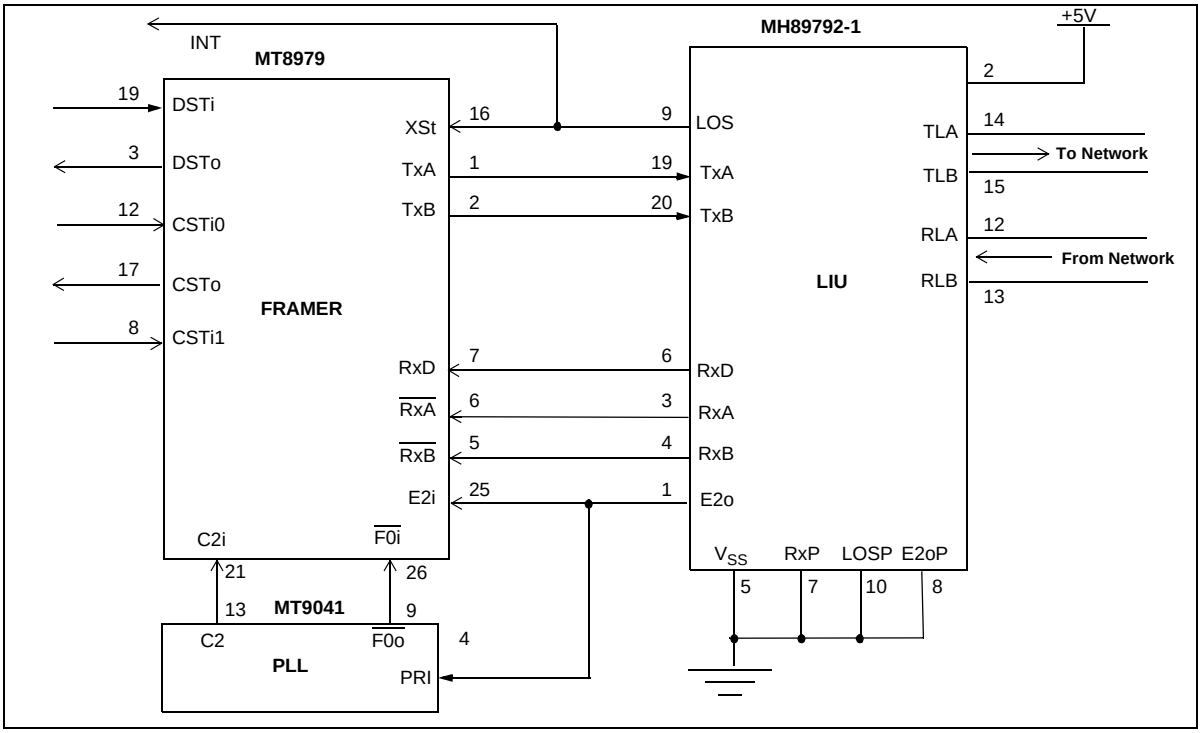

Figure 6 - Connection Diagram for MH89792-1 with MT8979 and MT9041

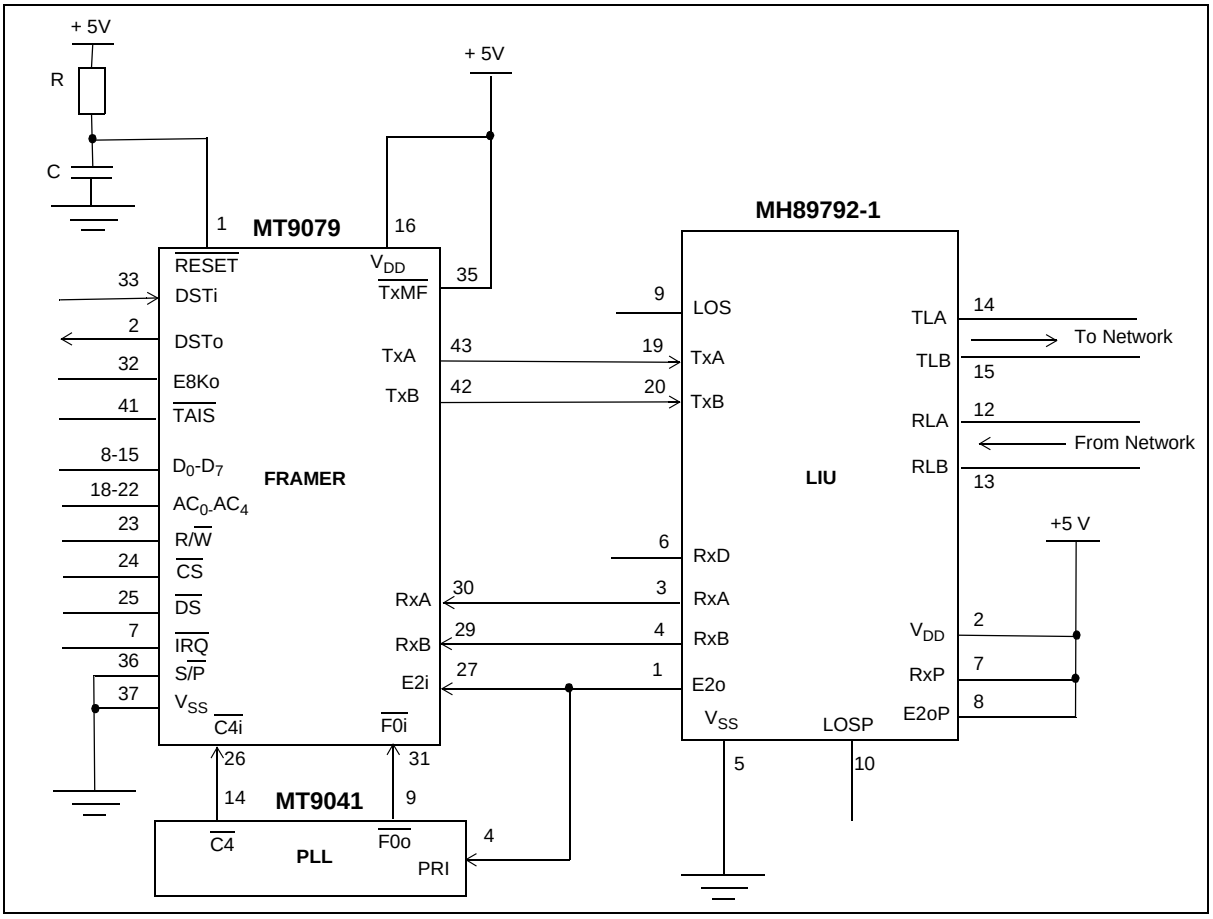

Figure 7 - Connection Diagram for MH89792-1 with MT9079 and MT9041

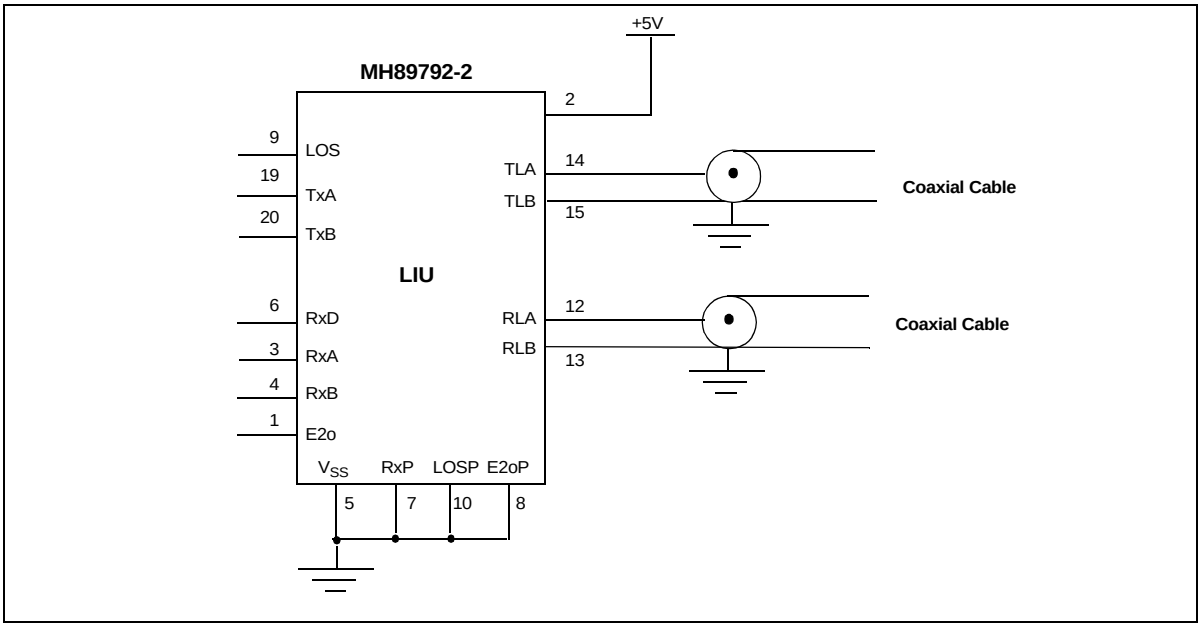

Figure 8 - Configuration of MH89792-2 for 75W Coaxial Cable

Line Protection Circuitry

The MH89792 possesses minimal line protection capability. In order to meet relevant standards governing overvoltage/overcurrent stresses from lightening strikes and other surges, an external protection network is required.

For information on suggested external line protection circuitry, please consult the factory.

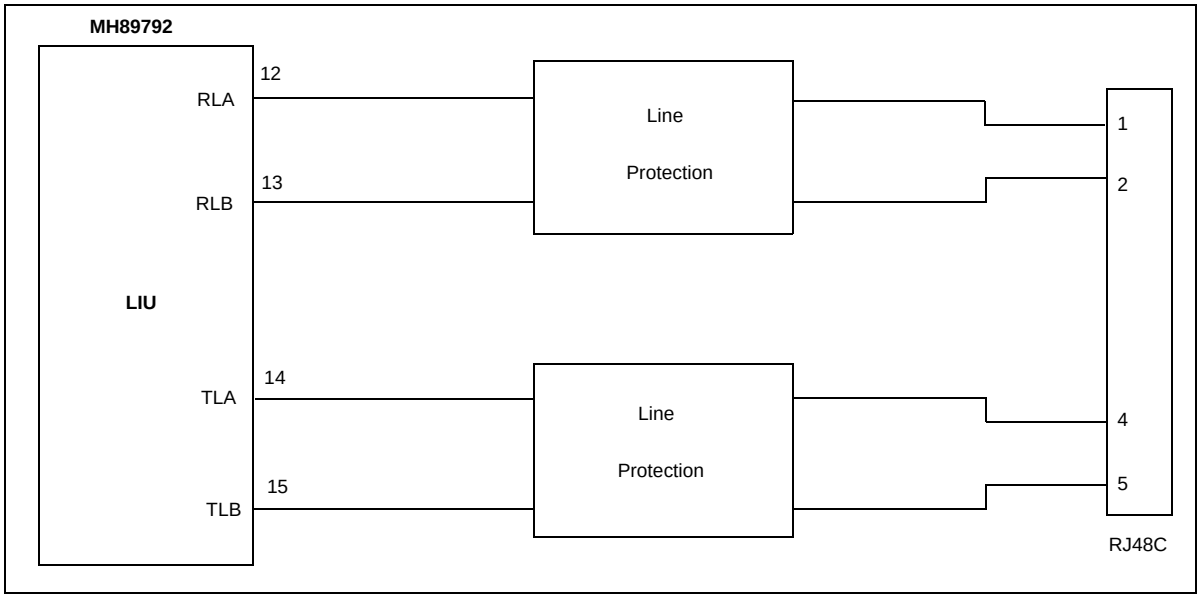

Figure 9 - Protection Circuitry Requirement

Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	Supply Voltage with respect to V_{SS}	V_{DD}	-	6	V
2	Voltage on any pin other than supplies		V_{SS}-0.3	V_{DD}+0.3	V
3	Current at any pin other than supplies		-	40	mA
4	Storage Temperature	T_{ST}	-40	85	°C
5	Package Power Dissipation	P_D		1	W

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Symbol	Min	Typ‡	Max	Units
1	Operating Temperature	T_{OP}	0	-	70	°C
2	Supply Voltage	V_{DD}	4.75	5.0	5.25	V

DC Electrical Characteristics - Clocked operation over recommended temperature ranges and power supply voltages

	Parameters	Sym	Min	Typ‡	Max	Units	Conditions
1	Supply Current	I_{DD}		10	30	mA	Outputs Unloaded
2	Input High Voltage	V_{IH}	2.0		V_{DD}	V	
3	Input Low Voltage	V_{IL}	0.0		0.8	V	
4	Input Leakage Current	I_{IL}		$\pm$1	$\pm$10	µA	V_I = 0 to V_{DD}
5	Output High Voltage	V_{OH}	2.4		V_{DD}	V	I_{OH}=7 mA @ V_{OH}=2.4 V
	Output High Current	I_{OH}	7	20		mA	Source V_{OH}=2.4 V
6	Output Low Voltage	V_{OL}	V_{SS}		0.4	V	I_{OL}= 2 mA @ V_{OL}=0.4 V
	Output Low Current	I_{OL}	2	10		mA	Sink V_{OL}=0.4 V

AC Electrical Characteristics - Timing Parameter Measurement Voltage Levels

	Characteristics	Sym	Level	Units	Conditions
1	TTL Threshold Voltage	V_{TT}	1.5	V	See Note 1
2	CMOS Threshold Voltage	V_{CT}	0.5V_{DD}	V	See Note 1
3	Rise/Fall Threshold Voltage High	V_{HM}	2.0 0.7V_{DD}	V V	TTL CMOS
4	Rise/Fall Threshold Voltage Low	V_{LM}	0.8 0.3V_{DD}	V V	TTL CMOS

Notes:

1. Timing for output signals is based on the worst case result of the combination of TTL and CMOS threshold.

AC Electrical Characteristics - Capacitance

	Characteristics	Sym	Min	Typ‡	Max	Units
1	Input Pin Capacitance	C_1		10		pF
2	Output Pin Capacitance	C_0		10		pF

AC Electrical Characteristics† - Line Transmitter (T_{ST} = 0 °C to 70 °C; V_{DD} = 5.0 V ±5%; V_{SS} = 0V)

	Parameter	Min	Typ‡	Max	Units	Conditions
1	AMI Output Pulse Amplitudes MH89792-2 (75Ω) MH89792-1(120Ω)	 2.14 2.7	 2.37 3	 2.6 3.3	 V V	 Terminated with a 75Ω Load Terminated with a 120Ω Load
2	Transmitter Return Loss (for 75Ω)	 8 14 10	 13 18 15	 - -	 dB dB dB	Measured with transmitter in idle state 51 KHz to 102 KHz 102 KHz to 2.048 MHz 2.048 MHz to 3.072 MHz
3	Transmitter Return Loss (for 120Ω)	 8 14 10	 14 18 15	 - - -	 dB dB dB	Measured with transmitter in idle state 51 KHz to 102 KHz 102 KHz to 2.048 MHz 2.048 MHz to 3.072 MHz
4	Isolation Voltage	1.5			KVrms	

AC Electrical Characteristics† - Line Receiver (T_{ST} = 0 °C to 70 °C; V_{DD} = 5.0 V ±5%; V_{SS} = 0V)

	Parameter	Min	Typ‡	Max	Units	Conditions
1	Receiver Input Jitter Tolerance	 0.2 1.5	 1.7 11	 - -	 UI UI	 18 KHz - 100 KHz 2.4KHz
2	Receiver Return Loss (for 75Ω)	 12 18 14	 23 27 20	 - - -	 dB dB dB	 51 KHz to 102 KHz 102 KHz to 2.048 MHz 2.048 MHz to 3.072 MHz
3	Receiver Return Loss (for 120Ω)	 12 18 14	 23 28 25	 - - -	 dB dB dB	 51 KHz to 102 KHz 102 KHz to 2.048 MHz 2.048 MHz to 3.072 MHz
4	Loss of Signal Threshold	1.5			V	
5	Receive Sensitivity	6			dB	

AC Electrical Characteristics† - Link Timing (Figure 10)

	Characteristics	Sym	Min	Typ‡	Max	Units	Conditions
1	E2o Clock Period	t_{PEC}	439	488	537	ns	
2	E2o Clock Width High or Low	t_{WEC}	195	244	293	ns	
3	Receive Data Setup Time	t_{RDS}	98			ns	Note 1
4	Receive Data Hold Time	t_{RDH}	49			ns	Note 1
5	Receive Data Pulse Width	t_{RDW}	195	244	293	ns	
6	Receive Data Fall Time	t_{RDF}			20	ns	
7	Receive Data Rise Time	t_{RDR}			30	ns	

Note 1: The parameter t_{RDS} and t_{RDH} are related to device functionality

† Timing is over recommended operating temperature and power supply voltage ranges.

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

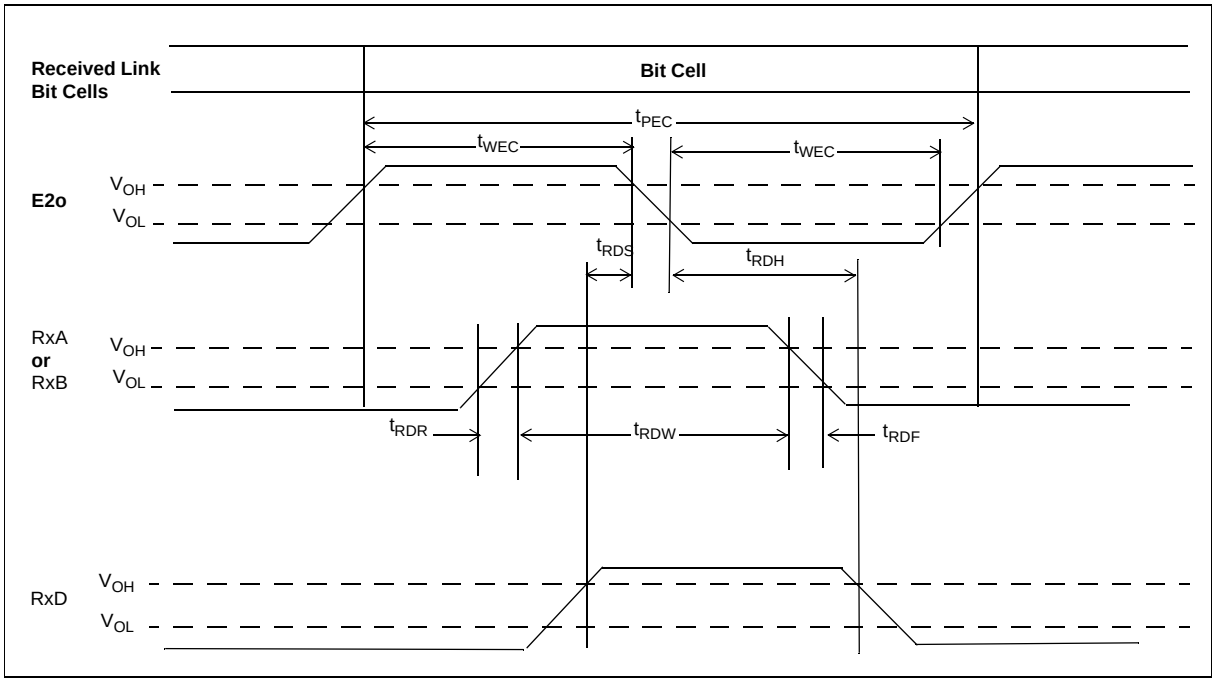

Figure 10 - Receive Timing Link

Note: 1. RxP is High and E2oP is High.

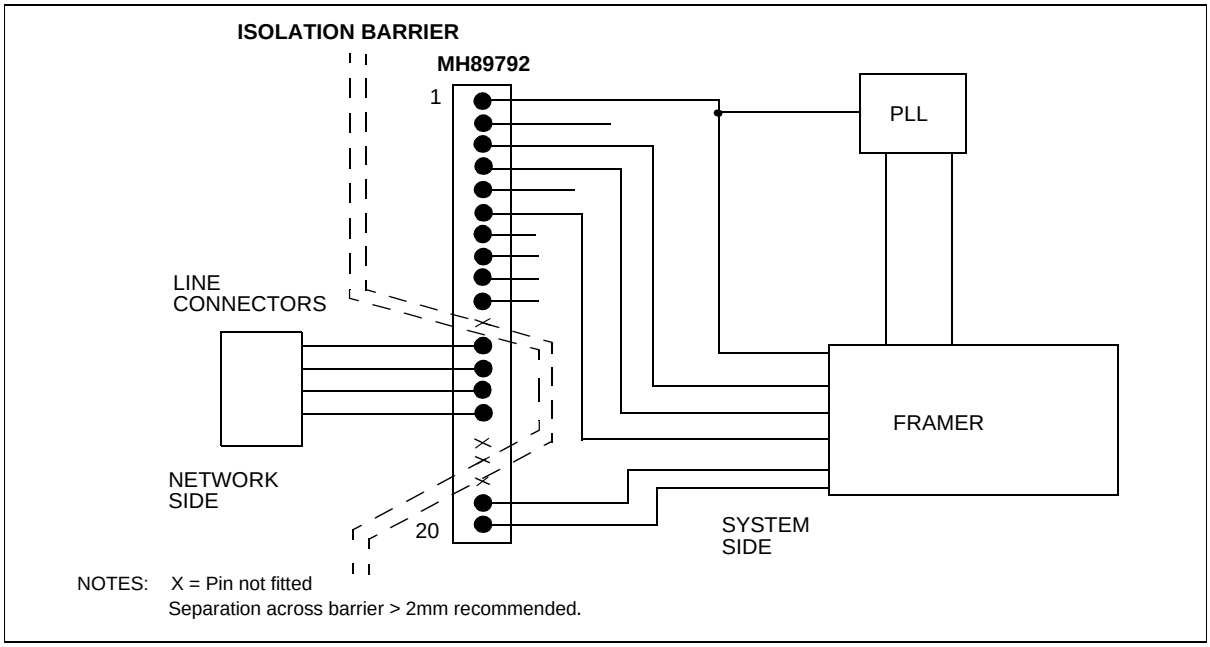

Figure 11 - Recommended Component Placement

For more information about all Zarlink products
visit our Web Site at

www.zarlink.com