C141-E050-02EN

MHC2032AT, MHC2040AT
MHD2032AT, MHD2021AT
DISK DRIVES

PRODUCT MANUAL

FUJITSU

FOR SAFE OPERATION

Handling of This Manual

This manual contains important information for using this product. Read thoroughly before using the product. Use this product only after thoroughly reading and understanding especially the section “Important Alert Items” in this manual. Keep this manual handy, and keep it carefully.

FUJITSU makes every effort to prevent users and bystanders from being injured or from suffering damage to their property. Use the product according to this manual.

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C141-E050-02EN

Revision History

Edition	Date	Revised section (*1) (Added/Deleted/Altered)	Details
01	1998-02-15	—	—
02	1998-0-		

*1 Section(s) with asterisk (*) refer to the previous edition when those were deleted.

Preface

This manual describes the MHC Series and MHD Series, 2.5-inch hard disk drives. These drives have a built-in controller that is compatible with the ATA interface.

This manual describes the specifications and functions of the drives and explains in detail how to incorporate the drives into user systems. This manual assumes that the reader has a basic knowledge of hard disk drives and their implementations in computer systems.

This manual consists of seven chapters and sections explaining the special terminology and abbreviations used in this manual:

Overview of Manual

CHAPTER 1 Drive Overview

This chapter gives an overview of the MHC Series and MHD Series and describes their features.

CHAPTER 2 Drive Configuration

This chapter describes the internal configurations of the MHC Series and MHD Series and the configuration of the systems in which they operate.

CHAPTER 3 Conditions Installation

This chapter describes the external dimensions, installation conditions, and switch settings of the MHC Series and MHD Series.

CHAPTER 4 Theory of Drive Operation

This chapter describes the operation theory of the MHC Series and MHD Series.

CHAPTER 5 Interface

This chapter describes the interface specifications of the MHC Series and MHD Series.

CHAPTER 6 Operations

This chapter describes the operations of the MHC Series and MHD Series.

Terminology

This section explains the special terminology used in this manual.

Abbreviation

This section gives the meanings of the definitions used in this manual.

Conventions for Alert Messages

This manual uses the following conventions to show the alert messages. An alert message consists of an alert signal and alert statements. The alert signal consists of an alert symbol and a signal word or just a signal word.

The following are the alert signals and their meanings:

This indicates a hazarous situation *could* result in *minor* or *moderate personal injury* if the user does not perform the procedure correctly. This alert signal also indicates that damages to the product or other property, *may* occur if the user does not perform the procedure correctly.

IMPORTANT

This indicates information that could help the user use the product more efficiently.

In the text, the alert signal is centered, followed below by the indented message. A wider line space precedes and follows the alert message to show where the alert message begins and ends. The following is an example:

(Example)

Data corruption: Avoid mounting the disk drive near strong magnetic sources such as loud speakers. Ensure that the disk drive is not affected by external magnetic fields.

The main alert messages in the text are also listed in the “Important Alert Items.”

Operating Environment

This product is designed to be used in offices or computer rooms.

For details regarding the operating environment of use, refer to the _____ _____ (Cnnn-Xnnn) and the _____ _____ (Cnnn-Xnnn).

Attention

Please forward any comments you may have regarding this manual.

To make this manual easier for users to understand, opinions from readers are needed. Please write your opinions or requests on the Comment at the back of this manual and forward it to the address described in the sheet.

Liability Exception

"Disk drive defects" refers to defects that involve adjustment, repair, or replacement.

Fujitsu is not liable for any other disk drive defects, such as those caused by user misoperation or mishandling, inappropriate operating environments, defects in the power supply or cable, problems of the host system, or other causes outside the disk drive.

Important Alert Items

Important Alert Messages

The important alert messages in this manual are as follows:

A hazardous situation *could* result in *minor* or *moderate personal injury* if the user does not perform the procedure correctly. Also, damage to the predate or other property, *may* occur if the user does not perform the procedure correctly.

Task	Alert message	Page
Normal Operation	**Data corruption:** Avoid mounting the disk near strong magnetic soures such as loud speakers. Ensure that the disk drive is not affected by extrnal magnetic fields.	3-6

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CHAPTER 1 Device Overview

Overview and features are described in this chapter, and specifications and power requirement are described.

The MHC Series and MHD Series are 2.5-inch hard disk drives with built-in disk controllers. These disk drives use the AT-bus hard disk interface protocol and are compact and reliable.

1.1 Features

1.1.1 Functions and performance

The fillowing features of the MHC Series and MHD Series are described.

(1) Compact

The MHC2032AT and MHC2040AT have 2 or 3 disks of 65 mm (2.5 inches) diameter, and its height is 12.5 mm (0.492 inch). The MHD2032AT and MHD2021AT have 2 disks of 65 mm (2.5 inches) diameter, and its height is 9.5 mm (0.374 inch).

(2) Large capacity

The disk drive can record up to 1,083 MB (formatted) on one disk using the (16/17) EPR4ML recording method and 12 recording zone technology. The MHC Series and MHD Series have a formatted capacity of 3.25 GB (MHC2032AT, MHD2032AT), 4.09 GB (MHC2040AT) and 2.16 GB (MHD2021AT) respectively.

(3) High-speed Transfer rate

The disk drives (the MHC Series and MHD Series) have an internal data rate up to 10.6 MB/s (MHC/D2032AT). The disk drive supports an external data rate up to 33.3 MB/s (U-DMA mode 2).

(4) Average positioning time

Use of a rotary voice coil motor in the head positioning mechanism greatly increases the positioning speed. The average positioning time is 13 ms (at read).

1.1.2 Adaptability

(1) Power save mode

The power save mode feature for idle operation, stand by and sleep modes makes The disk drives (the MHC Series and MHD Series) ideal for applications where power consumption is a factor.

(2) Wide temperature range

The disk drives (the MHC Series and MHD Series) can be used over a wide temperature range (5°C to 55°C).

(3) Low noise and vibration

In Ready status, the noise of the disk drives (the MHC Series and MHD Series) is only about 30 dBA (measured at 1 m apart from the drive under the idle mode).

1.1.3 Interface

(1) Connection to interface

With the built-in ATA interface controller, the disk drives (the MHC Series and MHD Series) can be connected to an ATA interface of a personal computer.

(2) 512-KB data buffer

The disk drives (the MHC Series and MHD Series) uses a 512-KB data buffer to transfer data between the host and the disk media.

In combination with the read-ahead cache system described in item (3) and the write cache described in item (7), the buffer contributes to efficient I/O processing.

(3) Read-ahead cache system

After the execution of a disk read command, the disk drive automatically reads the subsequent data block and writes it to the data buffer (read ahead operation). This cache system enables fast data access. The next disk read command would normally cause another disk access. But, if the read ahead data corresponds to the data requested by the next read command, the data in the buffer can be transferred instead.

(4) Master/slave

The disk drives (the MHC Series and MHD Series) can be connected to ATA interface as daisy chain configuration. Drive 0 is a master device, drive 1 is a slave device.

(5) Error correction and retry by ECC

If a recoverable error occurs, the disk drives (the MHC Series and MHD Series) themselves attempt error recovery. The ECC has improved buffer error correction for correctable data errors.

(6) Self-diagnosis

The disk drives (the MHC Series and MHD Series) have a diagnostic function to check operation of the controller and disk drives. Executing the diagnostic command invokes self-diagnosis.

(7) Write cache

When the disk drives (the MHC Series and MHD Series) receive a write command, the disk drives post the command completion at completion of transferring data to the data buffer completion of writing to the disk media. This feature reduces the access time at writing.

1.2 Device Specifications

1.2.1 Specifications summary

Table 1.1 shows the specfications of the disk drives (MHC2032AT/MHC2040AT).

Table 1.1 Specifications (MHC2032AT/MHC2040AT)

	MHC2032AT	MHC2040AT
Format Capacity (*1)	3.25 GB	4.09 GB
Number of Heads	4	6
Number of Cylinders (User)	7,322	7,230
Bytes per Sector	512	
Recording Method	(16/17) EPR4ML	
Track Density	11,960 TPI	
Bit Density	178,000 BPI	
Rotational Speed	4,000 rpm ± 1%	
Average Latency	7.5 ms	
Positioning time (read and seek) • Minimum (Track to Track) • Average • Maximum (Full)	 2.5 ms (typ.) Read: 13 ms (typ.) 23 ms (typ.)	
Start/Stop time • Start (0 rpm to Drive Read) • Stop (at Power Down)	 Typ.: 5 sec, Max.: 10 sec Typ.: 5 sec, Max.: 15 sec (when the command is stopped) (when the power is off)	
Interface	ATA-3 (Max. Cable length: 0.46 m)	
Data Transfer Rate • To/From Media	6.3 to 10.6 MB/s	5.5 to 9.8 MB/s
• To/From Host	33.3 MB/s Max. (U-DMA mode 2)	
Data Buffer Size	512 KB	
Physical Dimensions (Height × Width × Depth)	12.5 mm × 100.0 mm × 70.0 mm (0.49" × 3.94" × 2.75")	
Weight	145 g	

Table 1.2 shows the specfications of the disk drives (MHD2021AT/MHD2032AT).

Table 1.2 Specifications (MHD2021AT/MHD2032AT)

	MHD2021AT	MHD2032AT
Format Capacity (*1)	2.16 GB	3.25 GB
Number of Heads	3	4
Number of Cylinders (User)	7,290	7,322
Bytes per Sector	512	
Recording Method	(16/17) EPR4ML	
Track Density	11,960 TPI	
Bit Density	191 Kbpi	217 Kbpi
Rotational Speed	4,000 rpm ± 1%	
Average Latency	7.5 ms	
Positioning time (read and seek) • Minimum (Track to Track) • Average • Maximum (Full)	 2.5 ms (typ.) Read: 13 ms (typ.) 23 ms (typ.)	
Start/Stop time • Start (0 rpm to Drive Read) • Stop (at Power Down)	 Typ.: 5 sec, Max.: 10 sec Typ.: 5 sec, Max.: 15 sec (when the command is stopped) (when the power is off)	
Interface	ATA-3 (Max. Cable length: 0.46 m)	
Data Transfer Rate • To/From Media	5.9 to 10.0 MB/s	6.3 to 10.6 MB/s
• To/From Host	33.3 MB/s Max. (U-DMA mode 2)	
Data Buffer Size	512 KB	
Physical Dimensions (Height × Width × Depth)	9.5 mm × 100.0 mm × 70.0 mm (0.37" × 3.94" × 2.75")	
Weight	95 g	

*1: Capacity under the LBA mode.

Under the CHS mode (normal BIOS specification), formatted capacity, number of cylinders, number of heads, and number of sectors are as follows.

Model	Formatted Capacity	No. of Cylinder	No. of Heads	No. of Sectors
MHC2032AT	3,253.46 MB	6,304	16	63
MHC2040AT	4,099.86 MB	7,944	16	63
MHD2021AT	2,167.60 MB	4,200	16	63
MHD2032AT	3,253.46 MB	6,304	16	63

1.2.2 Model and product number

Table 1.3 lists the model names and product numbers of the MHC Series and MHD Series.

Table 1.3 Model names and product numbers

Model Name	Capacity (user area)	Mounting screw	Order No.
MHC2032AT	3.25 GB	M3, depth 3	CA01677-B040
MHC2040AT	4.09 GB	M3, depth 3	CA01677-B060
MHD2021AT	2.16 GB	M3, depth 3	CA01678-B030
MHD2032AT	3.25 GB	M3, depth 3	CA01678-B040

1.3 Power Requirements

(1) Input Voltage

- + 5 V ± 5 %

(2) Ripple

	+5 V
Maximum	100 mV (peak to peak)
Frequency	DC to 1 MHz

(3) Current Requirements and Power Dissipation

Table 1.4 lists the current and power dissipation.

Table 1.4 Current and power dissipation

	Typical RMS Current		Typical Power (*3)	
	MHC Series	MHD Series	MHC Series	MHD Series
Spin up (*1)	0.9 A	0.9 A	4.5 W	4.5 W
Idle	190 mA	190 mA	0.95 W	0.95 W
R/W (*2)	420 mA	430 mA	2.1 W	2.15 W
Standby	70 mA	70 mA	0.35 W	0.35 W
Sleep	26 mA	26 mA	0.13 W	0.13 W
Energy Consumption Efficiency	—	—	0.0002 W/MB	0.0003 W/MB

*1 Current at starting spindle motor.

*2 Power requirements reflect nominal values for +5V power.

*3 At 30% disk accessing.

(4) Current fluctuation (Typ.) at +5V when power is turned on

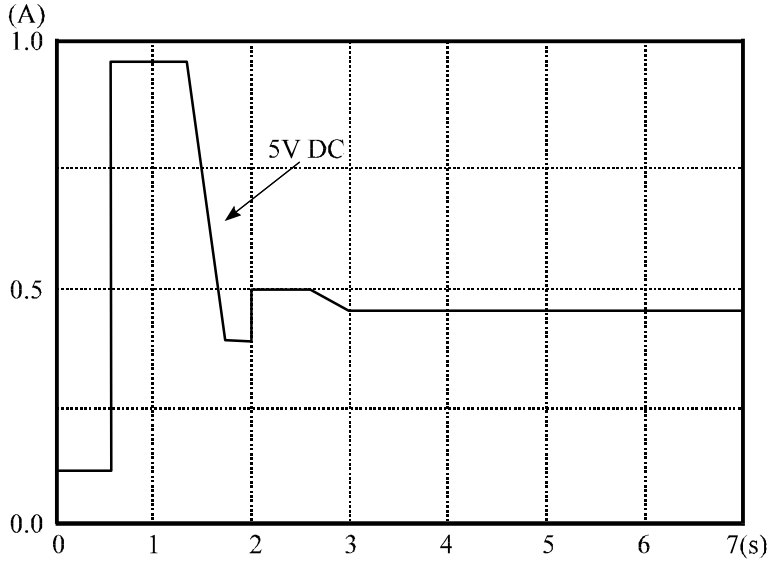


Figure 1.1 Current fluctuation (Typ.) at +5V when power is turned on

(5) Power on/off sequence

The voltage detector circuits (the MHC Series and MHD Series) monitor +5 V. The circuits do not allow a write signal if either voltage is abnormal. These prevent data from being destroyed and eliminates the need to be concerned with the power on/off sequence.

1.4 Environmental Specifications

Table 1.5 lists the environmental specifications.

Table 1.5 Environmental specifications

Temperature	
• Operating	5°C to 55°C (ambient)
	5°C to 60°C (disk enclosure surface)
• Non-operating	–40°C to 65°C
• Thermal Gradient	20°C/h or less
Humidity	
• Operating	8% to 90% RH (Non-condensing)
• Non-operating	5% to 95% RH (Non-condensing)
• Maximum Wet Bulb	29°C
Altitude (relative to sea level)	
• Operating	–300 to 3,000 m
• Non-operating	–300 to 12,000 m

1.5 Acoustic Noise

Table 1.6 lists the acoustic noise specification.

Table 1.6 Acoustic noise specification

Sound Pressure	
• Idle mode (DRIVE READY)	30 dBA typical at 1 m

1.6 Shock and Vibration

Table 1.7 lists the shock and vibration specification.

Table 1.7 Shock and vibration specification

Vibration (swept sine, one octave per minute)	
• Operating	5 to 500 Hz, 1.0G0-peak (MHC series) 5 to 400 Hz, 1.0G0-peak (MHD series) (without non-recovered errors) (9.8 m/s^2 0-peak)
• Non-operating	5 to 500 Hz, 5G0-peak (MHC series) 5 to 400 Hz, 5G0-peak (MHD series) (no damage) (49 m/s^2 0-peak)
Shock (half-sine pulse, 2 ms duration)	
• Operating	100G0-peak (without non-recovered errors) (980 m/s^2 0-peak)
• Non-operating	500G0-peak (no damage) (4,900 m/s^2 0-peak)

1.7 Reliability

(1) Mean time between failures (MTBF)

Conditions of 300,000 h	Current time	250H/month or less 3000H/years or less
	Operating time	20% or less of current time
	CSS operations	50/day or less Total 50,000 or less
	Power on/off	1/day or more needed.
	Environment	5 to 55°C/8 to 90% But humidity bulb temperature 29°C or less

MTBF is defined as follows:

$$\text{MTBF} = \frac{\text{Total operation time in all fields}}{\text{number of device failure in all fields}} \text{ (H)}$$

"Disk drive defects" refers to defects that involve repair, readjustment, or replacement. Disk drive defects do not include failures caused by external factors, such as damage caused by handling, inappropriate operating environments, defects in the power supply host system, or interface cable.

(2) Mean time to repair (MTTR)

The mean time to repair (MTTR) is 30 minutes or less, if repaired by a specialist maintenance staff member.

(3) Service life

In situations where management and handling are correct, the disk drive requires no overhaul for five years when the DE surface temperature is less than 48°C. When the DE surface temperature exceeds 48°C, the disk drives requires no overhaul for five years or 20,000 hours of operation, whichever occurs first. Refer to item (3) in Subsection 3.2 for the measurement point of the DE surface temperature. Also the operating conditions except the environment temperature are based on the MTBF conditions.

(4) Data assurance in the event of power failure

Except for the data block being written to, the data on the disk media is assured in the event of any power supply abnormalities. This does not include power supply abnormalities during disk media initialization (formatting) or processing of defects (alternative block assignment).

1.8 Error Rate

Known defects, for which alternative blocks can be assigned, are not included in the error rate count below. It is assumed that the data blocks to be accessed are evenly distributed on the disk media.

(1) Unrecoverable read error

Read errors that cannot be recovered by maximum 252 times read retries without user's retry and ECC corrections shall occur no more than 10 times when reading data of 10^{14} bits. Read retries are executed according to the disk drive's error recovery procedure, and include read retries accompanying head offset operations.

(2) Positioning error

Positioning (seek) errors that can be recovered by one retry shall occur no more than 10 times in 10^{7} seek operations.

1.9 Media Defects

Defective sectors are replaced with alternates when the disk (the MHC Series and MHD Series) are formatted prior to shipment from the factory (low level format). Thus, the hosts see a defect-free devices.

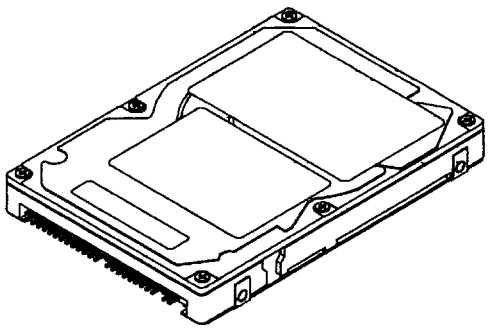
Alternate sectors are automatically accessed by the disk drive. The user need not be concerned with access to alternate sectors.

CHAPTER 2 Device Configuration

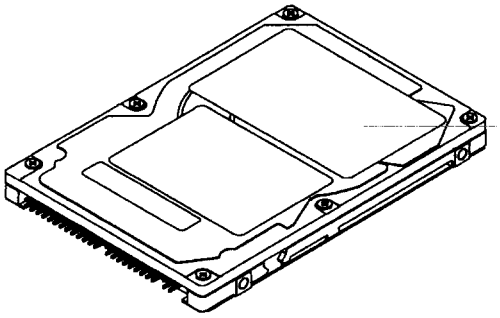
This chapter describes the internal configurations of the hard disk drives and the configuration of the systems in which they operate.

2.1 Device Configuration

Figure 2.1 shows the disk drive. The disk drive consists of a disk enclosure (DE), read/write preamplifier, and controller PCA. The disk enclosure contains the disk media, heads, spindle motors, actuators, and a circulating air filter.



MHC20xxAT



MHD20xxAT

Figure 2.1 Disk drive outerview (the MHC Series and MHD Series)

(1) Disk

The outer diameter of the disk is 65 mm. The inner diameter is 20 mm. The number of disks used varies with the model, as described below. The disks are rated at over 50,000 start/stop operations.

MHC2032AT: 2 disks (4 Heads) MHD2032AT: 2 disks (4 Heads)

MHC2040AT: 3 disks (6 Heads) MHD2021AT: 2 disks (3 Heads)

(2) Head

The heads are of the contact start/stop (CSS) type. The head touches the disk surface while the disk is not rotating and automatically lifts when the disk starts.

Figure 2.2 illustrates the configuration of the disks and heads of each model. In the disk surface, servo information necessary for controlling positioning and read/write and user data are written. Numerals 0 to 5 indicate read/write heads.

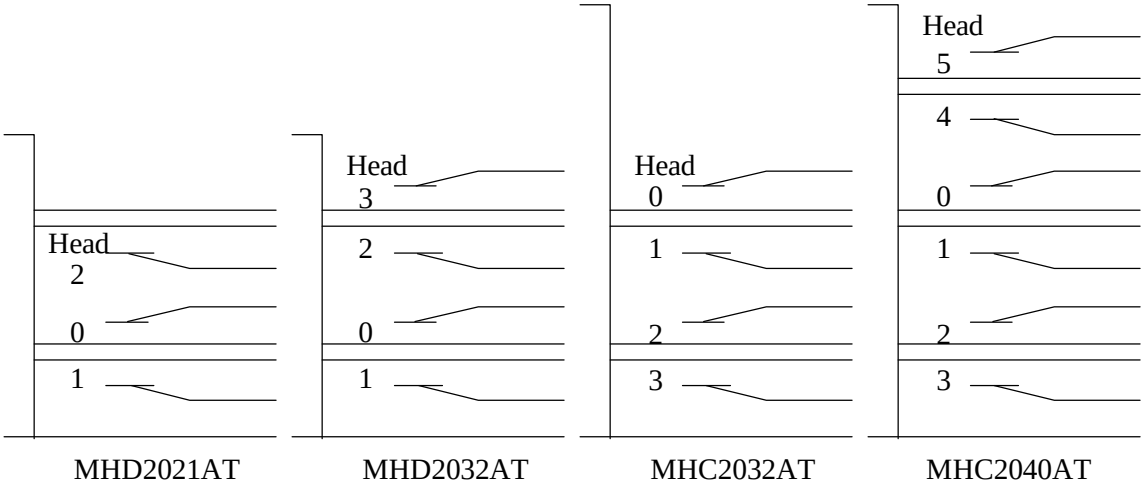


Figure 2.2 Configuration of disk media heads

(3) Spindle motor

The disks are rotated by a direct drive Hall-less DC motor.

(4) Actuator

The actuator uses a revolving voice coil motor (VCM) structure which consumes low power and generates very little heat. The head assembly at the edge of the actuator arm is controlled and positioned by feedback of the servo information read by the read/write head. If the power is not on or if the spindle motor is stopped, the head assembly stays in the specific CSS zone on the disk and is fixed by a mechanical lock.

(5) Air circulation system

The disk enclosure (DE) is sealed to prevent dust and dirt from entering. The disk enclosure features a closed loop air circulation system that relies on the blower effect of the rotating disk. This system continuously circulates the air through the circulation filter to maintain the cleanliness of the air within the disk enclosure.

(6) Read/write circuit

The read/write circuit uses a LSI chip for the read/write preamplifier. It improves data reliability by preventing errors caused by external noise.

(7) Controller circuit

The controller circuit consists of an LSI chip to improve reliability. The high-speed microprocessor unit (MPU) achieves a high-performance AT controller.

2.2 System Configuration

2.2.1 ATA interface

Figures 2.3 and 2.4 show the ATA interface system configuration. The drive has a 44-pin PC AT interface connector and supports the PIO transfer at 16.6 MB/s (ATA-3, Mode 4), the DMA transfer at 16.6 MB/s (ATA-3, Multiword mode 2) and also the U-DMA at 33.3 MB/s (ATA-3, Mode 2).

2.2.2 1 drive connection

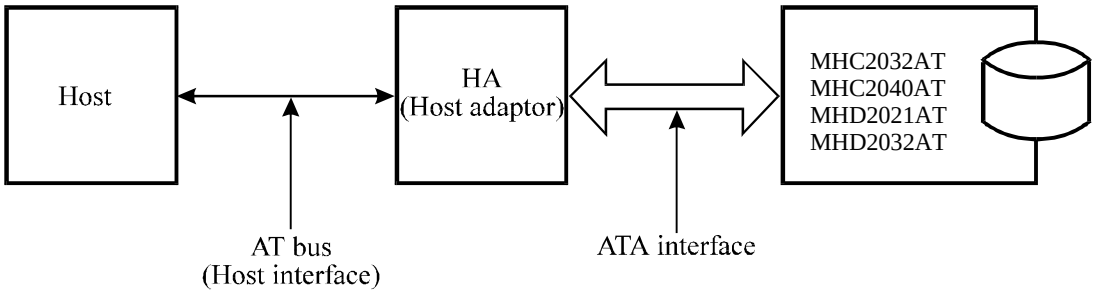
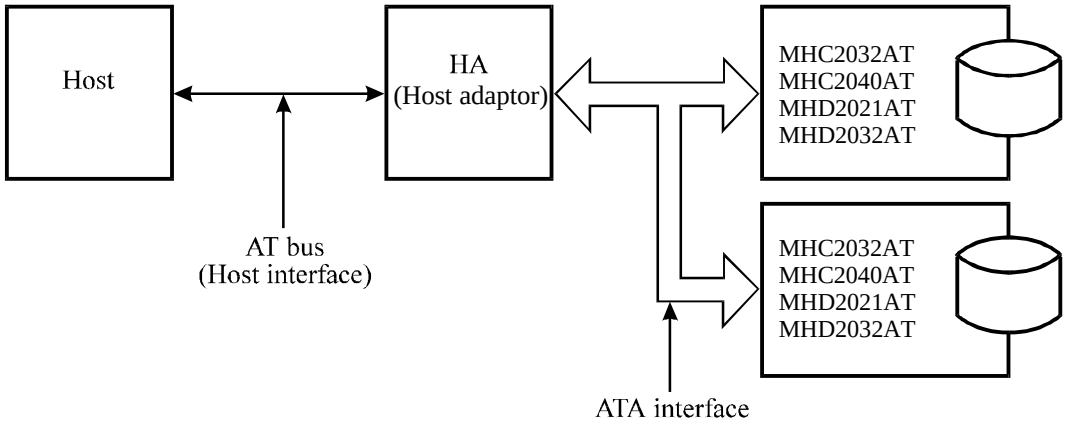


Figure 2.3 1 drive system configuration

2.2.3 2 drives connection



Note:

When the drive that is not conformed to ATA is connected to the disk drive above configuration, the operation is not guaranteed.

Figure 2.4 2 drives configuration

IMPORTANT

HA (host adaptor) consists of address decoder, driver, and receiver. ATA is an abbreviation of “AT attachment”. The disk drive is conformed to the ATA-3 interface.

At high speed data transfer (PIO mode 3, mode 4, or DMA mode 2 U-DMA mode 2), occurence of ringing or crosstalk of the signal lines (AT bus) between the HA and the disk drive may be a great cause of the obstruction of system reliability. Thus, it is necessary that the capacitance of the signal lines including the HA and cable does not exceed the ATA-3 standard, and the cable length between the HA and the disk drive should be as short as possible.

No need to push the top cover of the disk drive. If the over-power worked, the cover could be contacted with the spindle motor. Thus, that could be made it the cause of failure.

CHAPTER 3 Installation Conditions

This chapter gives the external dimensions, installation conditions, surface temperature conditions, cable connections, and switch settings of the hard disk drives.

3.1 Dimensions

Figure 3.1 illustrates the dimensions of the disk drive and positions of the mounting screw holes. All dimensions are in mm.

MHD2032AT

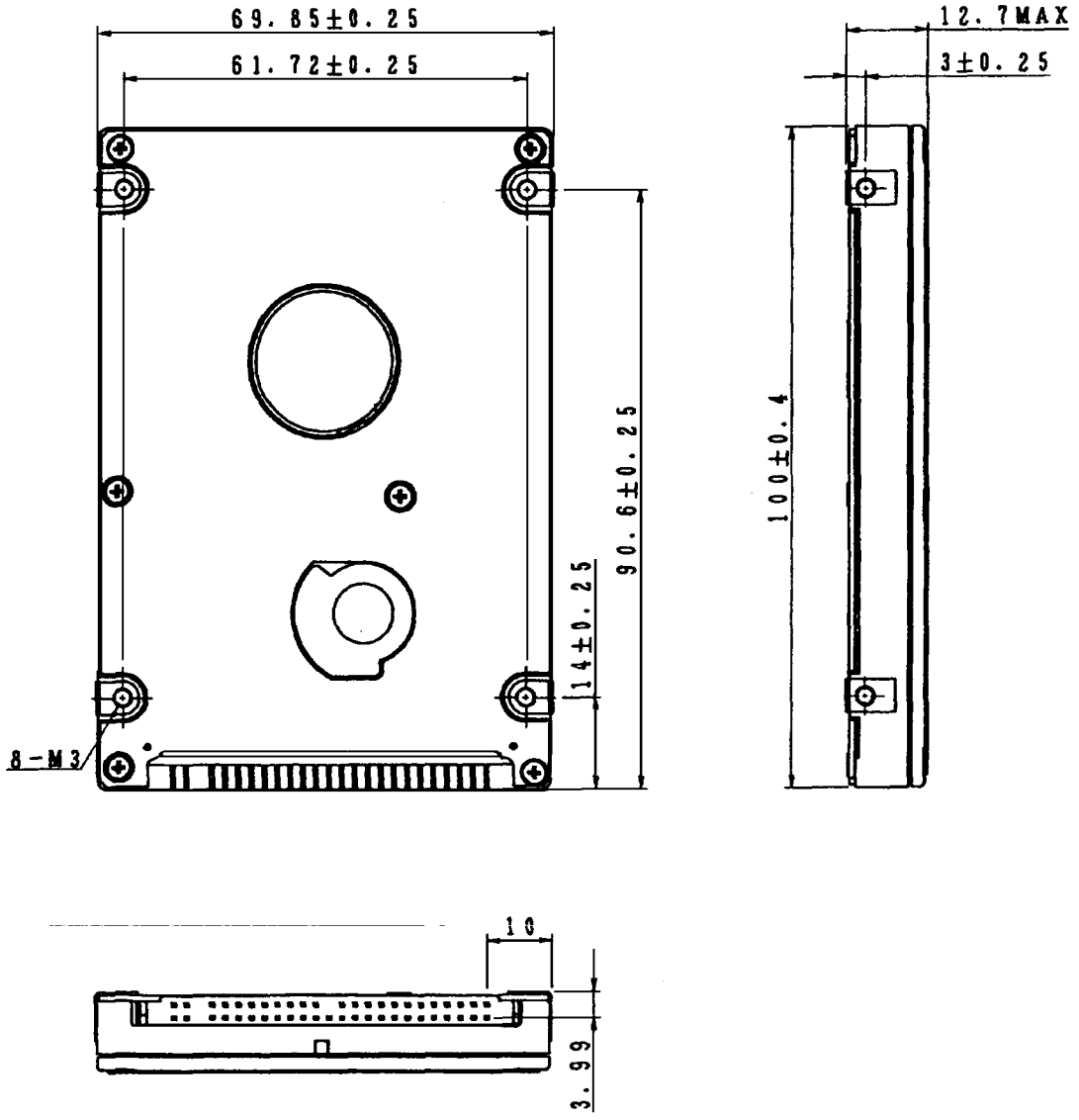


Figure 3.1 Dimensions (MHC series) (1/2)

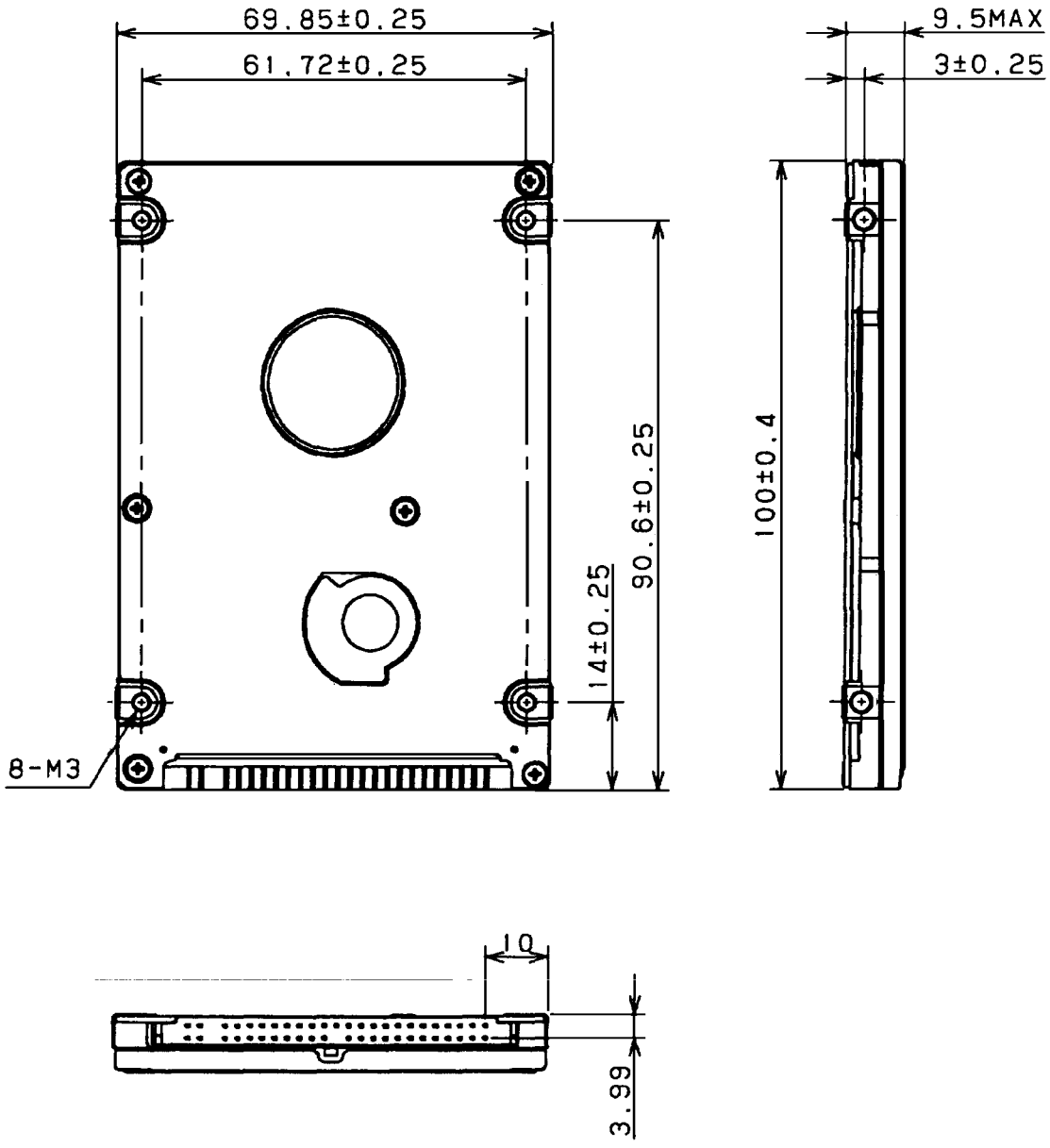
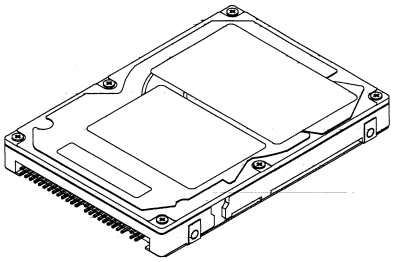


Figure 3.1 Dimensions (MHD series) (2/2)

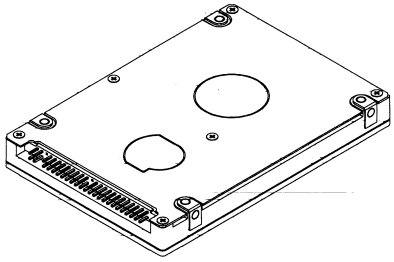
3.2 Mounting

(1) Orientation

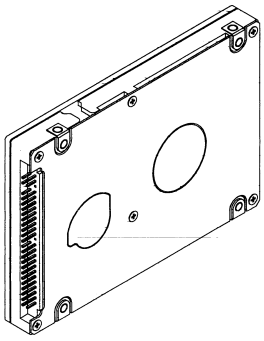
Figure 3.2 illustrates the allowable orientations for the disk drive.



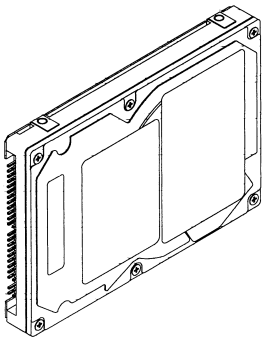
(a) Horizontal –1



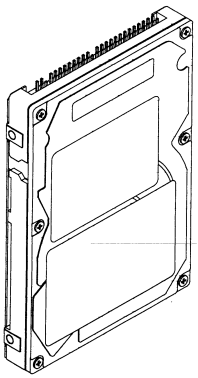
(b) Horizontal –1



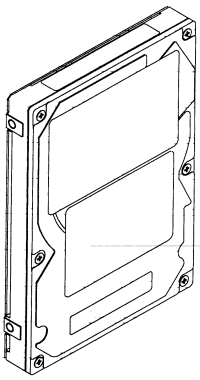
(c) Vertical –1



(d) Vertical –2



(e) Vertical –3



(f) Vertical –4

Figure 3.2 Orientation (Sample: MHC2040AT)

(2) Frame

The MR head bias of the HDD disk enclosure (DE) is zero. The mounting frame is connected to SG.

IMPORTANT

Use M3 screw for the mounting screw and the screw length should satisfy the specification in Figure 3.3.

The tightening torque must not exceed 3 kgcm.

When attaching the HDD to the system frame, do not allow the system frame to touch parts (cover and base) other than parts to which the HDD is attached.

(3) Limitation of side-mounting

Do not use the center hole. For screw length, see Figure 3.3.

Note) These dimensions are recommended values; if it is not possible to satisfy them, contact us.

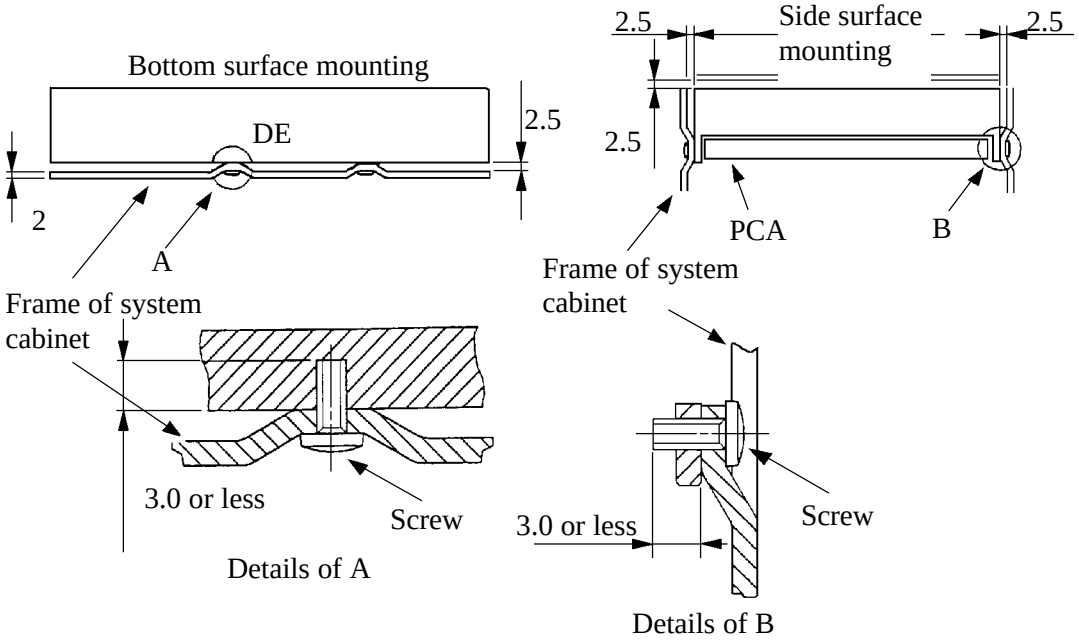


Figure 3.3 Mounting frame structure

(4) Ambient temperature

The temperature conditions for a disk drive mounted in a cabinet refer to the ambient temperature at a point 3 cm from the disk drive. The ambient temperature must satisfy the temperature conditions described in Section 1.4, and the airflow must be considered to prevent the DE surface temperature from exceeding 60°C.

Provide air circulation in the cabinet such that the PCA side, in particular, receives sufficient cooling. To check the cooling efficiency, measure the surface temperatures of the DE. Regardless of the ambient temperature, this surface temperature must meet the standards listed in Table 3.1. Figure 3.4 shows the temperature measurement point.

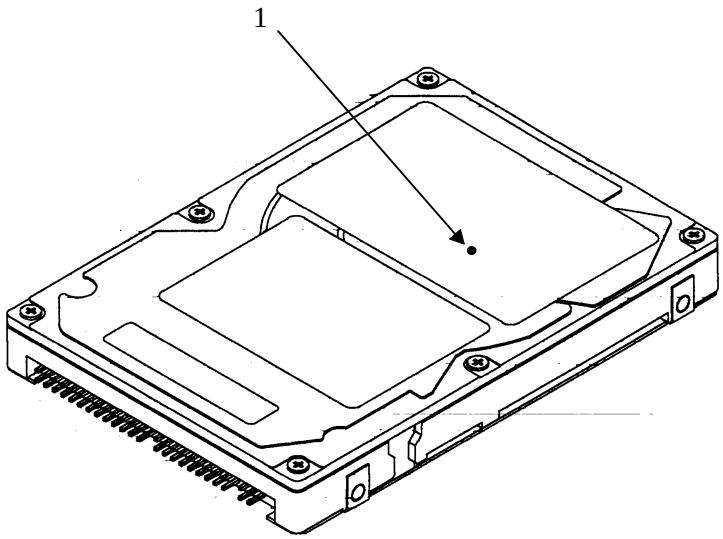


Figure 3.4 Surface temperature measurement points (Sample: MHC2040AT)

Table 3.1 Surface temperature measurement points and standard values

No.	Measurement point	Temperature
1	DE cover	60°C max

(5) Service area

Figure 3.5 shows how the drive must be accessed (service areas) during and after installation.

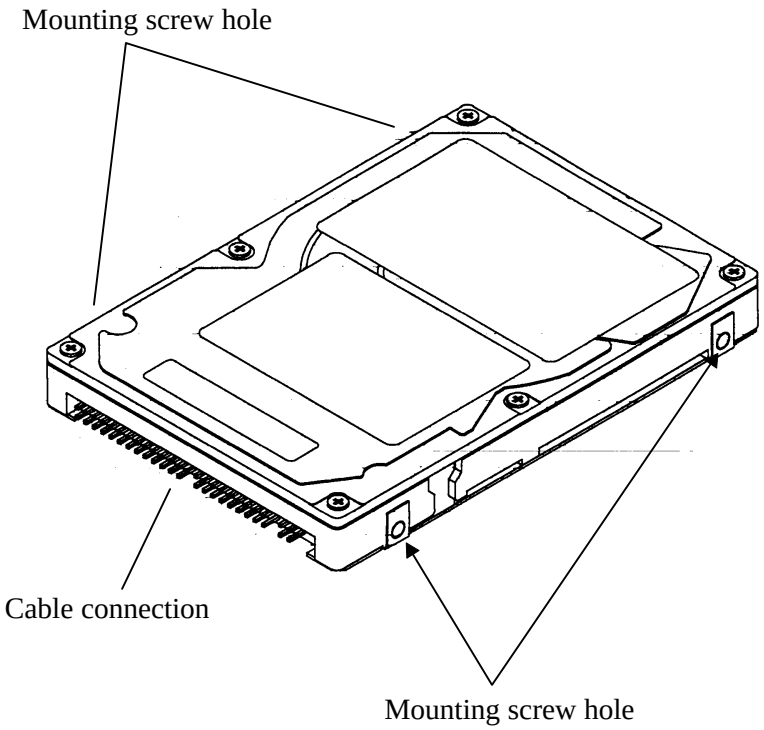


Figure 3.5 Service area (Sample: MHC2040AT)

(6) External magnetic fields

CAUTION

Data corruption: Avoid mounting the disk drive near strong magnetic sources such as loud speakers. Ensure that the disk drive is not affected by external magnetic fields.

3.3 Cable Connections

3.3.1 Device connector

The disk drive has the connectors and terminals listed below for connecting external devices. Figure 3.6 shows the locations of these connectors and terminals.

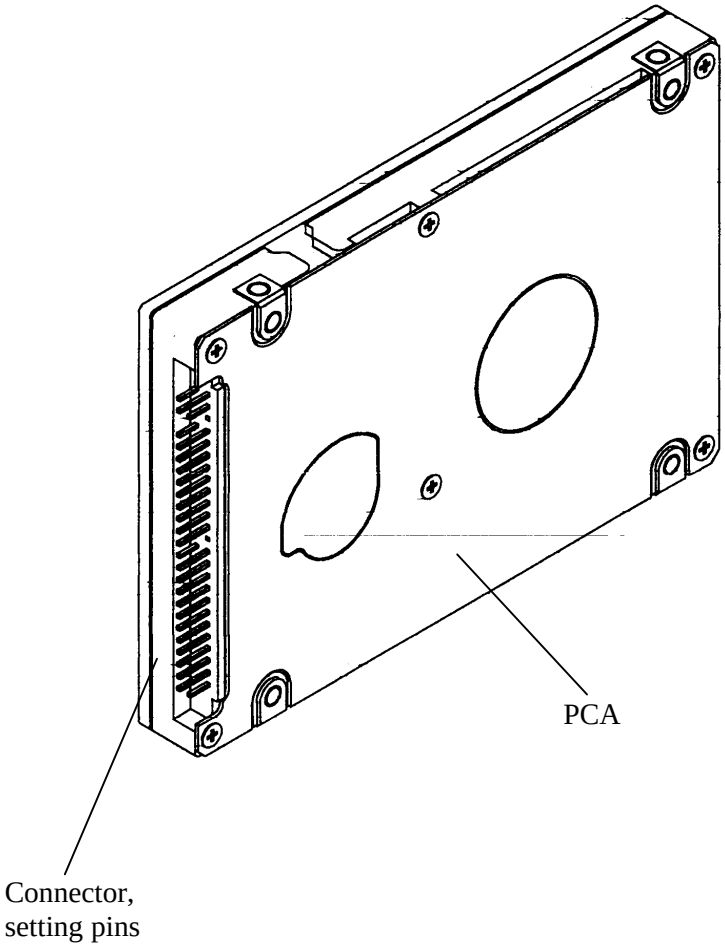


Figure 3.6 Connector locations (Sample: MHC2040AT)

3.3.2 Cable connector specifications

Table 3.2 lists the recommended specifications for the cable connectors.

Table 3.2 Cable connector specifications

	Name	Model	Manufacturer
ATA interface and power supply cable (44-pin type)	Cable socket (44-pin type)	89361-144	BERG
	Cable (44-pin type)	FV08-A440	Junkosha

IMPORTANT

For the host interface cable, use a ribbon cable. A twisted cable or a cable with wires that have become separated from the ribbon may cause crosstalk between signal lines. This is because the interface is designed for ribbon cables and not for cables carrying differential signals.

3.3.3 Device connection

Figure 3.7 shows how to connect the devices.

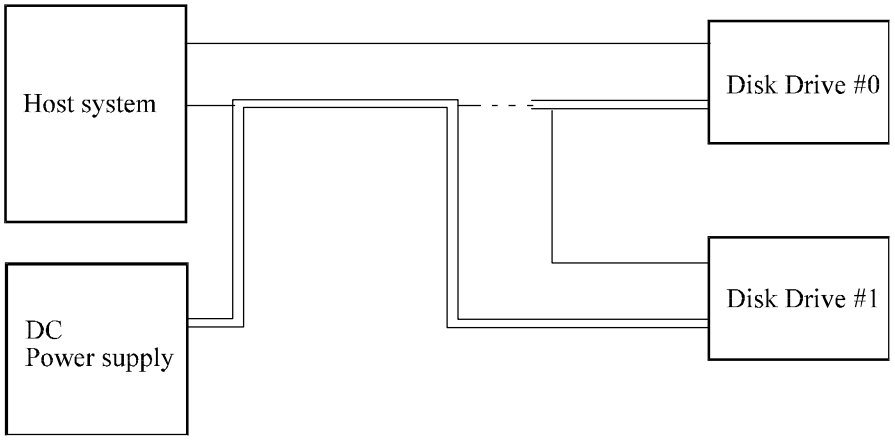


Figure 3.7 Cable connections

3.3.4 Power supply connector (CN1)

Figure 3.8 shows the pin assignment of the power supply connector (CN1).

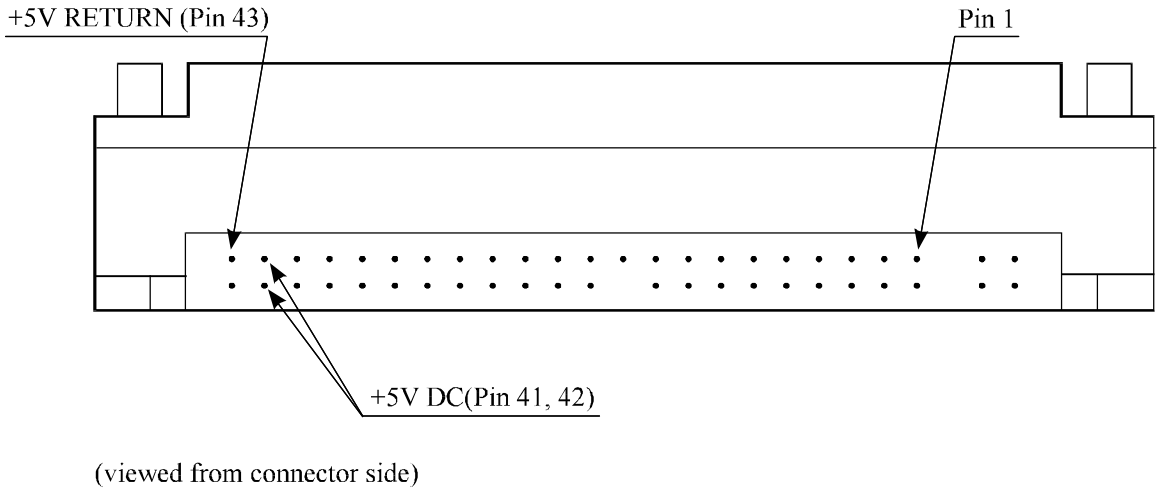


Figure 3.8 Power supply connector pins (CN1)

3.4 Jumper Settings

3.4.1 Location of setting jumpers

Figure 3.9 shows the location of the jumpers to select drive configuration and functions.

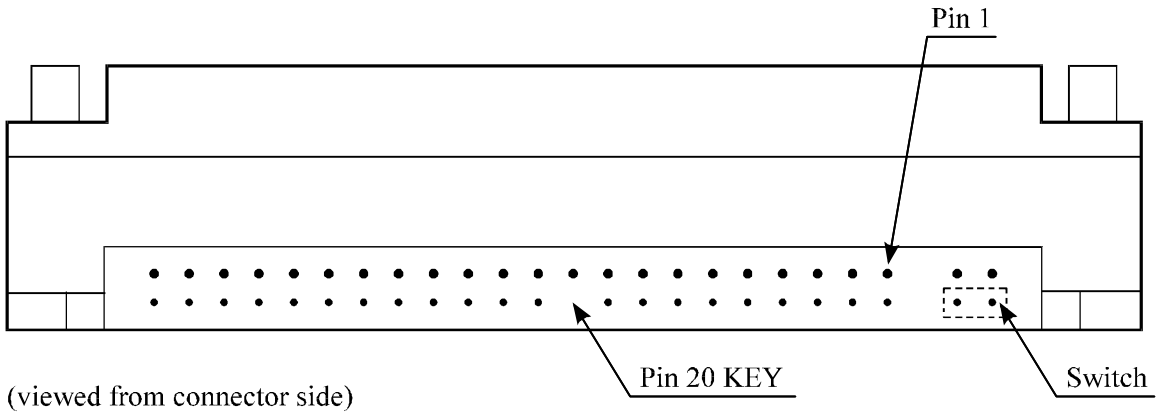


Figure 3.9 Jumper location

3.4.2 Factory default setting

Figure 3.10 shows the default setting position at the factory.

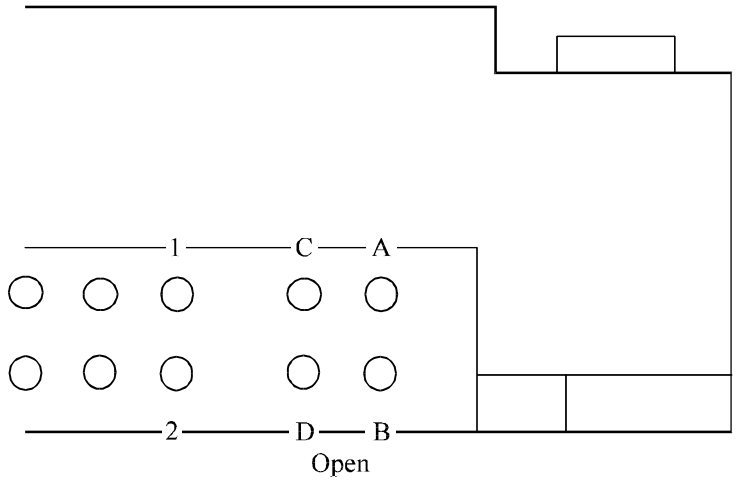


Figure 3.10 Factory default setting

3.4.3 Master drive-slave drive setting

Master device (device #0) or slave device (device #1) is selected.

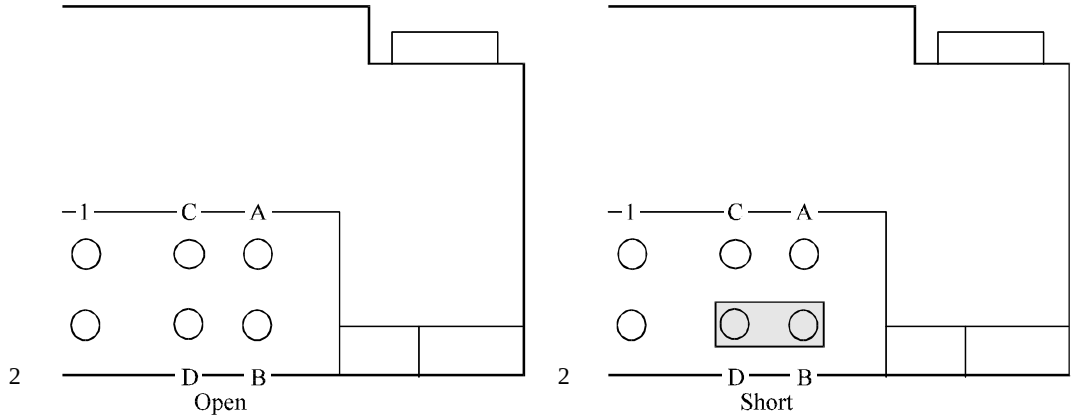


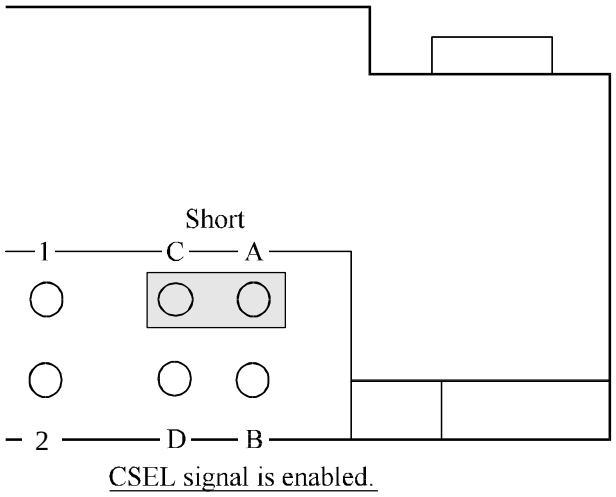
Figure 3.11 Jumper setting of master or slave device

Note:

Pins A and C should be open.

3.4.4 CSEL setting

Figure 3.12 shows the cable select (CSEL) setting.



Note:

The CSEL setting is not depended on setting between pins Band D.

Figure 3.12 CSEL setting

Figure 3.13 and 3.14 show examples of cable selection using unique interface cables.

By connecting the CSEL of the master device to the CSEL Line (conducer) of the cable and connecting it to ground further, the CSEL is set to low level. The device is identified as a master device. At this time, the CSEL of the slave device does not have a conductor. Thus, since the slave device is not connected to the CSEL conductor, the CSEL is set to high level. The device is identified as a slave device.

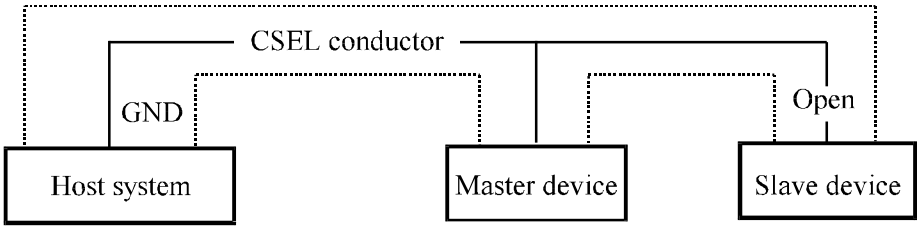


Figure 3.13 Example (1) of Cable Select

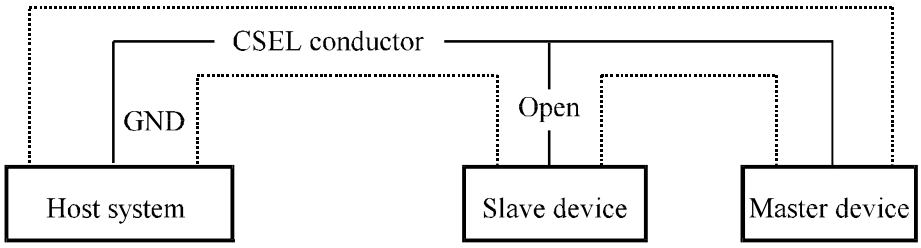


Figure 3.14 Example (2) of Cable Select

CHAPTER 4 Theory of Device Operation

This chapter explains basic design concepts of the disk drive. Also, this chapter explains subassemblies of the disk drive, each sequence, servo control, and electrical circuit blocks.

4.1 Outline

This chapter consists of two parts. First part (Section 4.2) explains mechanical assemblies of the disk drive. Second part (Sections 4.3 through 4.7) explains a servo information recorded in the disk drive and drive control method.

4.2 Subassemblies

The disk drive consists of a disk enclosure (DE) and printed circuit assembly (PCA).

The DE contains all movable parts in the disk drive, including the disk, spindle, actuator, read/write head, and air filter. For details, see Subsections 4.2.1 to 4.2.5.

The PCA contains the control circuits for the disk drive. The disk drive has one PCA. For details, see Sections 4.3.

4.2.1 Disk

The DE contains disks with an outer diameter of 65 mm and an inner diameter of 20 mm. The MHC2040AT has three disks and MHC2032AT, MHD2032AT and MHD2021AT have two disks.

The head contacts the disk each time the disk rotation stops; the life of the disk is 50,000 contacts or more. Servo data is recorded on top disk.

Servo data is recorded on each cylinder (total 60). Servo data written at factory is read out by the read/write head. For servo data, see Section 4.7.

4.2.2 Head

Figure 4.1 shows the read/write head structures. MHC2040AT has 6 read/write heads and MHC2032AT has 4 read/write heads. MHD2032AT has 4 read/write heads and MHD2021AT has 3 read/write heads. These heads are raised from the disk surface as the spindle motor the rated rotation speed.

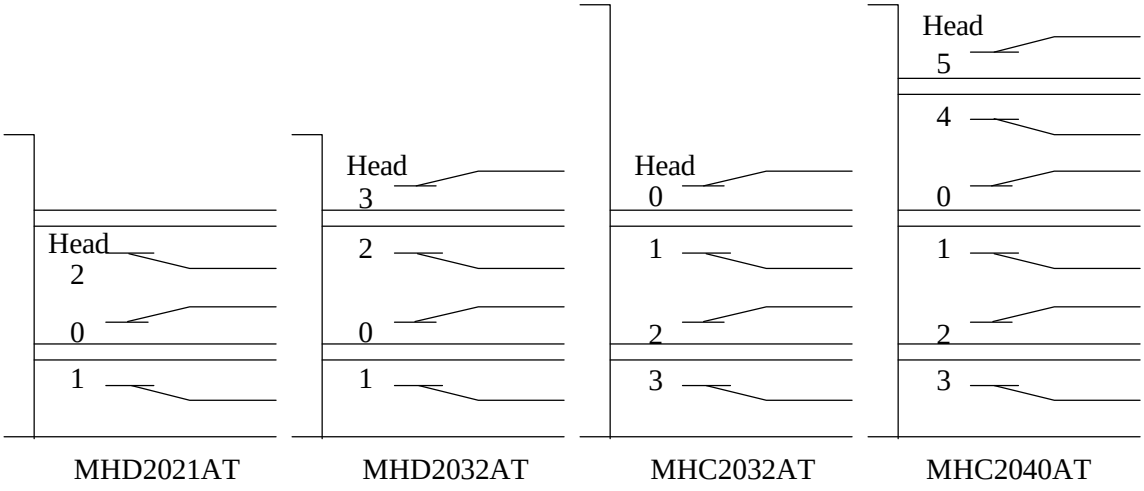


Figure 4.1 Head structure

4.2.3 Spindle

The spindle consists of a disk stack assembly and spindle motor. The disk stack assembly is activated by the direct drive sensor-less DC spindle motor, which has a speed of 4,000 rpm ±1%. The spindle is controlled with detecting a PHASE signal generated by counter electromotive voltage of the spindle motor at starting.

4.2.4 Actuator

The actuator consists of a voice coil motor (VCM) and a head carriage. The VCM moves the head carriage along the inner or outer edge of the disk. The head carriage position is controlled by feeding back the difference of the target position that is detected and reproduced from the servo information read by the read/write head.

4.2.5 Air filter

There are two types of air filters: a breather filter and a circulation filter.

The breather filter makes an air in and out of the DE to prevent unnecessary pressure around the spindle when the disk starts or stops rotating. When disk drives are transported under conditions where the air pressure changes a lot, filtered air is circulated in the DE.

The circulation filter cleans out dust and dirt from inside the DE. The disk drive cycles air continuously through the circulation filter through an enclosed loop air cycle system operated by a blower on the rotating disk.

4.3 Circuit Configuration

Figure 4.2 shows the disk drive circuit configuration.

(1) Read/write circuit

The read/write circuit consists of two LSIs; read/write preamplifier (PreAMP) and read channel (RDC).

The PreAMP consists of the write current switch circuit, that flows the write current to the head coil, and the voltage amplifier circuit, that amplitudes the read output from the head.

The RDC is the read demodulation circuit using the extended partial response class 4 (EPR4), and contains the Viterbi detector, programmable filter, adaptable transversal filter, times base generator, and data separator circuits. The RDC also contains the 16/17 group coded recording (GCR) encoder and decoder and servo demodulation circuit.

(2) Servo circuit

The position and speed of the voice coil motor are controlled by 2 closed-loop servo using the servo information recorded on the data surface. The servo information is an analog signal converted to digital for processeing by a MPU and then reconverted to an analog signal for control of the voice coil motor.

The MPU precisely sets each head on the track according on the servo information on the media surface.

(3) Spindle motor driver circuit

The circuit measures the interval of a PHASE signal generated by counter-electromotive voltage of a motor at the MPU and controls the motor speed comparing target speed.

(4) Controller circuit

Major functions are listed below.

- Data buffer (512 KB) management
- ATA interface control and data transfer control
- Sector format control
- Defect management
- ECC control
- Error recovery and self-diagnosis

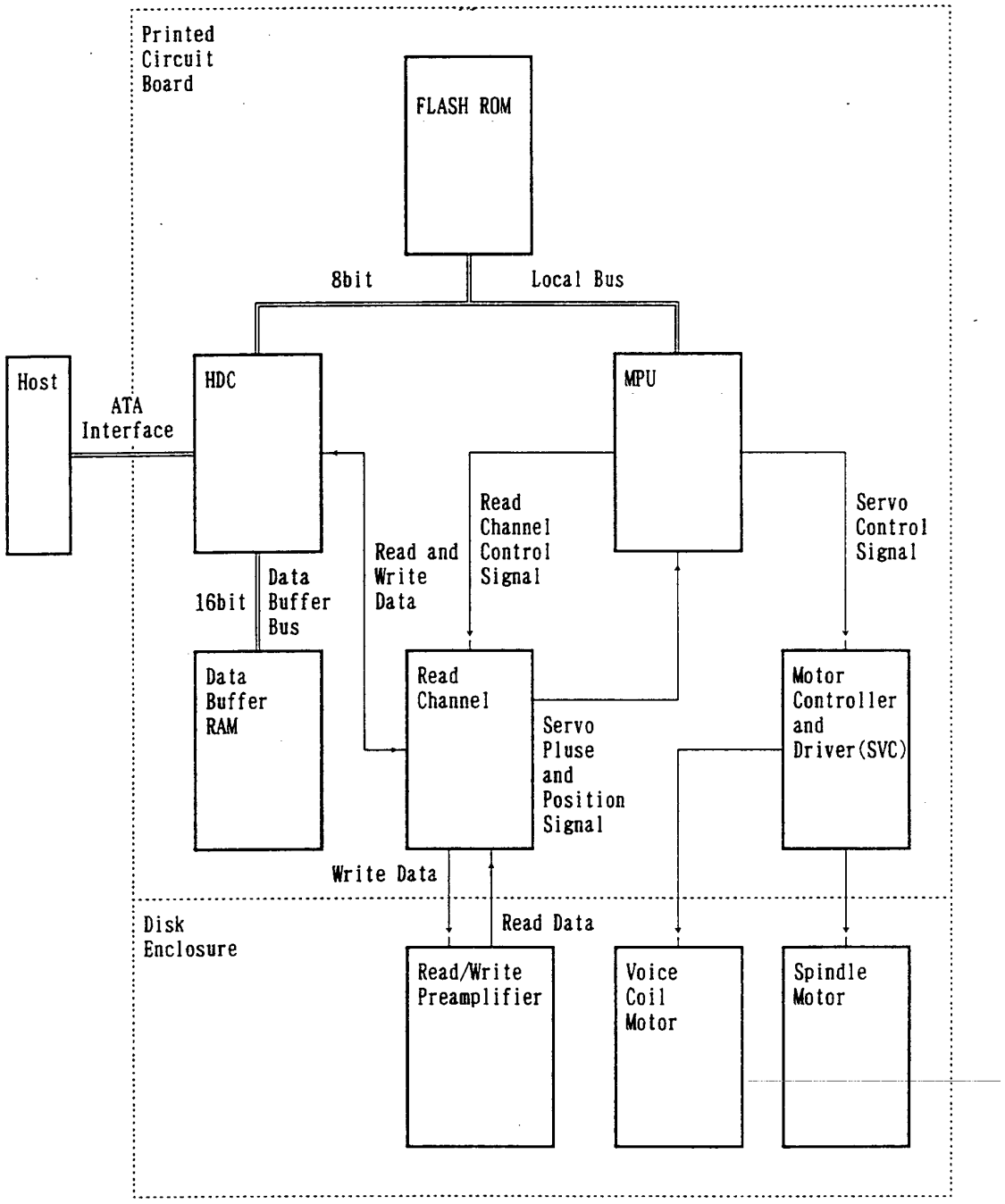


Figure 4.2 Circuit Configuration

4.4 Power-on Sequence

Figure 4.3 describes the operation sequence of the disk drive at power-on. The outline is described below.

a) After the power is turned on, the disk drive executes the MPU bus test, internal register read/write test, and work RAM read/write test. When the self-diagnosis terminates successfully, the disk drive starts the spindle motor.

b) The disk drive executes self-diagnosis (data buffer read/write test) after enabling response to the ATA bus.

c) After confirming that the spindle motor has reached rated speed, the disk drive releases the heads from the actuator magnet lock mechanism by applying current to the VCM. This unlocks the heads which are parked at the inner circumference of the disks.

d) The disk drive positions the heads onto the SA area and reads out the system information.

e) The disk drive executes self-seek-calibration. This collects data for VCM tarque and mechanical external forces applied to the actuator, and updates the calibrating value.

f) The drive becomes ready. The host can issue commands.

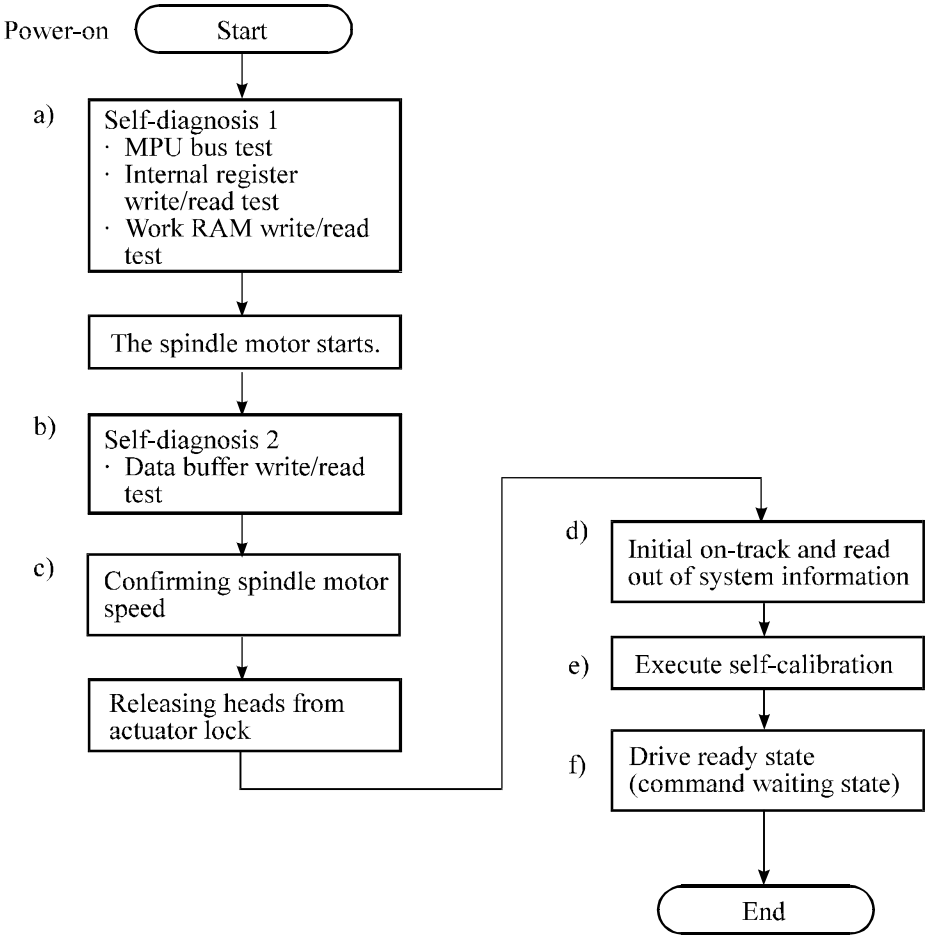


Figure 4.3 Power-on operation sequence

4.5 Self-calibration

The disk drive occasionally performs self-calibration in order to sense and calibrate mechanical external forces on the actuator, and VCM tarque. This enables precise seek and read/write operations.

4.5.1 Self-calibration contents

(1) Sensing and compensating for external forces

The actuator suffers from torque due to the FPC forces and winds accompanying disk revolution. The torque vary with the disk drive and the cylinder where the head is positioned. To execute stable fast seek operations, external forces are occasionally sensed.

The firmware of the drive measures and stores the force (value of the actuator motor drive current) that balances the torque for stopping head stably. This includes the current offset in the power amplifier circuit and DAC system.

The forces are compensated by adding the measured value to the specified current value to the power amplifier. This makes the stable servo control.

To compensate torque varing by the cylinder, the disk is divided into 8 areas from the innermost to the outermost circumference and the compensating value is measured at the measuring cylinder on each area at factory calibration. The measured values are stored in the SA cylinder. In the self-calibration, the compensating value is updated using the value in the SA cylinder.

(2) Compensating open loop gain

Torque constant value of the VCM has a dispersion for each drive, and varies depending on the cylinder that the head is positioned. To realize the high speed seek operation, the value that compensates torque constant value change and loop gain change of the whole servo system due to temperature change is measured and stored.

For sensing, the firmware mixes the disturbance signal to the position signal at the state that the head is positioned to any cylinder. The firmware calculates the loop gain from the position signal and stores the compensation value against to the target gain as ratio.

For compensating, the direction current value to the power amplifier is multiplied by the compensation value. By this compensation, loop gain becomes constant value and the stable servo control is realized.

To compensate torque constant value change depending on cylinder, whole cylinders from most inner to most outer cylinder are divided into 8 partitions at calibration in the factory, and the compensation data is measured for representive cylinder of each partition. This measured value is stored in the SA area. The compensation value at self-calibration is calculated using the value in the SA area.

4.5.2 Execution timing of self-calibration

Self-calibration is executed when:

- The power is turned on.
- The disk drive receives the RECALIBRATE command from the host.
- The self-calibration execution timechart of the disk drive specifies self-calibration.

The disk drive performs self-calibration according to the timechart based on the time elapsed from power-on. The timechart is shown in Table 4.1. After power-on, self-calibration is performed about every five or ten or fifteen minutes for the first 60 minutes or six RECALIBRATE command executions, and about every 30 minutes after that.

Table 4.1 Self-calibration execution timechart

	Time elapsed	Time elapsed (accumulated)
1	At power-on	Initial calibration
2	About 5 minutes	About 5 minutes
3	About 5 minutes	About 10 minutes
4	About 10 minutes	About 20 minutes
5	About 10 minutes	About 30 minutes
6	About 15 minutes	About 45 minutes
7	About 15 minutes	About 60 minutes
8	Every about 30 minutes	

4.5.3 Command processing during self-calibration

If the disk drive receives a command execution request from the host while executing self-calibration according to the timechart, the disk drive terminates self-calibration and starts executing the command precedingly. In other words, if a disk read or write service is necessary, the disk drive positions the head to the track requested by the host, reads or writes data, and restarts calibration.

This enables the host to execute the command without waiting for a long time, even when the disk drive is performing self-calibration. The command execution wait time is about maximum 100 ms.

4.6 Read/write Circuit

The read/write circuit consists of the read/write preamplifier (PreAMP), the write circuit, the read circuit, and the time base generator in the read channel (RDC). Figure 4.4 is a block diagram of the read/write circuit.

4.6.1 Read/write preamplifier (PreAMP)

One PreAMP is mounted on the FPC. The PreAMP consists of an read preamplifier and a write current switch and senses a write error. Each channel is connected to each data head. The head IC switches the heads by the chip select signals (*CS) and the head select signals. The IC generates a write error sense

signal (WUS) when a write error occurs due to head short-circuit or head disconnection.

The Pre AMP sets the write current and bias current which flows through MR devices.

4.6.2 Write circuit

The write data is output from the hard disk controller (HDC) with the NRZ data format, and sent to the encoder circuit in the RDC. The NRZ write data is converted from 16-bit data to 17-bit data by the encoder circuit then sent to the PreAMP, and the data is written onto the media.

(1) 16/17 GCR

The disk drive converts data using the 16/17 (0, 12, 8) group coded recording (GCR) algorithm. This code follows a format in which 0 to 12 “0”s are inserted while the code bit is “1” and 0 to 8 “0”s are inserted while the 0DD/EVEN bit is “1”.

(2) Write precompensation

Write precompensation compensates, during a write process, for write non-leneartiry generated at reading. Table 4.2 shows the write precompensation algorithm.

Table 4.2 Write precompensation algorithm

Bits	Compensation
111001	–7
111010	–6
:	
111111	–1
000000	±0
000001	+1
:	
010000	+16
:	
100000	+32

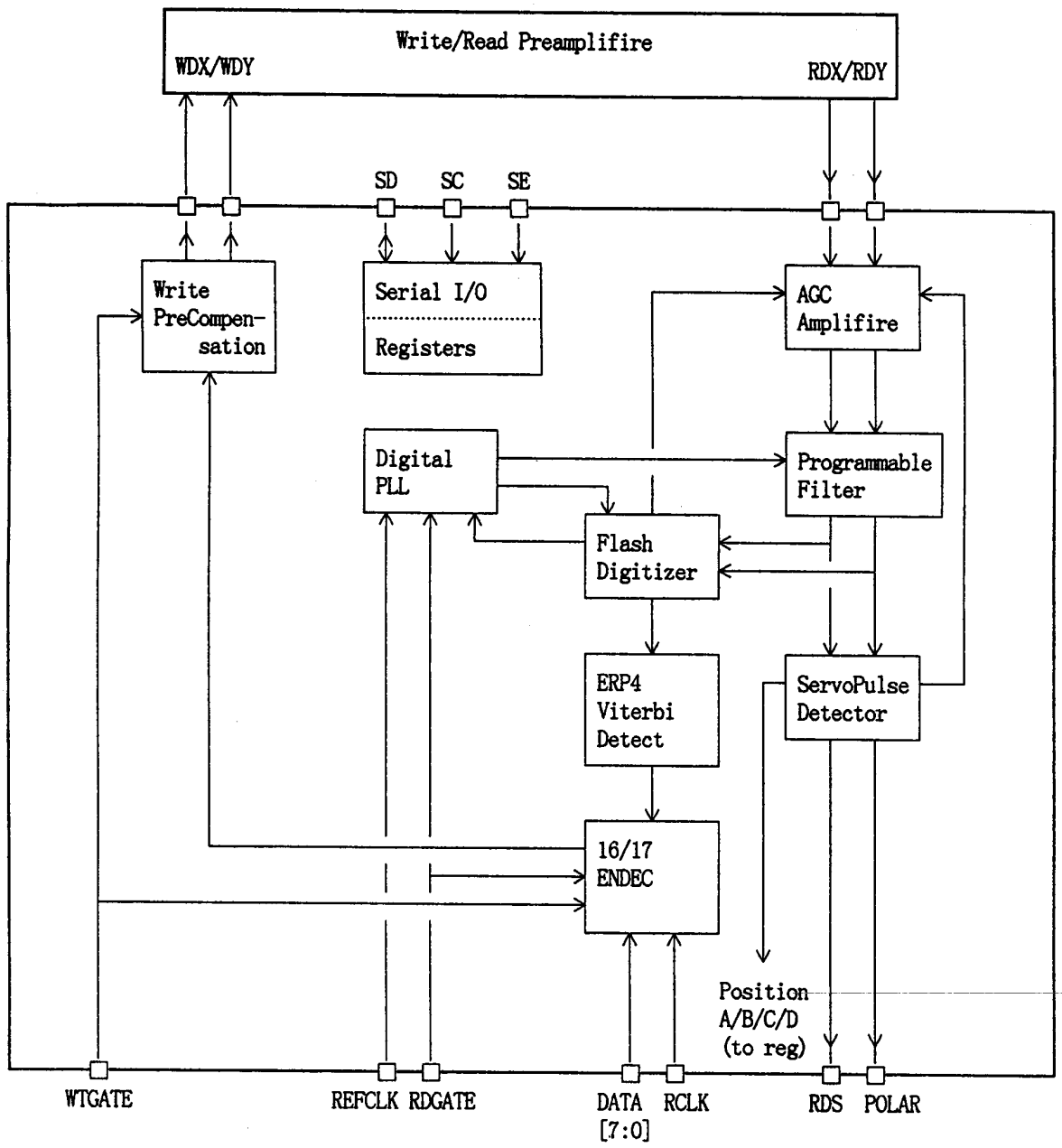


Figure 4.4 Read/write circuit block diagram

4.6.3 Read circuit

The head read signal from the PreAMP is regulated by the automatic gain control (AGC) circuit. Then the output is converted into the sampled read data pulse by the programmable filter circuit and the flash digitizer circuit. This clock signal is converted into the NRZ data by the 16/17 GCR decoder circuit based on the read data maximum-likelihood-detected by the Viterbi detection circuit, then is sent to the HDC.

(1) AGC circuit

The AGC circuit automatically regulates the output amplitude to a constant value even when the input amplitude level fluctuates. The AGC amplifier output is maintained at a constant level even when the head output fluctuates due to the head characteristics or outer/inner head positions.

(2) Programmable filter

The programmable filter circuit has a low-pass filter function that eliminates unnecessary high frequency noise component and a high frequency boost-up function that equalizes the waveform of the read signal.

Cut-off frequency of the low-pass filter and boost-up gain are controlled from the register in read channel by an instruction of the serial data signal from MPU (M5). The MPU optimizes the cut-off frequency and boost-up gain according to the transfer frequency of each zone.

Figure 4.5 shows the frequency characteristic sample of the programmalbe filter.

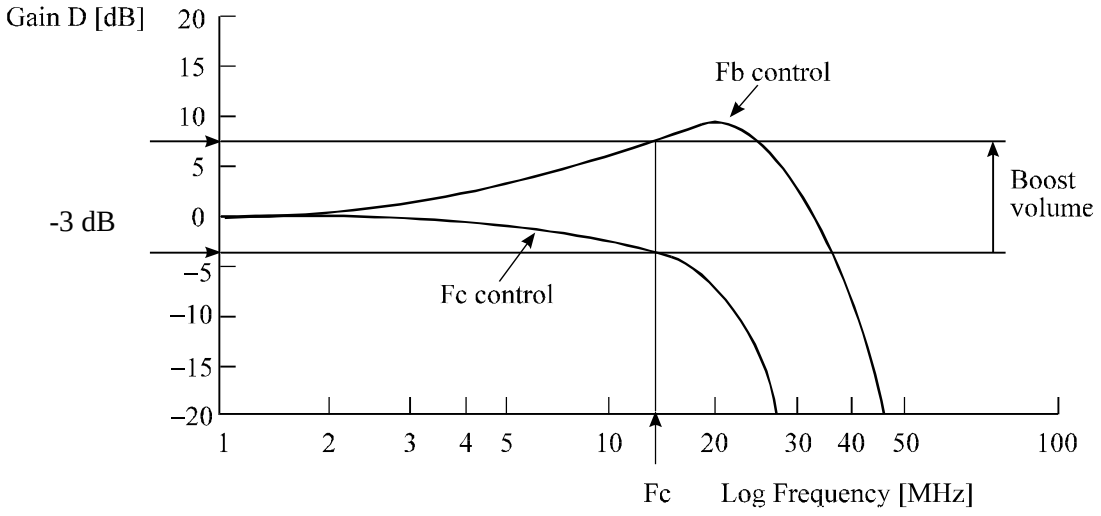


Figure 4.5 Frequency characteristic of programmable filter

(3) Flash digitizer circuit

This circuit is 10-tap sampled analog transversal filter circuit that cosine-equalizes the head read signal to the partial response class 4 (EPR4) waveform.

(4) Viterbi detection circuit

The sample hold waveform output from the flash digitizer circuit is sent to the Viterbi detection circuit. The Viterbi detection circuit demodulates data according to the survivor path sequence.

(5) 16/17 GCR decoder

This circuit converts the 17-bit read data into the 16-bit NRZ data.

4.6.4 Digital PLL circuit

The drive uses constant density recording to increase total capacity. This is different from the conventional method of recording data with a fixed data transfer rate at all data area. In the constant density recording method, data area is divided into zones by radius and the data transfer rate is set so that the recording density of the inner cylinder of each zone is nearly constant. The drive divides data area into 12 zones to set the data transfer rate.

The MPU transfers the data transfer rate setup data (SD/SC) to the RDC that includes the Digital PLL circuit to change the data transfer rate.

4.7 Servo Control

The actuator motor and the spindle motor are submitted to servo control. The actuator motor is controlled for moving and positioning the head to the track containing the desired data. To turn the disk at a constant velocity, the actuator motor is controlled according to the servo data that is written on the data side beforehand.

4.7.1 Servo control circuit

Figure 4.6 is the block diagram of the servo control circuit. The following describes the functions of the blocks:

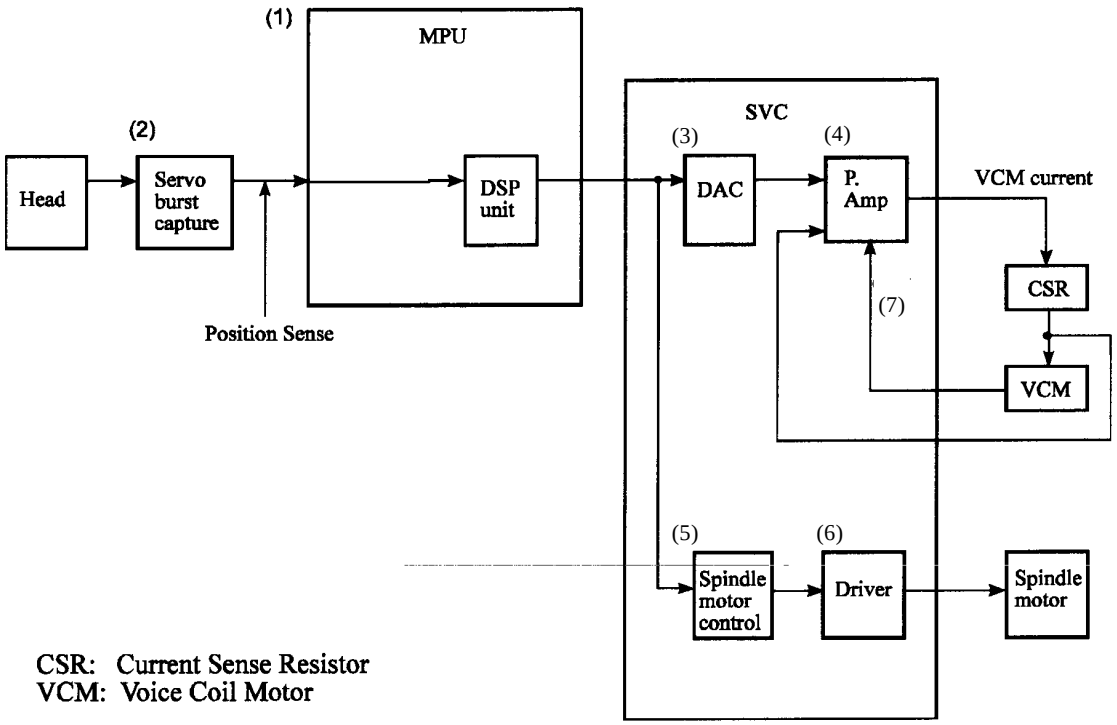


Figure 4.6 Block diagram of servo control circuit

(1) Microprocessor unit (MPU)

The MPU includes the DSP unit, and the MPU starts the spindle motor, moves the heads to the reference cylinders, seeks the specified cylinder, and executes calibration according to the internal operations of the MPU. Main internal operation of the MPU are shown below.

The major internal operations are listed below.

a. Spindle motor start

   Starts the spindle motor and accelerates it to normal speed when power is applied.

b. Move head to reference cylinder

   Drives the VCM to position the head at the any cylinder in the data area. The logical initial cylinder is at the outermost circumference (cylinder 0).

c. Seek to specified cylinder

   Drives the VCM to position the head to the specified cylinder.

d. Calibration

   Senses and stores the thermal offset between heads and the mechanical forces on the actuator, and stores the calibration value.

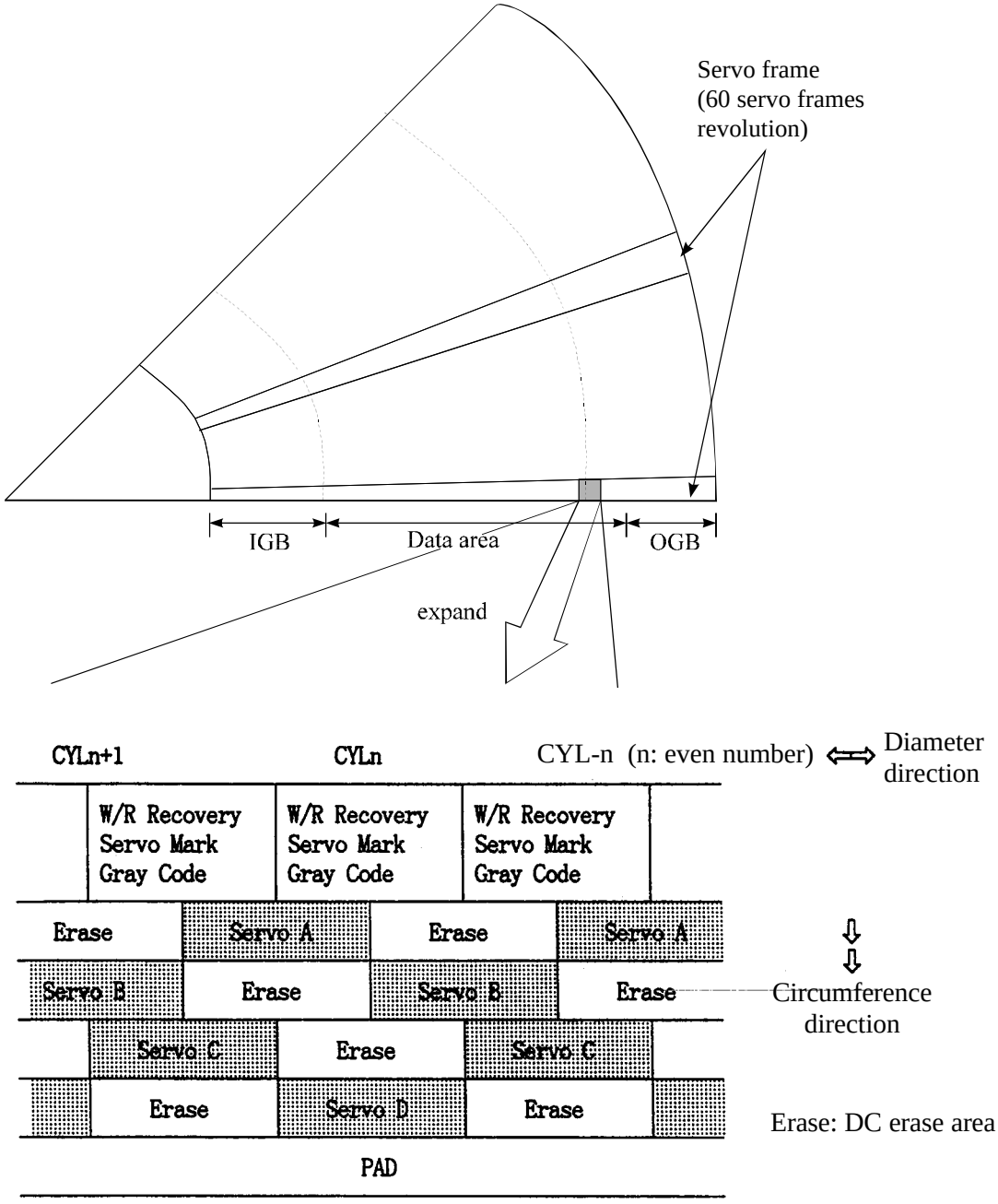


Figure 4.7 Physical sector servo configuration on disk surface

(2) Servo burst capture circuit

The servo burst capture circuit reproduces signals (position signals) that indicate the head position from the servo data on the data surface. SERVO A, SERVO B, SERVO C and SERVO D burst signals shown in Figure 4.8 followed the servo mark, cylinder gray and index information are output from the servo area on the data surface via the data head. The servo signals A/D-converts the amplitudes of the POSA, POSB, POSC and POSD signals at the peak hold circuit in the servo burst capture circuit at the timing of the STROB signal. At that time the AGC circuit is in hold mode. The A/D converted data is recognized by the MPU as position information with A-B and C-D processed.

(3) D/A converter (DAC)

The D/A converter (DAC) converts the VCM drive current value (digital value) calculated by the DSP unit into analog values and transfers them to the power amplifier.

(4) Power amplifier

The power amplifier feeds currents, corresponding to the DAC output signal voltage to the VCM.

(5) Spindle motor control circuit

The spindle motor control circuit controls the sensor-less spindle motor. This circuit detects number of revolution of the motor by the interrupt generated periodically, compares with the target revolution speed, then flows the current into the motor coil according to the differentation (abberration).

(6) Driver circuit

The driver circuit is a power amplitude circuit that receives signals from the spindle motor control circuit and feeds currents to the spindle motor.

(7) VCM current sense resistor (CSR)

This resistor controls current at the power amplifier by converting the VCM current into voltage and feeding back.

4.7.2 Data-surface servo format

Figure 4.7 describes the physical layout of the servo frame. The three areas indicated by (1) to (3) in Figure 4.7 are described below.

(1) Inner guard band

The head is in contact with the disk in this space when the spindle starts turning or stops, and the rotational speed of the spindle can be controlled on this cylinder area for head moving.

(2) Data area

This area is used as the user data area SA area.

(3) Outer guard band

This area is located at outer position of the user data area, and the rotational speed of the spindle can be controlled on this cylinder area for head moving.

4.7.3 Servo frame format

As the servo information, the IDD uses the two-phase servo generated from the gray code and servo A to D. This servo information is used for positioning operation of radius direction and position detection of circumstance direction.

The servo frame consists of 6 blocks; write/read recovery, servo mark, gray code, servo A to D, and PAD. Figure 4.8 shows the servo frame format.

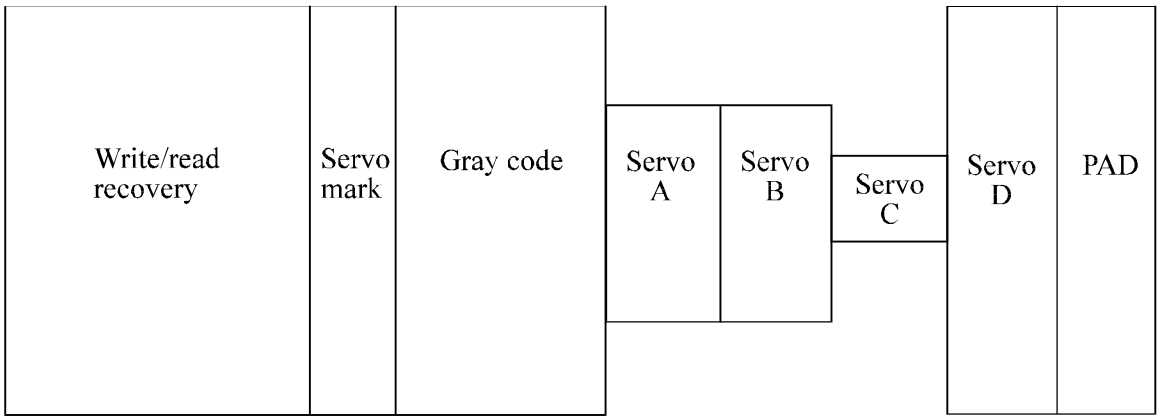


Figure 4.8 Servo frame format

(1) Write/read recovery

This area is used to absorb the write/read transient and to stabilize the AGC.

(2) Servo mark

This area gererates a timing for demodulating the gray code and position-demodulating the servo A to D by detecting the servo mark.

(3) Gray code (including index bit)

This area is used as cylinder address. The data in this area is converted into the binary data by the gray code demodulation circuit

(4) Servo A, servo B, servo C, servo D

This area is used as position signals between tracks, and the IDD control at on-track so that servo A level equals to servo B level.

(5) PAD

This area is used as a gap between servo and data.

4.7.4 Actuator motor control

The voice coil motor (VCM) is controlled by feeding back the servo data recorded on the data surface. The MPU fetches the position sense data on the servo frame at a constant interval of sampling time, executes calculation, and updates the VCM drive current.

The servo control of the actuator includes the operation to move the head to the reference cylinder, the seek operation to move the head to the target cylinder to read or write data, and the track-following operation to position the head onto the target track.

(1) Operation to move the head to the reference cylinder

The MPU moves the head to the reference cylinder when the power is turned. The reference cylinder is in the data area.

When power is applied the heads are moved from the inner circumference shunt zone to the normal servo data zone in the following sequence:

a) Micro current is fed to the VCM to press the head against the inner circumference.

b) Micro current is fed to the VCM to move the head toward the outer circumference.

c) When the servo mark is detected the head is moved slowly toward the outer circumference at a constant speed.

d) If the head is stopped at the reference cylinder from there. Track following control starts.

(2) Seek operation

Upon a data read/write request from the host, the MPU confirms the necessity of access to the disk. If a read/write instruction is issued, the MPU seeks the desired track.

The MPU feeds the VCM current via the D/A converter and power amplifier to move the head. The MPU calculates the difference (speed error) between the specified target position and the current position for each sampling timing during head moving. The MPU then feeds the VCM drive current by setting the calculated result into the D/A converter. The calculation is digitally executed by the firmware. When the head arrives at the target cylinder, the track is followed.

(3) Track following operation

Except during head movement to the reference cylinder and seek operation under the spindle rotates in steady speed, the MPU does track following control. To position the head at the center of a track, the DSP drives the VCM by feeding micro current. For each sampling time, the VCM drive current is determined by filtering the position difference between the target position and the position clarified by the detected position sense data. The filtering includes servo compensation. These are digitally controlled by the firmware.

4.7.5 Spindle motor control

Hall-less three-phase twelve-pole motor is used for the spindle motor, and the 3-phase full/half-wave analog current control circuit is used as the spindle motor driver (called SVC hereafter). The firmware operates on the MPU manufactured by Fujitsu. The spindle motor is controlled by sending several signals from the MPU to the SVC. There are three modes for the spindle control; start mode, acceleration mode, and stable rotation mode.

(1) Start mode

When power is supplied, the spindle motor is started in the following sequence:

a) After the power is turned on, the MPU sends a signal to the SVC to charge the charge pump capacitor of the SVC. The charged amount defines the current that flows in the spindle motor.

b) When the charge pump capacitor is charged enough, the MPU sets the SVC to the motor start mode. Then, a current (approx. 0.7 A) flows into the spindle motor.

c) The SVC generates a phase switching signal by itself, and changes the phase of the current flowed in the motor in the order of (V-phase to U-phase), (W-phase to U-phase), (W-phase to V-phase), (U-phase to V-phase), (U-phase to W-phase), and (V-phase to W-phase) (after that, repeating this order).

d) During phase switching, the spindle motor starts rotating in low speed, and generates a counter electromotive force. The SVC detects this counter electromotive force and reports to the MPU using a PHASE signal for speed detection.

e) The MPU is waiting for a PHASE signal. When no phase signal is sent for a sepcific period, the MPU resets the SVC and starts from the beginning. When a PHASE signal is sent, the SVC enters the acceleration mode.

(2) Acceleration mode

In this mode, the MPU stops to send the phase switching signal to the SVC. The SVC starts a phase switching by itself based on the counter electromotive force. Then, rotation of the spindle motor accelerates. The MPU calcurates a rotational speed of the spindle motor based on the PHASE signal from the SVC, and accelerates till the rotational speed reaches 4,000 rpm. When the rotational speed reaches 4,000 rpm, the SVC enters the stable rotation mode.

(3) Stable rotation mode

The MPU calcurates a time for one revolution of the spindle motor based on the PHASE signal from the SVC. The MPU takes a difference between the current time and a time for one revolution at 4,000 rpm that the MPU already recognized. Then, the MPU keeps the rotational speed to 4,000 rpm by charging or discharging the charge pump for the different time. For example, when the actual rotational speed is 3,800 rpm, the time for one revolution is 15.789 ms. And, the time for one revolution at 4,000 rpm is 15 ms. Therefore, the MPU charges the charge pump for 0.789 ms $\times$ k (k: constant value). This makes the flowed current into the motor higher and the rotational speed up. When the actual rotational speed is faster than 4,000 rpm, the MPU discharges the pump the other way. This control (charging/discharging) is performed every 1 revolution.

CHAPTER 5 Interface

This chapter gives details about the interface, and the interface commands and timings.

5.1 Physical Interface

5.1.1 Interface signals

Figure 5.1 shows the interface signals.

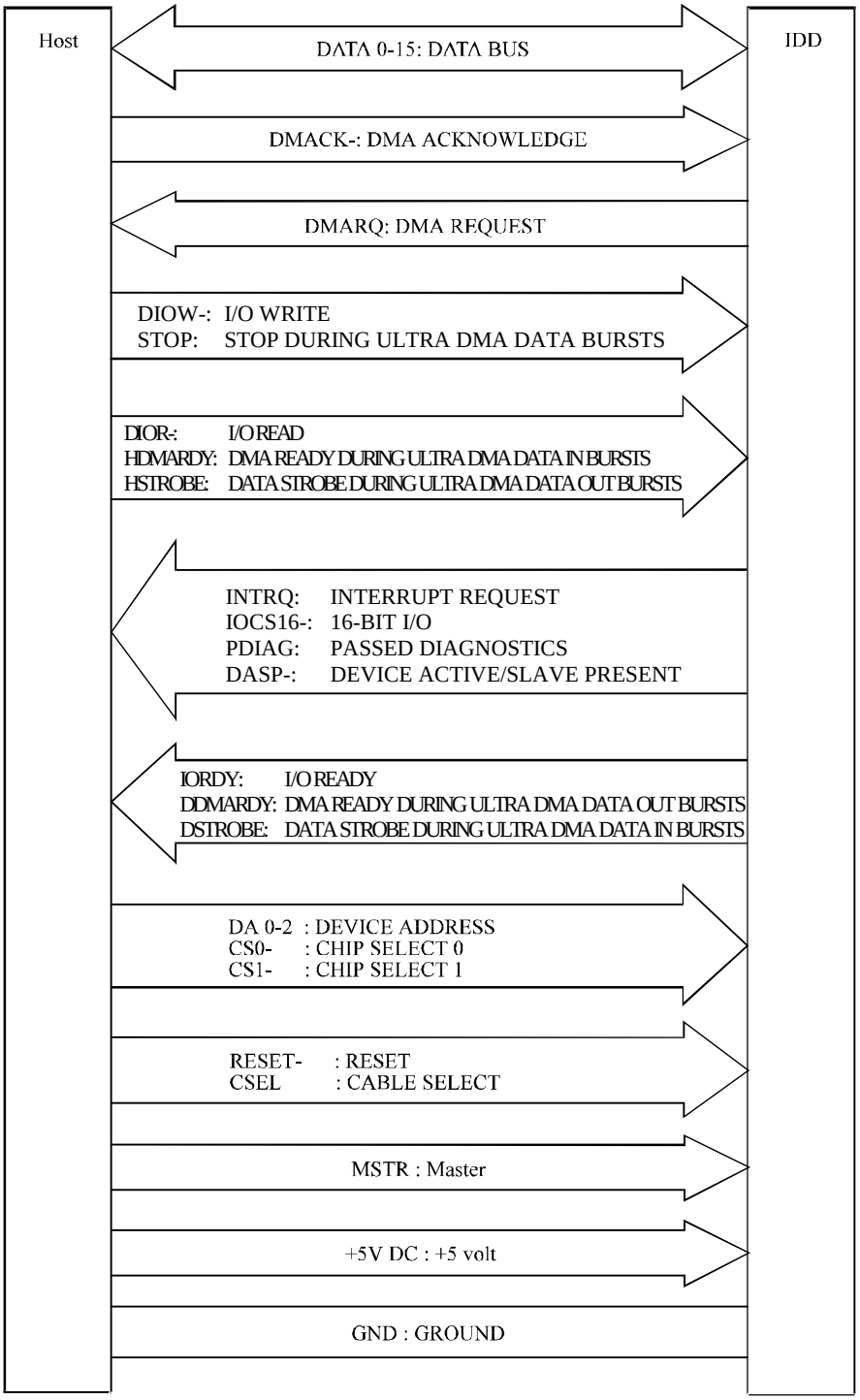


Figure 5.1 Interface signals

5.1.2 Signal assignment on the connector

Table 5.1 shows the signal assignment on the interface connector.

Table 5.1 Signal assignment on the interface connector

Pin No.	Signal	Pin No.	Signal
A	ENCSEL	B	GND
C	ENCSEL	D	MSTR
E	(KEY)	F	(KEY)
1	RESET–	2	GND
3	DATA7	4	DATA8
5	DATA6	6	DATA9
7	DATA5	8	DATA10
9	DATA4	10	DATA11
11	DATA3	12	DATA12
13	DATA2	14	DATA13
15	DATA1	16	DATA14
17	DATA0	18	DATA15
19	GND	20	(KEY)
21	DMARQ	22	GND
23	DIOW-, STOP	24	GND
25	DIOR-, HDMRDY, HSTROBE	26	GND
27	IORDY, DDMARDY, DSTROBE	28	CSEL
29	DMACK–	30	GND
31	INTRQ	32	IOCS16–
33	DA1	34	PDIAG
35	DA0	36	DA2
37	CS0–	38	CS1–
39	DASP–	40	GND
41	+5 VDC	42	+5 VDC
43	GND	44	unused

[signal]	[I/O]	[Description]
ENCSEL	I	This signal is used to set master/slave using the CSEL signal (pin 28). Pins A and C Open: Sets master/slave by the MSTR signal without using the CSEL signal. Short: Sets master/slave using the CSEL signal. The MSTR signal is ignored.
MSTR	I	MSTR, I, Master/slave setting 1: Master 0: Slave
RESET-	I	Reset signal from the host. This signal is low active and is asserted for a minimum of 25 µs during power on.
DATA 0-15	I/O	Sixteen-bit bi-directional data bus between the host and the device. These signals are used for data transfer
DIOW-	I	Signal asserted by the host to write to the device register or data port.
STOP	I	DIOW- must be negated by the host before starting the Ultra DMA transfer. The STOP signal must be negated by the host before data is transferred during the Ultra DMA transfer. During data transfer in Ultra DMA mode, the assertion of the STOP signal asserted by the host later indicates that the transfer has been suspended.
DIOR-	I	Read strobe signal from the host to read the device register or data port
HDMARDY-	I	Flow control signal for Ultra DMA data In transfer (READ DMA command). This signal is asserted by the host to inform the device that the host is ready to receive the Ultra DMA data In transfer. The host can negate the HDMARDY- signal to suspend the Ultra DMA data In transfer.
HSTROBE	I	Data Out Strobe signal from the host during Ultra DMA data Out transfer (WRITE DMA command). Both the rising and falling edges of the HSTROBE signal latch data from Data 15-0 into the device. The host can suspend the inversion of the HSTROBE signal to suspend the Ultra DMA data Out transfer.
INTRQ	O	Interrupt signal to the host. This signal is negated in the following cases: – assertion of RESET- signal – Reset by SRST of the Device Control register – Write to the command register by the host – Read of the status register by the host – Completion of sector data transfer (without reading the Status register) The signal output line has a high impedance when no devices are selected or interruption is disabled.

[signal]	[I/O]	[Description]
IOCS16-	O	This signal indicates 16-bit data bus is addressed in PIO data transfer. This signal is an open collector output. – When IOCS16- is not asserted: 8 bit data is transferred through DATA0 to DATA7 signals. – When IOCS16- is asserted: 16 bit data is transferred through DATA0 to DATA15 signals.
CS0-	I	Chip select signal decoded from the host address bus. This signal is used by the host to select the command block registers.
CS1-	I	Chip select signal decoded from the host address bus. This signal is used by the host to select the control block registers.
DA 0-2	I	Binary decoded address signals asserted by the host to access task file registers.
KEY	-	Key pin for prevention of erroneous connector insertion
PDIAG-	I/O	This signal is an input mode for the master device and an output mode for the slave device in a daisy chain configuration. This signal indicates that the slave device has been completed self diagnostics. This signal is pulled up to +5 V through 10 kΩ resistor at each device.
DASP-	I/O	This is a time-multiplexed signal that indicates that the device is active and a slave device is present. This signal is pulled up to +5 V through 10 kΩ resistor at each device.
IORDY	O	This signal requests the host system to delay the transfer cycle when the device is not ready to respond to a data transfer request from the host system.
DDMARDY-	O	Flow control signal for Ultra DMA data Out transfer (WRITE DMA command). This signal is asserted by the device to inform the host that the device is ready to receive the Ultra DMA data Out transfer. The device can negate the DDMARDY- signal to suspend the Ultra DMA data Out transfer.
DSTROBE	O	Data In Strobe signal from the device during Ultra DMA data In transfer. Both the rising and falling edges of the DSTROBE signal latch data from Data 15-0 into the host. The device can suspend the inversion of the DSTROBE signal to suspend the Ultra DMA data In transfer.
CSEL	I	This signal to configure the device as a master or a slave device. – When CSEL signal is grounded,, the IDD is a master device. – When CSEL signal is open,, the IDD is a slave device. This signal is pulled up with 240 kΩ resistor at each device.
DMACK-	I	The host system asserts this signal as a response that the host system receive data or to indicate that data is valid.

[signal]	[I/O]	[Description]
DMARQ	O	This signal is used for DMA transfer between the host system and the device. The device asserts this signal when the device completes the preparation of DMA data transfer to the host system (at reading) or from the host system (at writing). The direction of data transfer is controlled by the DIOR and DIOW signals. This signal hand shakes with the DMACK-signal. In other words, the device negates the DMARQ signal after the host system asserts the DMACK signal. When there is other data to be transferred, the device asserts the DMARQ signal again. When the DMA data transfer is performed, IOCS16-, CS0- and CS1- signals are not asserted. The DMA data transfer is a 16-bit data transfer.
+5 VDC	I	+5 VDC power supplying to the device.
GND	-	Grounded signal at each signal wire.

Note:

"I" indicates input signal from the host to the device.

"O" indicates output signal from the device to the host.

"I/O" indicates common output or bi-directional signal between the host and the device.

5.2 Logical Interface

The device can operate for command execution in either address-specified mode; cylinder-head-sector (CHS) or Logical block address (LBA) mode. The IDENTIFY DEVICE information indicates whether the device supports the LBA mode. When the host system specifies the LBA mode by setting bit 6 in the Device/Head register to 1, HS3 to HS0 bits of the Device/Head register indicates the head No. under the LBA mode, and all bits of the Cylinder High, Cylinder Low, and Sector Number registers are LBA bits.

The sector No. under the LBA mode proceeds in the ascending order with the start point of LBA0 (defined as follows).

LBA0 = [Cylinder 0, Head 0, Sector 1]

Even if the host system changes the assignment of the CHS mode by the INITIALIZE DEVICE PARAMETER command, the sector LBA address is not changed.

LBA = [((Cylinder No.) × (Number of head) + (Head No.)) × (Number of sector/track)] + (Sector No.) − 1

5.2.1 I/O registers

Communication between the host system and the device is done through input-output (I/O) registers of the device.

These I/O registers can be selected by the coded signals, CS0-, CS1-, and DA0 to DA2 from the host system. Table 5.2. shows the coding address and the function of I/O registers.

Table 5.2 I/O registers

CS0–	CS1–	DA2	DA1	DA0	I/O registers		Host I/O address
					Read operation	Write operation	
Command block registers							
L	H	L	L	L	Data	Data	X’1F0’
L	H	L	L	H	Error Register	Features	X’1F1’
L	H	L	H	L	Sector Count	Sector Count	X’1F2’
L	H	L	H	H	Sector Number	Sector Number	X’1F3’
L	H	H	L	L	Cylinder Low	Cylinder Low	X’1F4’
L	H	H	L	H	Cylinder High	Cylinder High	X’1F5’
L	H	H	H	L	Device/Head	Device/Head	X’1F6’
L	H	H	H	H	Status	Command	X’1F7’
L	L	X	X	X	(Invalid)	(Invalid)	—
Control block registers							
H	L	H	H	L	Alternate Status	Device Control	X’3F6’
H	L	H	H	H	—	—	X’3F7’

Notes:

1. The Data register for read or write operation can be accessed by 16 bit data bus (DATA0 to DATA15).

2. The registers for read or write operation other than the Data registers can be accessed by 8 bit data bus (DATA0 to DATA7).

3. When reading the Drive Address register, bit 7 is high-impedance state.

4. H indicates signal level High and L indicates signal level Low.

   And the LBA mode is specified, the Device/Head, Cylinder High, Cylinder Low, and Sector Number registers indicate LBA bits 27 to 24, 23 to 16, 15 to 8, and 7 to 0.

5.2.2 Command block registers

(1) Data register (X'1F0')

The Data register is a 16-bit register for data block transfer between the device and the host system. Data transfer mode is PIO or DMA mode.

(2) Error register (X'1F1')

The Error register indicates the status of the command executed by the device. The contents of this register are valid when the ERR bit of the Status register is 1.

This register contains a diagnostic code after power is turned on, a reset , or the EXECUTIVE DEVICE DIAGNOSTIC command is executed.

[Status at the completion of command execution other than diagnostic command]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ICRC	UNC	X	IDNF	X	ABRT	TK0NF	AMNF

X: Unused

- Bit 7: Interface CRC Error (ICRC). This bit indicates that a CRC error occurred during Ultra DMA transfer.
- Bit 6: Uncorrectable Data Error (UNC). This bit indicates that an uncorrectable data error has been encountered.
- Bit 5: Unused
- Bit 4: ID Not Found (IDNF). This bit indicates an error except for bad sector, uncorrectable error and SB not found.
- Bit 3: Unused
- Bit 2: Aborted Command (ABRT). This bit indicates that the requested command was aborted due to a device status error (e.g. Not Ready, Write Fault) or the command code was invalid.
- Bit 1: Track 0 Not Found (TK0NF). This bit indicates that track 0 was not found during RECALIBRATE command execution.
- Bit 0: Address Mark Not Found (AMNF). This bit indicates that the SB Not Found error occurred.

[Diagnostic code]

X'01': No Error Detected.

X'02': HDC Register Compare Error

X'03': Data Buffer Compare Error.

X'05': ROM Sum Check Error.

X'80': Device 1 (slave device) Failed.

Error register of the master device is valid under two devices (master and slave) configuration. If the slave device fails, the master device posts X'80' OR (the diagnostic code) with its own status (X'01' to X'05').

However, when the host system selects the slave device, the diagnostic code of the slave device is posted.

(3) Features register (X'1F1')

The Features register provides specific feature to a command. For instance, it is used with SET FEATURES command to enable or disable caching.

(4) Sector Count register (X'1F2')

The Sector Count register indicates the number of sectors of data to be transferred in a read or write operation between the host system and the device. When the value in this register is X'00', the sector count is 256.

When this register indicates X'00' at the completion of the command execution, this indicates that the command is completed succefully. If the command is not completed scuccessfully, this register indicates the number of sectors to be transferred to complete the request from the host system. That is, this register indicates the number of remaining sectors that the data has not been transferred due to the error.

The contents of this register has other definition for the following commands; INITIALIZE DEVICE PARAMETERS, SET FEATURES, IDLE, STANDBY and SET MULTIPLE MODE.

(5) Sector Number register (X'1F3')

The contents of this register indicates the starting sector number for the subsequent command. The sector number should be between X'01' and [the number of sectors per track defined by INITIALIZE DEVICE PARAMETERS command.

Under the LBA mode, this register indicates LBA bits 7 to 0.

(6) Cylinder Low register (X'1F4')

The contents of this register indicates low-order 8 bits of the starting cylinder address for any disk-access.

At the end of a command, the contents of this register are updated to the current cylinder number.

Under the LBA mode, this register indcates LBA bits 15 to 8.

(7) Cylinder High register (X'1F5')

The contents of this register indicates high-order 8 bits of the disk-access start cylinder address.

At the end of a command, the contents of this register are updated to the current cylinder number. The high-order 8 bits of the cylinder address are set to the Cylinder High register.

Under the LBA mode, this register indicates LBA bits 23 to 16.

(8) Device/Head register (X'1F6')

The contents of this register indicate the device and the head number.

When executing INITIALIZE DEVICE PARAMETERS command, the contents of this register defines "the number of heads minus 1" (a maximum head No.).

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	L	X	DEV	HS3	HS2	HS1	HS0

- Bit 7: Unused
- Bit 6: L. 0 for CHS mode and 1 for LBA mode.
- Bit 5: Unused
- Bit 4: DEV bit. 0 for the master device and 1 for the slave device.
- Bit 3: HS3 CHS mode head address 3 (2^3). LBA bit 27.
- Bit 2: HS2 CHS mode head address 2 (2^2). LBA bit 26.
- Bit 1: HS1 CHS mode head address 1 (2^1). LBA bit 25.
- Bit 0: HS0 CHS mode head address 0 (2^0). LBA bit 24.

(9) Status register (X'1F7')

The contents of this register indicate the status of the device. The contents of this register are updated at the completion of each command. When the BSY bit is cleared, other bits in this register should be validated within 400 ns. When the BSY bit is 1, other bits of this register are invalid. When the host system reads this register while an interrupt is pending, it is considered to be the Interrupt Acknowledge (the host system acknowledges the interrupt). Any pending interrupt is cleared (negating INTRQ signal) whenever this register is read.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BSY	DRDY	DF	DSC	DRQ	0	0	ERR

- Bit 7: Busy (BSY) bit. This bit is set whenever the Command register is accessed. Then this bit is cleared when the command is completed. However, even if a command is being executed, this bit is 0 while data transfer is being requested (DRQ bit = 1).When BSY bit is 1, the host system should not write the command block registers. If the host system reads any command block register when BSY bit is 1, the contents of the Status register are posted. This bit is set by the device under following conditions:

  (a) Within 400 ns after RESET- is negated or SRST is set in the Device Control register, the BSY bit is set. the BSY bit is cleared, when the reset process is completed.

  The BSY bit is set for no longer than 15 seconds after the IDD accepts reset.

  (b) Within 400 ns from the host system starts writing to the Command register.

  (c) Within 5 µs following transfer of 512 bytes data during execution of the READ SECTOR(S), WRITE SECTOR(S), or WRITE BUFFER command.

  Within 5 µs following transfer of 512 bytes of data and the appropriate number of ECC bytes during execution of READ LONG or WRITE LONG command.

- Bit 6: Device Ready (DRDY) bit. This bit indicates that the device is capable to respond to a command.

  The IDD checks its status when it receives a command. If an error is detected (not ready state), the IDD clears this bit to 0. This is cleared to 0 at power-on and it is cleared until the rotational speed of the spindle motor reaches the steady speed.

- Bit 5: The Device Write Fault (DF) bit. This bit indicates that a device fault (write fault) condition has been detected.

  If a write fault is detected during command execution, this bit is latched and retained until the device accepts the next command or reset.

- Bit 4: Device Seek Complete (DSC) bit. This bit indicates that the device heads are positioned over a track.

  In the IDD, this bit is always set to 1 after the spin-up control is completed.

- Bit 3: Data Request (DRQ) bit. This bit indicates that the device is ready to transfer data of word unit or byte unit between the host system and the device.

- Bit 2: Always 0.

- Bit 1: Always 0.

- Bit 0: Error (ERR) bit. This bit indicates that an error was detected while the previous command was being executed. The Error register indicates the additional information of the cause for the error.

(10) Command register (X'1F7')

The Command register contains a command code being sent to the device. After this register is written, the command execution starts immediately.

Table 5.3 lists the executable commands and their command codes. This table also lists the neccesary parameters for each command which are written to certain registers before the Command register is written.

5.2.3 Control block registers

(1) Alternate Status register (X'3F6')

The Alternate Status register contains the same information as the Status register of the command block register.

The only difference from the Status register is that a read of this register does not imply Interrupt Acknowledge and INTRQ signal is not reset.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BSY	DRDY	DF	DSC	DRQ	0	0	ERR

(2) Device Control register (X'3F6')

The Device Control register contains device interrupt and software reset.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	X	SRST	nIEN	0

- Bit 2: SRST is the host software reset bit. When this bit is set, the device is held reset state. When two device are daisy chained on the interface, setting this bit resets both device simultaneously.

  The slave device is not required to execute the DASP- handshake.

- Bit 1: nIEN bit enables an interrupt (INTRQ signal) from the device to the host. When this bit is 0 and the device is selected, an interruption (INTRQ signal) can be enabled through a tri-state buffer. When this bit is 1 or the device is not selected, the INTRQ signal is in the high-impedance state.

5.3 Host Commands

The host system issues a command to the device by writing necessary parameters in related registers in the command block and writing a command code in the Command register.

The device can accept the command when the BSY bit is 0 (the device is not in the busy status).

The host system can halt the uncompleted command execution only at execution of hardware or software reset.

When the BSY bit is 1 or the DRQ bit is 1 (the device is requesting the data transfer) and the host system writes to the command register, the correct device operation is not guaranteed.

5.3.1 Command code and parameters

Table 5.3 lists the supported commands, command code and the registers that needed parameters are written.

Table 5.3 Command code and parameters (1 of 2)

Command name	Command code (Bit)								Parameters used				
	7	6	5	4	3	2	1	0	FR	SC	SN	CY	DH
READ SECTOR(S)	0	0	1	0	0	0	0	R	N	Y	Y	Y	Y
READ MULTIPLE	1	1	0	0	0	1	0	0	N	Y	Y	Y	Y
READ DMA	1	1	0	0	1	0	0	R	N	Y	Y	Y	Y
READ VERIFY SECTOR(S)	0	1	0	0	0	0	0	R	N	Y	Y	Y	Y
WRITE MULTIPLE	1	1	0	0	0	1	0	1	N	Y	Y	Y	Y
WRITE DMA	1	1	0	0	1	0	1	R	N	Y	Y	Y	Y
WRITE VERIFY	0	0	1	1	1	1	0	0	N	Y	Y	Y	Y
WRITE SECTOR(S)	0	0	1	1	0	0	0	R	N	Y	Y	Y	Y
RECALIBRATE	0	0	0	1	X	X	X	X	N	N	N	N	D
SEEK	0	1	1	1	X	X	X	X	N	N	Y	Y	Y
INITIALIZE DEVICE PARAMETERS	1	0	0	1	0	0	0	1	N	Y	N	N	Y
IDENTIFY DEVICE	1	1	1	0	1	1	0	0	N	N	N	N	D
IDENTIFY DEVICE DMA	1	1	1	0	1	1	0	0	N	N	N	N	D
SET FEATURES	1	1	1	0	1	1	1	1	Y	N*	N	N	D
SET MULTIPLE MODE	1	1	0	0	0	1	1	0	N	Y	N	N	D
EXECUTE DEVICE DIAGNOSTIC	1	0	0	1	0	0	0	0	N	N	N	N	D*
READ LONG	0	0	1	0	0	0	1	R	N	Y	Y	Y	Y
WRITE LONG	0	0	1	1	0	0	1	R	N	Y	Y	Y	Y
READ BUFFER	1	1	1	0	0	1	0	0	N	N	N	N	D
WRITE BUFFER	1	1	1	0	1	0	0	0	N	N	N	N	D
IDLE	1 1	0 1	0 1	1 0	0 0	1 0	1 1	1 1	N	Y	N	N	D

Table 5.3 Command code and parameters (2 of 2)

Command name	Command code (Bit)								Parameters used				
	7	6	5	4	3	2	1	0	FR	SC	SN	CY	DH
IDLE IMMEDIATE	1 1	0 1	0 1	1 0	0 0	1 0	0 0	1 1	N	N	N	N	D
STANDBY	1 1	0 1	0 1	1 0	0 0	1 0	1 1	0 0	N	Y	N	N	D
STANDBY IMMEDIATE	1 1	0 1	0 1	1 0	0 0	1 0	0 0	0 0	N	N	N	N	D
SLEEP	1 1	0 1	0 1	1 0	1 0	0 1	0 1	1 0	N	N	N	N	D
CHECK POWER MODE	1 1	0 1	0 1	1 0	1 0	0 1	0 0	0 1	N	N	N	N	D
SMART	1	0	1	1	0	0	0	0	Y	Y	Y	Y	D
SECURITY DISABLE PASSWORD	1	1	1	1	0	1	1	0	N	N	N	N	D
SECURITY ERASE PREPARE	1	1	1	1	0	0	1	1	N	N	N	N	D
SECURITY ERASE UNIT	1	1	1	1	0	1	0	0	N	N	N	N	D
SECURITY FREEZE LOCK	1	1	1	1	0	1	0	1	N	N	N	N	D
SECURITY SET PASSWORD	1	1	1	1	0	0	0	1	N	N	N	N	D
SECURITY UNLOCK	1	1	1	1	0	0	1	0	N	N	N	N	D
FLUSH CACHE	1	1	1	0	0	1	1	1	N	N	N	N	D

Notes:

FR: Features Register

CY: Cylinder Registers

SC: Sector Count Register

DH: Drive/Head Register

SN: Sector Number Register

R: Retry at error

1 = Without retry

0 = with retry

Y: Necessary to set parameters

Y*: Necessary to set parameters under the LBA mode.

N: Not necessary to set parameters (The parameter is ignored if it is set.)

N*: May set parameters

D: The device parameter is valid, and the head parameter is ignored.

D*: The command is addressed to the master device, but both the master device and the slave device execute it.

X: Do not care

5.3.2 Command descriptions

The contents of the I/O registers to be necessary for issuing a command and the example indication of the I/O registers at command conpletion are shown as following in this subsection.

Example: READ SECTOR(S) WITH RETRY

At command issuance (I/O registers setting contents)								
Bit	7	6	5	4	3	2	1	0
$1F7_H$(CM)	0	0	1	0	0	0	0	0
$1F6_H$(DH)	×	L	×	DV	Head No. / LBA [MSB]			
$1F5_H$(CH)	Start cylinder address [MSB] / LBA							
$1F4_H$(CL)	Start cylinder address [LSB] / LBA							
$1F3_H$(SN)	Start sector No. / LBA [LSB]							
$1F2_H$(SC)	Transfer sector count							
$1F1_H$(FR)	xx							

At command completion (I/O registers contents to be read)								
Bit	7	6	5	4	3	2	1	0
$1F7_H$(ST)	Status information							
$1F6_H$(DH)	×	L	×	DV	Head No. / LBA [MSB]			
$1F5_H$(CH)	End cylinder address [MSB] / LBA							
$1F4_H$(CL)	End cylinder address [LSB] / LBA							
$1F3_H$(SN)	End sector No. / LBA [LSB]							
$1F2_H$(SC)	X’00’							
$1F1_H$(ER)	Error information							

CM: Command register	FR: Features register
DH: Device/Head register	ST: Status register
CH: Cylinder High register	ER: Error register
CL: Cylinder Low register	L: LBA (logical block address) setting bit
SN: Sector Number register	DV: Device address. bit
SC: Sector Count register	x, xx: Do not care (no necessary to set)

Note:

1. When the L bit is specified to 1, the lower 4 bits of the DH register and all bits of the CH, CL and SN registers indicate the LBA bits (bits of the DH register are the MSB (most significant bit) and bits of the SN register are the LSB (least significant bit).

2. At error occurrance, the SC register indicates the remaining sector count of data transfer.

3. In the table indicating I/O registers contents in this subsection, bit indication is omitted.

(1) READ SECTOR(S) (X'20' or X'21')

This command reads data of sectors specified in the Sector Count register from the address specified in the Device/Head, Cylinder High, Cylinder Low and Sector Number registers. Number of sectors can be specified to 256 sectors in maximum. To specify 256 sectors reading, '00' is specified. For the DRQ, INTRQ, and BSY protocols related to data transfer, see Subsection 5.4.1.

If the head is not on the track specified by the host, the device performs a implied seek. After the head reaches to the specified track, the device reads the target sector.

A maximum of 252 retry reads are attempted to read the target sector before reporting an error, irrespective of the R bit setting.

The DRQ bit of the Status register is always set prior to the data transfer regardless of an error condition.

Upon the completion of the command execution, command block registers contain the cylinder, head, and sector addresses (in the CHS mode) or logical block address (in the LBA mode) of the last sector read.

If an error occurs in a sector, the read operation is terminated at the sector where the error occured.

Command block registers contain the cylinder, the head, and the sector addresses of the sector (in the CHS mode) or the logical block address (in the LBA mode) where the error occurred, and remaining number of sectors of which data was not transferred.

At command issuance (I/O registers setting contents)								
$1F7_H$(CM)	0	0	1	0	0	0	0	R
$1F6_H$(DH)	×	L	×	DV	Start head No. /LBA [MSB]			
$1F5_H$(CH)	Start cylinder No. [MSB] / LBA							
$1F4_H$(CL)	Start cylinder No. [LSB] / LBA							
$1F3_H$(SN)	Start sector No. / LBA [LSB]							
$1F2_H$(SC)	Transfer sector count							
$1F1_H$(FR)	xx							

R = 0 →with Retry
R = 1 →without Retry

At command completion (I/O registers contents to be read)					
$1F7_H$(ST)	Status information				
$1F6_H$(DH)	×	L	×	DV	End head No. /LBA [MSB]
$1F5_H$(CH)	End cylinder No. [MSB] / LBA				
$1F4_H$(CL)	End cylinder No. [LSB] / LBA				
$1F3_H$(SN)	End sector No. / LBA [LSB]				
$1F2_H$(SC)	00 (*1)				
$1F1_H$(ER)	Error information				

*1 If the command is terminated due to an error, the remaining number of sectors of which data was not transferred is set in this register.

(2) READ MULTIPLE (X'C4')

This command operates similarly to the READ SECTOR(S) command. The device does not generate an interrupt (assertion of the INTRQ signal) on each every sector. An interrupt is generateed after the transfer of a block of sectors for which the number is specified by the SET MULTIPLE MODE command.

The implementation of the READ MULTIPLE command is identical to that of the READ SECTOR(S) command except that the number of sectors is specified by the SET MULTIPLE MODE command are transferred without intervening interrupts. In the READ MULTIPLE command operation, the DRQ bit of the Status register is set only at the start of the data block, and is not set on each sector.

The number of sectors (block count) to be transferred without interruption is specifed by the SET MULTIPLE MODE command. The SET MULTIPLE MODE command should be executed prior to the READ MULTIPLE command.

When the READ MULTIPLE command is issued, the Sector Count register contains the number of sectors requested (not a number of the block count or a number of sectors in a block).

Upon receipt of this command, the device executes this command even if the value of the Sector Count register is less than the defined block count (the value of the Sector Count should not be 0).

If the number of requested sectors is not divided evenly (having the same number of sectors [block count]), as many full blocks as possible are transferred, then a final partial block is transferred. The number of sectors in the partial block to be transferred is n where n = remainder of (“number of sectors”/”block count”).

If the READ MULTIPLE command is issued before the SET MULTIPLE MODE command is executed or when the READ MULTIPLE command is disabled, the device rejects the READ MULTIPLE command with an ABORTED COMMAND error.

If an error occurs, reading sector is stopped at the sector where the error occurred. Command block registers contain the cylinder, the head, the sector addresses (in the CHS mode) or the logical block address (in the LBA mode) of the sector where the error occurred, and remaining number of sectors that had not transferred after the sector where the error occurred.

An interrupt is generated when the DRQ bit is set at the beginning of each block or a partial block.

Figure 5.2 shows an example of the execution of the READ MULTIPLE command.

- Block count specified by SET MULTIPLE MODE command = 4 (number of sectors in a block)
- READ MULTIPLE command specifies;

Number of requested sectors = 9 (Sector Count register = 9)

↓

Number of sectors in incomplete block = remainder of 9/4 =1

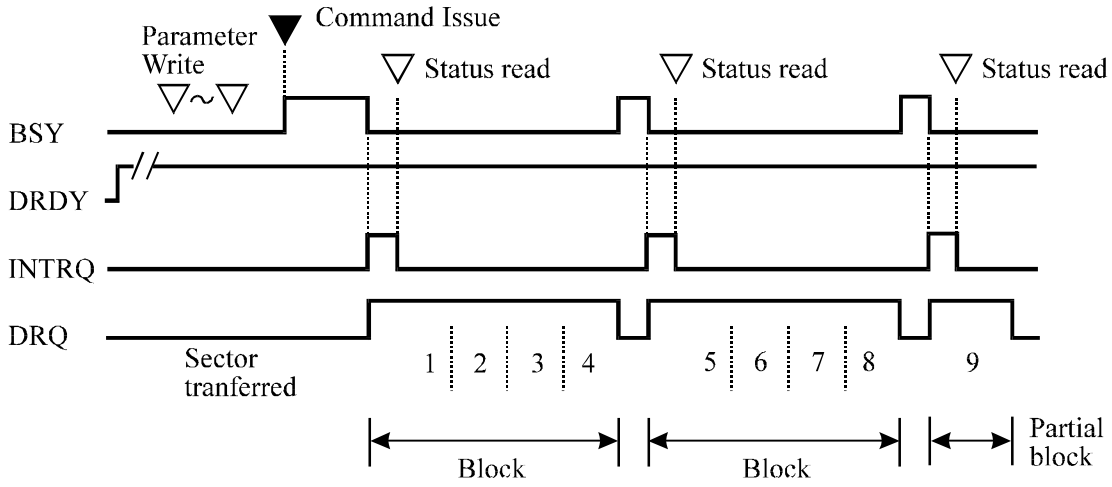


Figure 5.2 Execution example of READ MULTIPLE command

At command issuance (I/O registers setting contents)								
$1F7_H$(CM)	1	1	0	0	0	1	0	0
$1F6_H$(DH)	×	L	×	DV	Start head No. /LBA [MSB]			
$1F5_H$(CH)	Start cylinder No. [MSB] / LBA							
$1F4_H$(CL)	Start cylinder No. [LSB] / LBA							
$1F3_H$(SN)	Start sector No. / LBA [LSB]							
$1F2_H$(SC)	Transfer sector count							
$1F1_H$(FR)	xx							

At command completion (I/O registers contents to be read)					
$1F7_H$(ST)	Status information				
$1F6_H$(DH)	×	L	×	DV	End head No. /LBA [MSB]
$1F5_H$(CH)	End cylinder No. [MSB] / LBA				
$1F4_H$(CL)	End cylinder No. [LSB] / LBA				
$1F3_H$(SN)	End sector No. / LBA [LSB]				
$1F2_H$(SC)	$00^{(*1)}$				
$1F1_H$(ER)	Error information				

*1 If the command is terminated due to an error, the remaining number of sectors for which data was not transferred is set in this register.

(3) READ DMA (X'C8' or X'C9')

This command operates similarly to the READ SECTOR(S) command except for following events.

- The data transfer starts at the timing of DMARQ signal assertion.
- The device controls the assertion or negation timing of the DMARQ signal.
- The device posts a status as the result of command execution only once at completion of the data transfer.

When an error, such as an unrecoverable medium error, that the command execution cannot be continued is detected, the data transfer is stopped without transferring data of sectors after the erred sector. The device generates an interrupt using the INTRQ signal and posts a status to the host system. The format of the error information is the same as the READ SECTOR(S) command.

In LBA mode

The logical block address is specified using the start head No., start cylinder No., and first sector No. fields. At command completion, the logical block address of the last sector and remaining number of sectors of which data was not transferred, like in the CHS mode, are set.

The host system can select the DMA transfer mode by using the SET FEATURES command.

1) Single word DMA transfer mode 0 to 2

2) Multiword DMA transfer mode 0 to 2

3) Ultra DMA transfer mode 0 to 2

At command issuance (I/O registers setting contents)								
$1F7_H$(CM)	1	1	0	0	1	0	0	R
$1F6_H$(DH)	×	L	×	DV	Start head No. /LBA [MSB]			
$1F5_H$(CH)	Start cylinder No. [MSB] / LBA							
$1F4_H$(CL)	Start cylinder No. [LSB] / LBA							
$1F3_H$(SN)	Start sector No. / LBA [LSB]							
$1F2_H$(SC)	Transfer sector count							
$1F1_H$(FR)	xx							

R = 0 → with Retry
R = 1 → without Retry

At command completion (I/O registers contents to be read)					
$1F7_H$(ST)	Status information				
$1F6_H$(DH)	×	L	×	DV	End head No. /LBA [MSB]
$1F5_H$(CH)	End cylinder No. [MSB] / LBA				
$1F4_H$(CL)	End cylinder No. [LSB] / LBA				
$1F3_H$(SN)	End sector No. / LBA [LSB]				
$1F2_H$(SC)	00 (*1)				
$1F1_H$(ER)	Error information				

*1 If the command is terminated due to an error, the remaining number of sectors of which data was not transferred is set in this register.

(4) READ VERIFY SECTOR(S) (X'40' or X'41')

This command operates similarly to the READ SECTOR(S) command except that the data is not transferred to the host system.

After all requested sectors are verified, the device clears the BSY bit of the Status register and generates an interrupt. Upon the completion of the command execution, the command block registers contain the cylinder, head, and sector number of the last sector verified.

If an error occurs, the verify operation is terminated at the sector where the error occurred. The command block registers contain the cylinder, the head, and the sector addresses (in the CHS mode) or the logical block address (in the LBA mode) of the sector where the error occurred. The Sector Count register indicates the number of sectors that have not been verified.

If a correctable error is found, the device sets the CORR bit of the Status register to 1 after the command is completed (before the device generates an interrupt).

At command issuance (I/O registers setting contents)								
$1F7_H$(CM)	0	1	0	0	0	0	0	R
$1F6_H$(DH)	×	L	×	DV	Start head No. /LBA [MSB]			
$1F5_H$(CH)	Start cylinder No. [MSB] / LBA							
$1F4_H$(CL)	Start cylinder No. [LSB] / LBA							
$1F3_H$(SN)	Start sector No. / LBA [LSB]							
$1F2_H$(SC)	Transfer sector count							
$1F1_H$(FR)	xx							

R = 0 →with Retry
R = 1 →without Retry

At command completion (I/O registers contents to be read)					
$1F7_H$(ST)	Status information				
$1F6_H$(DH)	×	L	×	DV	End head No. /LBA [MSB]
$1F5_H$(CH)	End cylinder No. [MSB] / LBA				
$1F4_H$(CL)	End cylinder No. [LSB] / LBA				
$1F3_H$(SN)	End sector No. / LBA [LSB]				
$1F2_H$(SC)	00 (*1)				
$1F1_H$(ER)	Error information				

*1 If the command is terminated due to an error, the remaining number of sectors of which data was not transferred is set in this register.

(5) WRITE SECTOR(S) (X'30' or X'31')

This command writes data of sectors from the address specified in the Device/Head, Cylinder High, Cylinder Low, and Sector Number registers to the address specified in the Sector Count register. Number of sectors can be specified to 256 sectors in maximum. Data transfer begins at the sector specified in the Sector Number register. For the DRQ, INTRQ, and BSY protocols related to data transfer, see Subsection 5.4.2.

If the head is not on the track specified by the host, the device performs a implied seek. After the head reaches to the the specified track, the device writes the target sector.

If an error occurs when writing to the target sector, a maximum of 63 retries are attempted before reporting the error, irrespective of the R bit setting.

The data stored in the buffer, and CRC code and ECC bytes are written to the data field of the corresponding sector(s). Upon the completion of the command execution, the command block registers contain the cylinder, head, and sector addresses of the last sector written.

If an error occurs during multiple sector write operation, the write operation is terminated at the sector where the error occured. Command block registers contain the cylinder, the head, the sector addresses (in the CHS mode) or the logical block address (in the LBA mode) of the sector where the error occurred. Then the host can read the command block registers to determine what error has occurred and on which sector the error has occurred.

At command issuance (I/O registers setting contents)								
$1F7_H$(CM)	0	0	1	1	0	0	0	R
$1F6_H$(DH)	×	L	×	DV	Start head No. /LBA [MSB]			
$1F5_H$(CH)	Start cylinder No. [MSB] / LBA							
$1F4_H$(CL)	Start cylinder No. [LSB] / LBA							
$1F3_H$(SN)	Start sector No. / LBA [LSB]							
$1F2_H$(SC)	Transfer sector count							
$1F1_H$(FR)	xx							

R = 0 →with Retry
R = 1 →without Retry

At command completion (I/O registers contents to be read)					
$1F7_H$(ST)	Status information				
$1F6_H$(DH)	×	L	×	DV	End head No. /LBA [MSB]
$1F5_H$(CH)	End cylinder No. [MSB] / LBA				
$1F4_H$(CL)	End cylinder No. [LSB] / LBA				
$1F3_H$(SN)	End sector No. / LBA [LSB]				
$1F2_H$(SC)	00 (*1)				
$1F1_H$(ER)	Error information				

*1 If the command is terminated due to an error, the remaining number of sectors of which data was not transferred is set in this register.

(6) WRITE MULTIPLE (X'C5')

This command is similar to the WRITE SECTOR(S) command. The device does not generate interrupts (assertion of the INTRQ) signal) on each sector but on the transfer of a block which contains the number of sectors for which the number is defined by the SET MULTIPLE MODE command.

The implementation of the WRITE MULTIPLE command is identical to that of the WRITE SECTOR(S) command except that the number of sectors is specified by the SET MULTIPLE MODE command are transferred without intervening interrupts. In the WRITE MULTIPLE command operation, the DRQ bit of the Status register is required to set only at the start of the data block, not on each sector.

The number of sectors (block count) to be transferred without interruption is specifed by the SET MULTIPLE MODE command. The SET MULTIPLE MODE command should be executed prior to the WRITE MULTIPLE command.

When the WRITE MULTIPLE command is issued, the Sector Count register contains the number of sectors requested (not a number of the block count or a number of sectors in a block).

Upon receipt of this command, the device executes this command even if the value of the Sector Count register is less than the defined block count the value of the Sector Count should not be 0).

If the number of requested sectors is not divided evenly (having the same number of sectors [block count]), as many full blocks as possible are transferred, then a final partial block is transferred. The number of sectors in the partial block to be transferred is n where n = remainder of ("number of sectors"/"block count").

If the WRITE MULTIPLE command is issued before the SET MULTIPLE MODE command is executed or when WRITE MULTIPLE command is disabled, the device rejects the WRITE MULTIPLE command with an ABORTED COMMAND error.

Disk errors encountered during execution of the WRITE MULTIPLE command are posted after attempting to write the block or the partial block that was transferred. Write operation ends at the sector where the error was encountered even if the sector is in the middle of a block. If an error occurs, the subsequent block shall not be transferred. Interrupts are generated when the DRQ bit of the Status register is set at the beginning of each block or partial block.

The contents of the command block registers related to addresses after the transfer of a data block containing an erred sector are undefined. To obtain a valid error information, the host should retry data transfer as an individual request.

At command issuance (I/O registers setting contents)								
$1F7_H$(CM)	1	1	0	0	0	1	0	1
$1F6_H$(DH)	×	L	×	DV	Start head No. /LBA [MSB]			
$1F5_H$(CH)	Start cylinder No. [MSB] / LBA							
$1F4_H$(CL)	Start cylinder No. [LSB] / LBA							
$1F3_H$(SN)	Start sector No. / LBA [LSB]							
$1F2_H$(SC)	Transfer sector count							
$1F1_H$(FR)	xx							

At command completion (I/O registers contents to be read)					
$1F7_H$(ST)	Status information				
$1F6_H$(DH)	×	L	×	DV	End head No. /LBA [MSB]
$1F5_H$(CH)	End cylinder No. [MSB] / LBA				
$1F4_H$(CL)	End cylinder No. [LSB] / LBA				
$1F3_H$(SN)	End sector No. / LBA [LSB]				
$1F2_H$(SC)	00				
$1F1_H$(ER)	Error information				

(7) WRITE DMA (X'CA' or X'CB')

This command operates similarly to the WRITE SECTOR(S) command except for following events.

- The data transfer starts at the timing of DMARQ signal assertion.
- The device controls the assertion or negation timing of the DMARQ signal.
- The device posts a status as the result of command execution only once at completion of the data transfer or completion of processing in the device.
- The device posts a status as the result of command execution only once at completion of the data transfer.

When an error, such as an unrecoverable medium error, that the command execution cannot be continued is detected, the data transfer is stopped without transferring data of sectors after the erred sector. The device generates an interrupt using the INTRQ signal and posts a status to the host system. The format of the error information is the same as the WRITE SECTOR(S) command.

A host system can select the following transfer mode using the SET FEATURES command.

1) Single word DMA transfer mode 0 to 2

2) Multiword DMA transfer mode 0 to 2

3) Ultra DMA transfer mode 0 to 2

At command issuance (I/O registers setting contents)								
$1F7_H$(CM)	1	1	0	0	1	0	1	R
$1F6_H$(DH)	×	L	×	DV	Start head No. /LBA [MSB]			
$1F5_H$(CH)	Start cylinder No. [MSB] / LBA							
$1F4_H$(CL)	Start cylinder No. [LSB] / LBA							
$1F3_H$(SN)	Start sector No. / LBA [LSB]							
$1F2_H$(SC)	Transfer sector count							
$1F1_H$(FR)	xx							

R = 0 →with Retry
R = 1 →without Retry

At command completion (I/O registers contents to be read)					
$1F7_H$(ST)	Status information				
$1F6_H$(DH)	×	L	×	DV	End head No. /LBA [MSB]
$1F5_H$(CH)	End cylinder No. [MSB] / LBA				
$1F4_H$(CL)	End cylinder No. [LSB] / LBA				
$1F3_H$(SN)	End sector No. / LBA [LSB]				
$1F2_H$(SC)	00 (*1)				
$1F1_H$(ER)	Error information				

*1 If the command is terminated due to an error, the remaining number of sectors of which data was not transferred is set in this register.

(8) WRITE VERIFY (X'3C')

This command operates similarly to the WRITE SECTOR(S) command except that the device verifies each sector immediately after being written. The verify operation is a read and check for data errors without data transfer. Any error that is detected during the verify operation is posted.

After all sectors are verified, the last interruption (INTRQ for command termination) is generated.

At command issuance (I/O registers setting contents)								
$1F7_H$(CM)	0	0	1	1	1	1	0	0
$1F6_H$(DH)	×	L	×	DV	Start head No. /LBA [MSB]			
$1F5_H$(CH)	Start cylinder No. [MSB] / LBA							
$1F4_H$(CL)	Start cylinder No. [LSB] / LBA							
$1F3_H$(SN)	Start sector No. / LBA [LSB]							
$1F2_H$(SC)	Transfer sector count							
$1F1_H$(FR)	xx							

At command completion (I/O registers contents to be read)					
$1F7_H$(ST)	Status information				
$1F6_H$(DH)	×	L	×	DV	End head No. /LBA [MSB]
$1F5_H$(CH)	End cylinder No. [MSB] / LBA				
$1F4_H$(CL)	End cylinder No. [LSB] / LBA				
$1F3_H$(SN)	End sector No. / LBA [LSB]				
$1F2_H$(SC)	00 (*1)				
$1F1_H$(ER)	Error information				

*1 If the command is terminated due to an error, the remaining number of sectors of which data was not transferred is set in this register.

(9) RECALIBRATE (X'1x', x: X'0' to X'F')

This command performs the calibration. Upon receipt of this command, the device sets BSY bit of the Status register and performs a calibration. When the device completes the calibration, the device updates the Status register, clears the BSY bit, and generates an interrupt.

This command can be issued in the LBA mode.

At command issuance (I/O registers setting contents)								
$1F7_H$(CM)	0	0	0	1	x	x	x	x
$1F6_H$(DH)	×	×	×	DV	xx			
$1F5_H$(CH)	xx							
$1F4_H$(CL)	xx							
$1F3_H$(SN)	xx							
$1F2_H$(SC)	xx							
$1F1_H$(FR)	xx							

At command completion (I/O registers contents to be read)					
$1F7_H$(ST)	Status information				
$1F6_H$(DH)	×	×	×	DV	xx
$1F5_H$(CH)	xx				
$1F4_H$(CL)	xx				
$1F3_H$(SN)	xx				
$1F2_H$(SC)	xx				
$1F1_H$(ER)	Error information				

Note:

Also executable in LBA mode.

(10) SEEK (X'7x', x : X'0' to X'F')

This command performs a seek operation to the track and selects the head specified in the command block registers. After completing the seek operation, the device clears the BSY bit in the Status register and generates an interrupt.

The IDD always sets the DSC bit (Drive Seek Complete status) of the Status register to 1.

In the LBA mode, this command performs the seek operation to the cylinder and head position in which the sector is specified with the logical block address.

At command issuance (I/O registers setting contents)								
$1F7_H$(CM)	0	1	1	1	x	x	x	x
$1F6_H$(DH)	×	L	×	DV	Head No. /LBA [MSB]			
$1F5_H$(CH)	Cylinder No. [MSB] / LBA							
$1F4_H$(CL)	Cylinder No. [LSB] / LBA							
$1F3_H$(SN)	Sector No. / LBA [LSB]							
$1F2_H$(SC)	xx							
$1F1_H$(FR)	xx							

At command completion (I/O registers contents to be read)					
$1F7_H$(ST)	Status information				
$1F6_H$(DH)	×	L	×	DV	Head No. /LBA [MSB]
$1F5_H$(CH)	Cylinder No. [MSB] / LBA				
$1F4_H$(CL)	Cylinder No. [LSB] / LBA				
$1F3_H$(SN)	Sector No. / LBA [LSB]				
$1F2_H$(SC)	xx				
$1F1_H$(ER)	Error information				

(11) INITIALIZE DEVICE PARAMETERS (X'91')

The host system can set the number of sectors per track and the maximum head number (maximum head number is "number of heads minus 1") per cylinder with this command. Upon receipt of this command, the device sets the BSY bit of Status register and saves the parameters. Then the device clears the BSY bit and generates an interrupt.

When the SC register is specified to X'00', an ABORTED COMMAND error is posted. Other than X'00' is specified, this command terminates normally.

The parameters set by this command are retained even after reset or power save operation regardless of the setting of disabling the reverting to default setting.

In LBA mode

The device ignores the L bit specification and operates with the CHS mode specification. An accessible area of this command within head moving in the LBA mode is always within a default area. It is recommended that the host system refers the addressable user sectors (total number of sectors) in word 60 to 61 of the parameter information by the IDENTIFY DEVICE command.

At command issuance (I/O registers setting contents)								
$1F7_H$(CM)	1	0	0	1	0	0	0	1
$1F6_H$(DH)	×	×	×	DV	Max. head No.			
$1F5_H$(CH)	xx							
$1F4_H$(CL)	xx							
$1F3_H$(SN)	xx							
$1F2_H$(SC)	Number of sectors/track							
$1F1_H$(FR)	xx							

At command completion (I/O registers contents to be read)					
$1F7_H$(ST)	Status information				
$1F6_H$(DH)	×	×	×	DV	Max. head No.
$1F5_H$(CH)	xx				
$1F4_H$(CL)	xx				
$1F3_H$(SN)	xx				
$1F2_H$(SC)	Number of sectors/track				
$1F1_H$(ER)	Error infomation				

(12) IDENTIFY DEVICE (X'EC')

The host system issues the IDENTIFY DEVICE command to read parameter information (512 bytes) from the device. Upon receipt of this command, the drive sets the BSY bit of Status register and sets required parameter information in the sector buffer. The device then sets the DRQ bit of the Status register, and generates an interrupt. After that, the host system reads the information out of the sector buffer. Table 5.4 shows the arrangements and values of the parameter words and the meaning in the buffer.

At command issuance (I/O registers setting contents)								
$1F7_H$(CM)	1	1	1	0	1	1	0	0
$1F6_H$(DH)	×	×	×	DV	xx			
$1F5_H$(CH)	xx							
$1F4_H$(CL)	xx							
$1F3_H$(SN)	xx							
$1F2_H$(SC)	xx							
$1F1_H$(FR)	xx							

At command completion (I/O registers contents to be read)					
$1F7_H$(ST)	Status information				
$1F6_H$(DH)	×	×	×	DV	xx
$1F5_H$(CH)	xx				
$1F4_H$(CL)	xx				
$1F3_H$(SN)	xx				
$1F2_H$(SC)	xx				
$1F1_H$(ER)	Error information				

Table 5.4 Information to be read by IDENTIFY DEVICE command (1 of 3)

Word	Value	Description
0	X’0c5a’	General Configuration *1
1	X’18A0’ X’IF08’	Number of cylinders MHC2032AT: X’18A0’ MHC2040AT: X’IF08’ MHD2021AT: X’I068’ MHD2032AT: X’I8A0’
2	X’0000’	Reserved
3	X’0010’	Number of Heads
4	X’0000’	Undefined
5	X’0000’	Undefined
6	X’003F’	Number of sectors per track
7-9	X’000000000000’	Undefined
10-19	Set by a device	Serial number (ASCII code) *2

Word	Value	Description
20	X’0000’	Undefined
21	X’0000’	Undefined
22	X’0004’	Number of ECC bytes transferred at READ LONG or WRITE LONG command
23-26	–	Firmware revision (ASCII code) *3
27-46	–	Model name (ASCII code) *4
47	X’8010’	Maximum number of sectors per interrupt on READ/WRITE MULTIPLE command
48	X’0000’	Reserved
49	X’0B00’	Capabilities *5
50	X’0000’	Reserved
51	X’0200’	PIO data transfer mode *6
52	X’0000’	Reserved
53	X’0007’	Enable/disable setting of words 54-58 and 64-70, 88 *7
54	(Variable)	Number of current Cylinders
55	(Variable)	Number of current Head
56	(Variable)	Number of current sectors per track
57-58	(Variable)	Total number of current sectors
59	*8	Transfer sector count currently set by READ/WRITE MULTIPLE command *8
60-61	X’60F600’ X’7A2F80’	Total number of user addressable sectors (LBA mode only) MHC2032AT: X’60F600’ MHC2040AT: X’7A2F80’ MHD2021AT: X’409980’ MHD2032AT: X’60F600’
62	X’0000’	Reserved
63	X’xx07’	Multiword DMA transfer mode *9
64	X’0003’	Advance PIO transfer mode support status *10
65	X’0078’	Minimum multiword DMA transfer cycle time per word : 120 [ns]
66	X’0078’	Manufacturer’s recommended DMA transfer cycle time : 120 [ns]
67	X’00F0’	Minimum PIO transfer cycle time without IORDY flow control : 240 [ns]
68	X’0078’	Minimum PIO transfer cycle time with IORDY flow control : 120 [ns]

Word	Value	Description
69-79	X’00’	Reserved
80	X’000E’	Major version number *11
81	X’0000’	Minor version number (not reported)
82	X’000B’	Support of command sets *12
83	X’4000’	Support of command sets (fixed)
84-87	X’00’	Reserved
88	X’xx07’	Ultra DMA transfer mode
89-127	X’00’	Reserved
128	(Variable)	Security status *13
129-159	X’00’	Undefined
160-255	X’00’	Reserved

Table 5.4 Information to be read by IDENTIFY DEVICE command (2 of 3)

*1 Word 0: General configuration

Bit 15:	ATA device = 0, ATAPI device = 1	0
Bit 14-12:	Undefined	0
Bit 11:	Rotational speed tolerance is more than 0.5 %.	1
Bit 10:	Disk-data transfer rate 10 Mbps.	1
Bit 9:	Disk-data transfer rate is faster than 5 Mbps but 10 Mbps or slower	0
Bit 8:	Disk-data transfer rate is 5 Mbps or slower.	0
Bit 7:	Removable disk drive	0
Bit 6:	Fixed drive.	1
Bit 5:	Spindle motor control option implemented.	0
Bit 4:	Head switching time is more than 15 microseconds.	1
Bit 3:	Not MFM encoded.	1
Bit 2:	Soft sectored.	0
Bit 1:	Hard sectored.	1
Bit 0:	Reserved	0

*2 Word 10-19: Serial number; ASCII code (20 characters, right-justified)

*3 Word 23-26: Firmware revision; ASCII code (8 characters, Left-justified)

*4 Word 27-46: Model name;

ASCII code (40 characters, Left-justified), remainder filled with blank code (X'20')

One of two model names; MHC2032AT or MHC2040AT

*5 Word 49: Capabilities

Bit 15-14: Reserved

Bit 13: Standby timer value. Factory default is 0.

Bit 12: Reserved

Bit 11: IORDY support 1=Supported

Bit 10: IORDY inhibition 0=Disable inhibition

Bit 9-0: Undefined

Bit 9, 8: Always 1

Bit 7-0: Undefined

*6 Word 51: PIO data transfer mode

Bit 15-8: PIO data transfer mode X'02'=PIO mode 2

Bit 7-0: Undefined

*7 Word 53: Enable/disable setting of word 54-58 and 64-70

Bit 15-3: Reserved

Bit 2: Enable/disable setting of word 88 1=Enable

Bit 1: Enable/disable setting of word 64-70 1=Enable

Bit 0: Enable/disable setting of word 54-58 1=Enable

*8 Word 59: Transfer sector count currently set by READ/WRITE MULTIPLE command

Bit 15-9: Reserved

Bit 8: Multiple sector transfer 1=Enable

Bit 7-0: Transfer sector count currently set by READ/WRITE MULTIPLE command without interrupt supports 2, 4, 8 and 16 sectors.

Table 5.4 Information to be read by IDENTIFY DEVICE command (3 of 3)

*9 Word 63: Multiword DMA transfer mode

Bit 15-8: Currently used multiword DMA transfer mode

Bit 7-0: Supportable multiword DMA transfer mode

Bit 2=1 Mode 2

Bit 1=1 Mode 1

Bit 0=1 Mode 0

*10 Word 64: Advance PIO transfer mode support status

Bit 15-8: Reserved

Bit 7-0: Advance PIO transfer mode

Bit 1 = 1 Mode 4

Bit 0 = 1 Mode 3

*11 WORD 80

Bit 15-4: Reserved

Bit 3: ATA-3 supported = 1

Bit 2: ATA-2 supported = 1

Bit 1: ATA-1 supported = 1

Bit 0: Undefined

*12 WORD 82

Bit 15-4: Reserved

Bit 3: Power Management feature set supported = 1

Bit 2: Removable feature set supported = 0

Bit 1: Security feature set supported = 1

Bit 0: SMART feature set supported = 1

*13 WORD 88

Bit 15-8: Currently used Ultra DMA transfer mode

Bit 7-0: Supportable Ultra DMA transfer mode

Bit 2 = 1 Mode 2

Bit 1 = 1 Mode 1

Bit 0 = 1 Mode 0

*14 WORD 128

Bit 15-9: Reserved

Bit 8: Security level. 0: High, 1: Maximum

Bit 7-5: Reserved

Bit 4: 1: Security counter expired

Bit 3: 1: Security frozen

Bit 2: 1: Security locked

Bit 1: 1: Security enabled

Bit 0: 1: Security supported

(13) IDENTIFY DEVICE DMA (X'EE')

When this command is not used to transfer data to the host in DMA mode, this command functions in the same way as the Identify Device command.

At command issuance (I/O registers setting contents)								
$1F7_H$(CM)	1	1	1	0	1	1	1	0
$1F6_H$(DH)	×	×	×	DV	xx			
$1F5_H$(CH)	xx							
$1F4_H$(CL)	xx							
$1F3_H$(SN)	xx							
$1F2_H$(SC)	xx							
$1F1_H$(FR)	xx							

At command completion (I/O registers contents to be read)					
$1F7_H$(ST)	Status information				
$1F6_H$(DH)	×	×	×	DV	xx
$1F5_H$(CH)	xx				
$1F4_H$(CL)	xx				
$1F3_H$(SN)	xx				
$1F2_H$(SC)	xx				
$1F1_H$(ER)	Error information				

(14) SET FEATURES (X'EF')

The host system issues the SET FEATURES command to set parameters in the Features register for the purpose of changing the device features to be executed. For the transfer mode (Feature register = 03), detail setting can be done using the Sector Count register.

Upon receipt of this command, the device sets the BSY bit of the Status register and saves the parameters in the Features register. Then, the device clears the BSY bit, and generates an interrupt.

If the value in the Features register is not supported or it is invalid, the device posts an ABORTED COMMAND error.

Table 5.5 lists the available values and operational modes that may be set in the Features register.

Table 5.5 Features register values and settable modes

Features Register	Drive operation mode
X'02'	Enables the write cache function.
X'03'	Transfer mode depends on the contents of the Sector Count register. (Details are given later.)
X'55'	Disables read cache function.
X'66'	Disables the reverting to power-on default settings after software reset.
X'82'	Disables the write cache function.
X'AA'	Enables the read cache function.
X'BB'	Specifies the transfer of 4-byte ECC for READ LONG and WRITE LONG commands.
X'CC'	Enables the reverting to power-on default settings after software reset.

At power-on or after hardware reset, the default mode is the same as that is set with a value greater than X'AA' (except for write cache). If X'66' is specified, it allows the seting value greater than X'AA' which may have been modified to a new value since power-on, to remain the same even after software reset.

At command issuance (I/O registers setting contents)								
$1F7_H$(CM)	1	1	1	0	1	1	1	1
$1F6_H$(DH)	×	×	×	DV	xx			
$1F5_H$(CH)	xx							
$1F4_H$(CL)	xx							
$1F3_H$(SN)	xx							
$1F2_H$(SC)	xx or transfer mode							
$1F1_H$(FR)	[See Table 5.6]							

At command completion (I/O registers contents to be read)					
$1F7_H$(ST)	Status information				
$1F6_H$(DH)	×	×	×	DV	xx
$1F5_H$(CH)	xx				
$1F4_H$(CL)	xx				
$1F3_H$(SN)	xx				
$1F2_H$(SC)	xx				
$1F1_H$(ER)	Error information				

The host sets X'03' to the Features register. By issuing this command with setting a value to the Sector Count register, the transfer mode can be selected. Upper 5 bits of the Sector Count register defines the transfer type and lower 3 bits specifies the binary mode value.

The IDD supports following values in the Sector Count register value. If other value than below is specified, an ABORTED COMMAND error is posted.

PIO default transfer mode	00000 000 (X'00')
PIO flow control transfer mode X	00001 000 (X'08': Mode 0)
	00001 001 (X'09': Mode 1)
	00001 010 (X'0A': Mode 2)
	00001 011 (X'0B': Mode 3)
	00001 100 (X'0C': Mode 4)

Single word DMA transfer mode X	00010 000 (X'10': Mode 0)
	00010 001 (X'11': Mode 1)
	00010 010 (X'12': Mode 2)
Multiword DMA transfer mode X	00100 000 (X'20': Mode 0)
	00100 001 (X'21': Mode 1)
	00100 010 (X'22': Mode 2)
Ultra DMA transfer mode X	01000 000 (X'40': Mode 0)
	01000 001 (X'41': Mode 1)
	01000 010 (X'42': Mode 2)

(15) SET MULTIPLE MODE (X'C6')

This command enables the device to perform the READ MULTIPLE and WRITE MULTIPLE commands. The block count (number of sectors in a block) for these commands are also specified by the SET MULTIPLE MODE command.

The number of sectors per block is written into the Sector Count register. The IDD supprots 2, 4, 8, 16 and 32 (sectors) as the block counts.

Upon receipt of this command, the device sets the BSY bit of the Status register and checks the contents of the Sector Count register. If the contents of the Sector Count register is valid and is a supported block count, the value is stored for all subsequent READ MULTIPLE and WRITE MULTIPLE commands. Execution of these commands is then enabled. If the value of the Sector Count register is not a supported block count, an ABORTED COMMAND error is posted and the READ MULTIPLE and WRITE MULTIPLE commands are disabled.

If the contents of the Sector Count register is 0 when the SET MULTIPLE MODE command is issued, the READ MULTIPLE and WRITE MULTIPLE commands are disabled.

When the SET MULTIPLE MODE command operation is completed, the device clears the BSY bit and generates an interrupt.

At command issuance (I/O registers setting contents)								
$1F7_H$(CM)	1	1	0	0	0	1	1	0
$1F6_H$(DH)	×	×	×	DV	xx			
$1F5_H$(CH)	xx							
$1F4_H$(CL)	xx							
$1F3_H$(SN)	xx							
$1F2_H$(SC)	Sector count/block							
$1F1_H$(FR)	xx							

At command completion (I/O registers contents to be read)					
$1F7_H$(ST)	Status information				
$1F6_H$(DH)	×	×	×	DV	xx
$1F5_H$(CH)	xx				
$1F4_H$(CL)	xx				
$1F3_H$(SN)	xx				
$1F2_H$(SC)	Sector count/block				
$1F1_H$(ER)	Error information				

After power-on or after hardware reset, the READ MULTIPLE and WRITE MULTIPLE command operation are disabled as the default mode.

The mode established before software reset is retained if disable default (Features Reg. = 66h setting) has been defined by the SET FEATURES command. If disable default has not been defined after the software is the READ MULTIPLE and WRITE MULTIPLE commands are disabled.

The parameters for the multiple commands which are posted to the host system when the IDENTIFY DEVICE command is issued are listed below. See Subsection 5.32 for the IDENTIFY DEVICE command.

Word 47

Bit 7-0 = 10: Maximum number of sectors that can be transferred per interrupt by the READ MULTIPLE and WRITE MULTIPLE commands are 16 (fixed).

Word 59 = 0000: The READ MULTIPLE and WRITE MULTIPLE commands are disabled.

= 00xx: The READ MULTIPLE and WRITE MULTIPLE commands are enabled. "xx" indicates the current setting for number of sectors that can be transferred per interrupt by the READ MULTIPLE and WRITE MULTIPLE commands.

e.g. 0010 = Block count of 16 has been set by the SET MULTIPLE MODE command.

(16) EXECUTE DEVICE DIAGNOSTIC (X'90')

This command performs an internal diagnostic test (self-diagnosis) of the device. This command usually sets the DRV bit of the Drive/Head register is to 0 (however, the DV bit is not checked). If two devices are present, both devices execute self-diagnosis.

If device 1 is present:

- Both devices shall execute self-diagnosis.
- The device 0 waits for up to 5 seconds until device 1 asserts the PDIAG- signal.
- If the device 1 does not assert the PDIAG- signal but indicates an error, the device 0 shall append X'80' to its own diagnostic status.
- The device 0 clears the BSY bit of the Status register and generates an interrupt. (The device 1 does not generate an interrupt.)
- A diagnostic status of the device 0 is read by the host system. When a diagnostic failure of the device 1 is detected, the host system can read a status of the device 1 by setting the DV bit (selecting the device 1).

When device 1 is not present:

- The device 0 posts only the results of its own self-diagnosis.
- The device 0 clears the BSY bit of the Status register, and generates an interrupt.

Table 5.6 lists the diagnostic code written in the Error register which is 8-bit code.

If the device 1 fails the self-diagnosis, the device 0 "ORs" X'80' with its own status and sets that code to the Error register.

Table 5.6 Diagnostic code

Code	Result of diagnostic
X'01'	No error detected.
X'03'	Data buffer compare error
X'05'	ROM sum check error
X'8x'	Failure of device 1

attention: The device responds normally to this command without excuting internal diagnostic test.

At command issuance (I/O registers setting contents)								
$1F7_H$(CM)	1	0	0	1	0	0	0	0
$1F6_H$(DH)	×	×	×	DV	Head No. /LBA [MSB]			
$1F5_H$(CH)	xx							
$1F4_H$(CL)	xx							
$1F3_H$(SN)	xx							
$1F2_H$(SC)	xx							
$1F1_H$(FR)	xx							

At command completion (I/O registers contents to be read)					
$1F7_H$(ST)	Status information				
$1F6_H$(DH)	×	×	×	DV	Head No. /LBA [MSB]
$1F5_H$(CH)	xx				
$1F4_H$(CL)	xx				
$1F3_H$(SN)	01_H (*1)				
$1F2_H$(SC)	01_H				
$1F1_H$(ER)	Diagnostic code				

*1 This register indicates X'00' in the LBA mode.

(17) READ LONG (X'22' or X'23')

This command operates similarly to the READ SECTOR(S) command except that the device transfers the data in the requested sector and the ECC bytes to the host system. The ECC error correction is not performed for this command. This

command is used for checking ECC function by combining with the WRITE LONG command.

Number of ECC bytes to be transferred is fixed to 4 bytes and cannot be changed by the SET FEATURES command.

The READ LONG command supports only single sector operation.

At command issuance (I/O registers setting contents)								
$1F7_H$(CM)	0	0	1	0	0	0	1	R
$1F6_H$(DH)	×	L	×	DV	Head No. /LBA [MSB]			
$1F5_H$(CH)	Cylinder No. [MSB] / LBA							
$1F4_H$(CL)	Cylinder No. [LSB] / LBA							
$1F3_H$(SN)	Sector No. / LBA [LSB]							
$1F2_H$(SC)	01							
$1F1_H$(FR)	xx							

R = 0 →with Retry
R = 1 →without Retry

At command completion (I/O registers contents to be read)					
$1F7_H$(ST)	Status information				
$1F6_H$(DH)	×	L	×	DV	Head No. /LBA [MSB]
$1F5_H$(CH)	Cylinder No. [MSB] / LBA				
$1F4_H$(CL)	Cylinder No. [LSB] / LBA				
$1F3_H$(SN)	Sector No. / LBA [LSB]				
$1F2_H$(SC)	00 (*1)				
$1F1_H$(ER)	Error information				

*1 If the command is terminated due to an error, this register indicates 01.

(18) WRITE LONG (X'32' or X'33')

This command operates similarly to the READ SECTOR(S) command except that the device writes the data and the ECC bytes transferred from the host system to the disk medium. The device does not generate ECC bytes by itself. The WRITE LONG command supports only single sector operation.

The number of ECC bytes to be transferred is fixed to 4 bytes and can not be changed by the SET FEATURES command.

This command is operated under the following conditions:

- The command is issued in a sequence of the READ LONG or WRITE LONG (to the same address) command issuance. (WRITE LONG command can be continuously issued after the READ LONG command.)

If above condition is not satisfied, the command operation is not guaranteed.

At command issuance (I/O registers setting contents)								
$1F7_H$(CM)	0	0	1	1	0	0	1	R
$1F6_H$(DH)	×	L	×	DV	Head No. /LBA [MSB]			
$1F5_H$(CH)	Cylinder No. [MSB] / LBA							
$1F4_H$(CL)	Cylinder No. [LSB] / LBA							
$1F3_H$(SN)	Sector No. / LBA [LSB]							
$1F2_H$(SC)	01							
$1F1_H$(FR)	xx							

R = 0 →with Retry
R = 1 →without Retry

At command completion (I/O registers contents to be read)					
$1F7_H$(ST)	Status information				
$1F6_H$(DH)	×	L	×	DV	Head No. /LBA [MSB]
$1F5_H$(CH)	Cylinder No. [MSB] / LBA				
$1F4_H$(CL)	Cylinder No. [LSB] / LBA				
$1F3_H$(SN)	Sector No. / LBA [LSB]				
$1F2_H$(SC)	00 (*1)				
$1F1_H$(ER)	Error information				

*1 If the command is terminated due to an error, this register indicates 01.

(19) READ BUFFER (X'E4')

The host system can read the current contents of the sector buffer of the device by issuing this command. Upon receipt of this command, the device sets the BSY bit of Status register and sets up the sector buffer for a read operation. Then the device sets the DRQ bit of Status register, clears the BSY bit, and generates an interrupt. After that, the host system can read up to 512 bytes of data from the buffer.

At command issuance (I/O registers setting contents)								
$1F7_H$(CM)	1	1	1	1	0	1	0	0
$1F6_H$(DH)	×	×	×	DV	xx			
$1F5_H$(CH)	xx							
$1F4_H$(CL)	xx							
$1F3_H$(SN)	xx							
$1F2_H$(SC)	xx							
$1F1_H$(FR)	xx							

At command completion (I/O registers contents to be read)					
$1F7_H$(ST)	Status information				
$1F6_H$(DH)	×	×	×	DV	xx
$1F5_H$(CH)	xx				
$1F4_H$(CL)	xx				
$1F3_H$(SN)	xx				
$1F2_H$(SC)	xx				
$1F1_H$(ER)	Error information				

(20) WRITE BUFFER (X'E8')

The host system can overwrite the contents of the sector buffer of the device with a desired data pattern by issuing this command. Upon receipt of this command, the device sets the BSY bit of the Status register. Then the device sets the DRQ bit of Status register and clears the BSY bit when the device is ready to receive the data. After that, 512 bytes of data is transferred from the host and the device writes the data to the sector buffer, then generates an interrupt.

At command issuance (I/O registers setting contents)								
$1F7_H$(CM)	1	1	1	1	1	0	0	0
$1F6_H$(DH)	×	×	×	DV	xx			
$1F5_H$(CH)	xx							
$1F4_H$(CL)	xx							
$1F3_H$(SN)	xx							
$1F2_H$(SC)	xx							
$1F1_H$(FR)	xx							

At command completion (I/O registers contents to be read)					
$1F7_H$(ST)	Status information				
$1F6_H$(DH)	×	×	×	DV	xx
$1F5_H$(CH)	xx				
$1F4_H$(CL)	xx				
$1F3_H$(SN)	xx				
$1F2_H$(SC)	xx				
$1F1_H$(ER)	Error information				

(21) IDLE (X'97' or X'E3')

Upon receipt of this command, the device sets the BSY bit of the Status register, and enters the idle mode. Then, the device clears the BSY bit, and generates an interrupt. The device generates an interrupt even if the device has not fully entered the idle mode. If the spindle of the device is already rotating, the spin-up sequence shall not be implemented.

By using this command, the automatic power-down function is enabled and the timer immediately starts the countdown. When the timer reaches the specified value, the device enters standby mode.

Enabling the automatic power-down function means that the device automatically enters the standby mode after a certain period of time. When the device enters the idle mode, the timer starts countdown. If any command is not issued while the timer is counting down, the device automatically enters the standby mode. If any command is issued while the timer is counting down, the timer is initialized and the command is executed. The timer restarts countdown after completion of the command execution.

The period of timer count is set depending on the value of the Sector Count register as shown below.

Sector Count register value		Point of timer
0	[X'00']	30 minutes
1 to 3	[X'01' to X'03']	15 seconds
4 to 240	[X'04' to X'F0']	(Value ×5) seconds
241 to 251	[X'F1' to X'FB']	30 minutes
252	[X'FC']	21 minutes
253	[X'FD']	30 minutes
254 to 255	[X'FE' to X'FF']	21 minutes 15 seconds

attention: The automatic power-down is excuted if no command is coming for 30 min. (default)

At command issuance (I/O registers setting contents)						
$1F7_H$(CM)	X'97' or X'E3'					
$1F6_H$(DH)	×	×	×	DV	xx	
$1F5_H$(CH)	xx					
$1F4_H$(CL)	xx					
$1F3_H$(SN)	xx					
$1F2_H$(SC)	Period of timer					
$1F1_H$(FR)	xx					

At command completion (I/O registers contents to be read)						
$1F7_H$(ST)	Status information					
$1F6_H$(DH)	×	×	×	DV	xx	
$1F5_H$(CH)	xx					
$1F4_H$(CL)	xx					
$1F3_H$(SN)	xx					
$1F2_H$(SC)	xx					
$1F1_H$(ER)	Error information					

(22) IDLE IMMEDIATE (X'95' or X'E1')

Upon receipt of this command, the device sets the BSY bit of the Status register, and enters the idle mode. Then, the device clears the BSY bit, and generates an interrupt. This command does not support the automatic power-down function.

At command issuance (I/O registers setting contents)					
$1F7_H$(CM)	X'95' or X'E1'				
$1F6_H$(DH)	×	×	×	DV	xx
$1F5_H$(CH)	xx				
$1F4_H$(CL)	xx				
$1F3_H$(SN)	xx				
$1F2_H$(SC)	xx				
$1F1_H$(FR)	xx				

At command completion (I/O registers contents to be read)					
$1F7_H$(ST)	Status information				
$1F6_H$(DH)	×	×	×	DV	xx
$1F5_H$(CH)	xx				
$1F4_H$(CL)	xx				
$1F3_H$(SN)	xx				
$1F2_H$(SC)	xx				
$1F1_H$(ER)	Error information				

(23) STANDBY (X'96' or X'E2')

Upon receipt of this command, the device sets the BSY bit of the Status register and enters the standby mode. The device then clears the BSY bit and generates an interrupt. The device generates an interrupt even if the device has not fully entered the standby mode. If the device has already spun down, the spin-down sequence is not implemented.

By using this command, the automatic power-down function is enabled and the timer starts the countdown when the device returns to idle mode.

When the timer value reaches 0 (a specified time has padded), the device enters standby mode.

Under the standby mode, the spindle motor is stopped. Thus, when the command involving a seek such as the READ SECTOR(s) command is received, the device processes the command after driving the spindle motor.

attention: The automatic power-down is excuted if no command is coming for 30 min. (default)

At command issuance (I/O registers setting contents)						
$1F7_H$(CM)	X'96' or X'E2'					
$1F6_H$(DH)	×	×	×	DV	xx	
$1F5_H$(CH)	xx					
$1F4_H$(CL)	xx					
$1F3_H$(SN)	xx					
$1F2_H$(SC)	Period of timer					
$1F1_H$(FR)	xx					

At command completion (I/O registers contents to be read)						
$1F7_H$(ST)	Status information					
$1F6_H$(DH)	×	×	×	DV	xx	
$1F5_H$(CH)	xx					
$1F4_H$(CL)	xx					
$1F3_H$(SN)	xx					
$1F2_H$(SC)	xx					
$1F1_H$(ER)	Error information					

(24) STANDBY IMMEDIATE (X'94' or X'E0')

Upon receipt of this command, the device sets the BSY bit of the Status register and enters the standby mode. The device then clears the BSY bit and generates an interrupt. This command does not support the automatic power-down sequence.

At command issuance (I/O registers setting contents)						
$1F7_H$(CM)	X'94' or X'E0'					
$1F6_H$(DH)	×	×	×	DV	xx	
$1F5_H$(CH)	xx					
$1F4_H$(CL)	xx					
$1F3_H$(SN)	xx					
$1F2_H$(SC)	xx					
$1F1_H$(FR)	xx					

At command completion (I/O registers contents to be read)						
$1F7_H$(ST)	Status information					
$1F6_H$(DH)	×	×	×	DV	xx	
$1F5_H$(CH)	xx					
$1F4_H$(CL)	xx					
$1F3_H$(SN)	xx					
$1F2_H$(SC)	xx					
$1F1_H$(ER)	Error information					

(25) SLEEP (X'99' or X'E6')

This command is the only way to make the device enter the sleep mode.

Upon receipt of this command, the device sets the BSY bit of the Status register and enters the sleep mode. The device then clears the BSY bit and generates an interrupt. The device generates an interrupt even if the device has not fully entered the sleep mode.

In the sleep mode, the spindle motor is stopped and the ATA interface section is inactive. All I/O register outputs are in high-impedance state.

The only way to release the device from sleep mode is to execute a software or hardware reset.

At command issuance (I/O registers setting contents)						
$1F7_H$(CM)	X'99' or X'E6'					
$1F6_H$(DH)	×	×	×	DV	xx	
$1F5_H$(CH)	xx					
$1F4_H$(CL)	xx					
$1F3_H$(SN)	xx					
$1F2_H$(SC)	xx					
$1F1_H$(FR)	xx					

At command completion (I/O registers contents to be read)						
$1F7_H$(ST)	Status information					
$1F6_H$(DH)	×	×	×	DV	xx	
$1F5_H$(CH)	xx					
$1F4_H$(CL)	xx					
$1F3_H$(SN)	xx					
$1F2_H$(SC)	xx					
$1F1_H$(ER)	Error information					

(26) CHECK POWER MODE (X'98' or X'E5')

The host checks the power mode of the device with this command.

The host system can confirm the power save mode of the device by analyzing the contents of the Sector Count and Sector registers.

The device sets the BSY bit and sets the following register value. After that, the device clears the BSY bit and generates an interrupt.

Power save mode	Sector Count register
• During moving to standby mode • Standby mode • During returning from the standby mode	X'00'
• Idle mode	X'FF'
• Active mode	X'FF'

At command issuance (I/O registers setting contents)					
$1F7_H$(CM)	X'98' or X'E5'				
$1F6_H$(DH)	×	×	×	DV	xx
$1F5_H$(CH)	xx				
$1F4_H$(CL)	xx				
$1F3_H$(SN)	xx				
$1F2_H$(SC)	xx				
$1F1_H$(FR)	xx				

At command completion (I/O registers contents to be read)					
$1F7_H$(ST)	Status information				
$1F6_H$(DH)	×	×	×	DV	xx
$1F5_H$(CH)	xx				
$1F4_H$(CL)	xx				
$1F3_H$(SN)	xx				
$1F2_H$(SC)	X'00' ,X'80' or X'FF'				
$1F1_H$(ER)	Error information				

(27) SMART (X'B0)

This command performs operations for device failure predictions according to a subcommand specified in the FR register. If the value specified in the FR register is supported, the Aborted Command error is posted.

It is necessary for the host to set the keys (CL = 4Fh and CH = C2h) in the CL and CH registers prior to issuing this command. If the keys are set incorrectly, the Aborted Command error is posted.

In the default setting, the failure prediction feature is disabled. In this case, the Aborted Command error is posted in response to subcommands other than SMART Enable Operations (FR register = D8h).

When the failure prediction feature is enabled, the device collects or updates several items to forecast failures. In the following sections, note that the values of items collected or updated by the device to forecast failures are referred to as attribute values.

Table 5.7 Features Register values (subcommands) and functions

Features Resister	Function
X'D0'	SMART Read Attribute Values: A device that received this subcommand asserts the BSY bit and saves all the updated attribute values. The device then clears the BSY bit and transfers 512-byte attribute value information to the host. * For infomation about the format of the attribute value information, see Table 5.8.
X'D1'	SMART Read Attribute Thresholds: This subcommand is used to transfer 512-byte insurance failure threshold value data to the host. * For infomation about the format of the insurance failure threshold value data, see Table 5.9.
X'D2'	SMART Enable-Disable Attribute AutoSave: This subcommand is used to enable (SC register ≠ 00h) or disable (SC register = 00h) the setting of the automatic saving feature for the device attribute data. The setting is maintained every time the device is turned off and then on. When the automatic saving feature is enabled, the attribute values are saved before the device enters the power saving mode. However, if the failure prediction feature is disabled, the attribute values are not automatically saved. When the device receives this subcommand, it asserts the BSY bit, enables or disables the automatic saving feature, then clears the BSY bit.
X'D3'	SMART Save Attribute Values: When the device receives this subcommand, it asserts the BSY bit, saves device attribute value data, then clears the BSY bit.
X'D8'	SMART Enable Operations: This subcommand enables the failure prediction feature. The setting is maintained even when the device is turned off and then on. When the device receives this subcommand, it asserts the BSY bit, enables the failure prediction feature, then clears the BSY bit.
X'D9'	SMART Disable Operations: This subcommand disables the failure prediction feature. The setting is maintained even when the device is turned off and then on. When the device receives this subcommand, it asserts the BSY bit, disables the failure prediction feature, then clears the BSY bit.

Features Resister	Function
X'DA'	SMART Return Status: When the device receives this subcommand, it asserts the BSY bit and saves the current device attribute values. Then the device compares the device attribute values with insurance failure threshold values. If there is an attribute value exceeding the threshold, F4h and 2Ch are loaded into the CL and CH registers. If there are no attribute values exceeding the thresholds, 4Fh and C2h are loaded into the CL and CH registers. After the settings for the CL and CH registers have been determined, the device clears the BSY bit

The host must regularly issue the SMART Read Attribute Values subcommand (FR register = D0h), SMART Save Attribute Values subcommand (FR register = D3h), or SMART Return Status subcommand (FR register = DAh) to save the device attribute value data on a medium.

Alternative, the device must issue the SMART Enable-Disable Attribute AutoSave subcommand (FR register = D2h) to use a feature which regularly save the device attribute value data to a medium.

The host can predict failures in the device by periodically issuing the SMART Return Status subcommand (FR register = DAh) to reference the CL and CH registers.

If an attribute value is below the insurance failure threshold value, the device is about to fail or the device is nearing the end of its life . In this case, the host recommends that the user quickly backs up the data.

At command issuance (I-O registers setting contents)								
$1F7_H$(CM)	1	0	1	1	0	0	0	0
$1F6_H$(DH)	×	×	×	DV	xx			
$1F5_H$(CH)	Key (C2h)							
$1F4_H$(CL)	Key (4Fh)							
$1F3_H$(SN)	xx							
$1F2_H$(SC)	xx							
$1F1_H$(FR)	Subcommand							

At command completion (I-O registers setting contents)						
$1F7_H$(ST)	Status information					
$1F6_H$(DH)	×	×	×	DV	xx	
$1F5_H$(CH)	Key-failure prediction status (C2h-2Ch)					
$1F4_H$(CL)	Key-failure prediction status (4Fh-F4h)					
$1F3_H$(SN)	xx					
$1F2_H$(SC)	xx					
$1F1_H$(ER)	Error information					

The attribute value information is 512-byte data; the format of this data is shown below. The host can access this data using the SMART Read Attribute Values subcommand (FR register = D0h). The insurance failure threshold value data is 512-byte data; the format of this data is shown below. The host can access this data using the SMART Read Attribute Thresholds subcommand (FR register = D1h).

Table 5.8 Format of device attribute value data

Byte	Item	
00 01	Data format version number	
02	Attribute 1	Attribute ID
03 04		Status flag
05		Current attribute value
06		Attribute value for worst case so far
07 to 0C		Raw attribute value
0D		Reserved
0E to 169	Attribute 2 to attribute 30	(The format of each attribute value is the same as that of bytes 02 to 0D.)
16A	Off-line data collection	Off-line data collection status
16B		Number of off-line data collection segments
16C, 16D		Time required for next segments [sec].
16E		Current segment pointer
16F		Off-line data collection capability
170 171	Failure prediction capability flag	
172 to 181	Reserved	
182 to 1FE	Vendor unique	
1FF	Check sum	

Table 5.9 Format of insurance failure threshold value data

Byte	Item	
00 01	Data format version number	
02	Attribute 1	Attribute ID
03		Insurance failure threshold
04 to 0D	Threshold 1 (Threshold of attribute 1)	Reserved
0E to 169	Threshold 2 to threshold 30	(The format of each threshold value is the same as that of bytes 02 to 0D.)
16A to 17B	Reserved	
17C to 1FE	Unique to vendor	
1FF	Check sum	

- Data format version number

  The data format version number indicates the version number of the data format of the device attribute values or insurance failure thresholds. The data format version numbers of the device attribute values and insurance failure thresholds are the same. When a data format is changed, the data format version numbers are updated.

- Attribute ID

  The attribute ID is defined as follows:

Attribute ID	Attribute name
0	(Indicates unused attribute data.)
1	Read error rate
2	Throughput performance
3	Spin up time
4	Start/stop count
5	Re-allocated sector count
7	Seek error rate
8	Seek time performance
9	Power-on time
10	Number of retries made to activate the spindle motor

Attribute ID	Attribute name
12	Number of power-on-power-off times
13 to 198	(Reserved)
199	Ultra ATA CRC error rate
200	Write error rate
201 to 255	(Unique to vendor)

- Status Flag

Bit	Meaning
0	If this bit 1, it indicates that if the attribute exceeds the threshold, it is the attribute covered by the drive warranty.
1	If this bit is 1 (0), it indicates the attribute only updated by an on-line test (off-line test).
2	If this bit 1, it indicates the attribute that represents performance.
3	If this bit 1, it indicates the attribute that represents an error rate.
4	If this bit 1, it indicates the attribute that represents the number of occurrences.
5	If this bit 1, it indicates the attribute that can be collected/saved even if the drive fault prediction function is disabled.
6 to 15	Reserve bit

- Current attribute value

  The current attribute value is the normalized raw attribute data. The value varies between 01h and 64h. The closer the value gets to 01h, the higher the possibility of a failure. The device compares the attribute values with thresholds. When the attribute values are larger than the thresholds, the device is operating normally.

- Attribute value for the worst case so far

  This is the worst attribute value among the attribute values collected to date. This value indicates the state nearest to a failure so far.

- Raw attribute value

  Raw attributes data is retained.

- Off-line data collection status

  Bits 0 to 6: Indicates the situation of off-line data collection according to the table below.

Bit 7: If this bit is 1, it indicates that the automatic off-line data collection function is enabled.

Status Byte	Meaning
0	Off-line data collection is not started.
2	Off-line data collection has been completed normally.
3	Off-line data collection is in progress.
4	Off-line data collection has been suspended by a command interrupt.
5	Off-line data collection has been aborted by a command interrupt.
6	Off-line data collection has been aborted by a fatal error.

- Number of off-line data collection segments

  Indicates the number of segments required to terminate off-line data collection.

- Time required for next segment [sec]

  Indicates the time required to terminate the next segment.

- Current segment pointer

  Indicates the number of the next segment to be executed.

- Off-line data collection capability

  Indicates the method of off-line data collection carried out by the drive. If the off-line data collection capability is 0, it indicates that off-line data collection is not supported.

Bit	Meaning
0	Indicates that Execute Off-Line Immediate is supported.
1	Vendor unique
2	Indicates that off-line data collection being executed is aborted when a new command is received.

- Failure prediction capability flag

  Bit 0: The attribute value data is saved to a media before the device enters power saving mode.

  Bit 1: The device automatically saves the attribute value data to a media after the previously set operation.

  Bits 2 to 15: Reserved bits

- Check sum

  Two's complement of the lower byte, obtained by adding 511-byte data one byte at a time from the beginning.

- Insurance failure threshold

  The limit of a varying attribute value. The host compares the attribute values with the thresholds to identify a failure.

(28) SECURITY DISABLE PASSWORD (F6h)

This command invalidates the user password already set and releases the lock function.

The host transfers the 512-byte data shown in Table 5.10 to the device. The device compares the user password or master password in the transferred data with the user password or master password already set, and releases the lock function if the passwords are the same.

Although this command invalidates the user password, the master password is retained. To recover the master password, issue the SECURITY SET PASSWORD command and reset the user password.

If the user password or master password transferred from the host does not match, the Aborted Command error is returned.

Issuing this command while in LOCKED MODE or FROZEN MODE returns the Aborted Command error.

(The section about the SECURITY FREEZE LOCK command describes LOCKED MODE and FROZEN MODE.)

Table 5.10 Contents of security password

Word	Contents
0	Control word Bit 0: Identifier 0 = Compares the user passwords. 1 = Compares the master passwords. Bits 1 to 15: Reserved
1 to 16	Password (32 bytes)
17 to 255	Reserved

At command issuance (I-O register contents))								
$1F7_h$(CM)	1	1	1	1	0	1	1	0
$1F6_h$(DH)	×	×	×	DV	xx			
$1F5_h$(CH)	xx							
$1F4_h$(CL)	xx							
$1F3_h$(SN)	xx							
$1F2_h$(SC)	xx							
$1F1_h$(FR)	xx							

At command completion (I-O register contents)					
$1F7_h$(ST)	Status information				
$1F6_h$(DH)	×	×	×	DV	xx
$1F5_h$(CH)	xx				
$1F4_h$(CL)	xx				
$1F3_h$(SN)	xx				
$1F2_h$(SC)	xx				
$1F1_h$(ER)	Error information				

(29) SECURITY ERASE PREPARE (F3h)

The SECURITY ERASE UNIT command feature is enabled by issuing the SECURITY ERASE PREPARE command and then the SECURITY ERASE UNIT command. The SECURITY ERASE PREPARE command prevents data from being erased unnecessarily by the SECURITY ERASE UNIT command.

Issuing this command during FROZEN MODE returns the Aborted Command error.

At command issuance (I-O register contents)								
$1F7_h$(CM)	1	1	1	1	0	0	1	1
$1F6_h$(DH)	×	×	×	DV	xx			
$1F5_h$(CH)	xx							
$1F4_h$(CL)	xx							
$1F3_h$(SN)	xx							
$1F2_h$(SC)	xx							
$1F1_h$(FR)	xx							

At command completion (I-O register contents)					
$1F7_h$(ST)	Status information				
$1F6_h$(DH)	×	×	×	DV	xx
$1F5_h$(CH)	xx				
$1F4_h$(CL)	xx				
$1F3_h$(SN)	xx				
$1F2_h$(SC)	xx				
$1F1_h$(ER)	Error information				

(30) SECURITY ERASE UNIT (F4h)

This command erases all user data. This command also invalidates the user password and releases the lock function.

The host transfers the 512-byte data shown in Table 5.10 to the device. The device compares the user password or master password in the transferred data with the user password or master password already set. The device erases user data, invalidates the user password, and releases the lock function if the passwords are the same.

Although this command invalidates the user password, the master password is retained. To recover the master password, issue the SECURITY SET PASSWORD command and reset the user password.

If the SECURITY ERASE PREPARE command is not issued immediately before this command is issued, the Aborted Command error is returned.

Issuing this command while in FROZEN MODE returns the Aborted Command error.

At command issuance (I-O register contents)								
$1F7_h$(CM)	1	1	1	1	0	1	0	0
$1F6_h$(DH)	×	×	×	DV	xx			
$1F5_h$(CH)	xx							
$1F4_h$(CL)	xx							
$1F3_h$(SN)	xx							
$1F2_h$(SC)	xx							
$1F1_h$(FR)	xx							

At command completion (I-O register contents)					
$1F7_h$(ST)	Status information				
$1F6_h$(DH)	×	×	×	DV	xx
$1F5_h$(CH)	xx				
$1F4_h$(CL)	xx				
$1F3_h$(SN)	xx				
$1F2_h$(SC)	xx				
$1F1_h$(ER)	Error information				

(31) SECURITY FREEZE LOCK (F5h)

This command puts the device into FROZEN MODE. The following commands used to change the lock function return the Aborted Command error if the device is in FROZEN MODE.

- SECURITY SET PASSWORD
- SECURITY UNLOCK
- SECURITY DISABLE PASSWORD
- SECURITY ERASE UNIT

FROZEN MODE is canceled when the power is turned off. If this command is reissued in FROZEN MODE, the command is completed and FROZEN MODE remains unchanged.

Issuing this command during LOCKED MODE returns the Aborted Command error.

The following medium access commands return the Aborted Command error when the device is in LOCKED MODE:

- READ DMA
- READ LONG
- READ MULTIPLE
- READ SECTORS
- WRITE DMA
- WRITE LONG
- WRITE MULTIPLE
- WRITE SECTORS
- WRITE VERIFY
- SECURITY DISABLE PASSWORD
- SECURITY FREEZE LOCK
- SECURITY SET PASSWORD

At command issuance (I-O register contents)								
$1F7_h$(CM)	1	1	1	1	0	1	0	1
$1F6_h$(DH)	×	×	×	DV	xx			
$1F5_h$(CH)	xx							
$1F4_h$(CL)	xx							
$1F3_h$(SN)	xx							
$1F2_h$(SC)	xx							
$1F1_h$(FR)	xx							

At command completion (I-O register contents)					
$1F7_h$(ST)	Status information				
$1F6_h$(DH)	×	×	×	DV	xx
$1F5_h$(CH)	xx				
$1F4_h$(CL)	xx				
$1F3_h$(SN)	xx				
$1F2_h$(SC)	xx				
$1F1_h$(ER)	Error information				

(32) SECURITY SET PASSWORD (F1h)

This command enables a user password or master password to be set.

The host transfers the 512-byte data shown in Table 1.2 to the device. The device determines the operation of the lock function according to the specifications of the Identifier bit and Security level bit in the transferred data. (Table 1.3)

Issuing this command in LOCKED MODE or FROZEN MODE returns the Aborted Command error.

Table 5.11 Contents of SECURITY SET PASSWORD data

Word	Contents
0	Control word Bit 0 Identifier 0 = Sets a user password. 1 = Sets a master password. Bits 1 to 7 Reserved Bit 8 Security level 0 = High 1 = Maximum Bits 9 to 15 Reserved
1 to 16	Password (32 bytes)
17 to 255	Reserved

Table 5.12 Relationship between combination of Identifier and Security level, and operation of the lock function

Indentifier	Level	Description
User	High	The specified password is saved as a new user password. The lock function is enabled after the device is turned off and then on. LOCKED MODE can be canceled using the user password or the master password already set.
Master	High	The specified password is saved as a new master password. The lock function is not enabled.
User	Maximum	The specified password is saved as a new user password. The lock function is enabled after the device is turned off and then on. LOCKED MODE can be canceled using the user password only. The master password already set cannot cancel LOCKED MODE.
Master	Maximum	The specified password is saved as a new master password. The lock function is not enabled.

(33) SECURITY UNLOCK

This command cancels LOCKED MODE.

The host transfers the 512-byte data shown in Table 1.1 to the device. Operation of the device varies as follows depending on whether the host specifies the master password.

- When the master password is selected

  When the security level is LOCKED MODE is high, the password is compared with the master password already set. If the passwords are the same, LOCKED MODE is conceled. Otherwise, the Aborted Command error is returned. If the security level in LOCKED MODE is set to the highest level, the Aborted Command error is always returned.

- When the user password is selected

  The password is compared with the user password already set. If the passwords are the same, LOCKED MODE is conceled. Otherwise, the Aborted Command error is returned.

If the password comparison fails, the device decrements the UNLOCK counter. The UNLOCK counter initially has a value of five. When the value of the UNLOCK counter reaches zero, this command or the SECURITY ERASE UNIT command causes the Aborted Command error until te device is turned off and then on, or until a hardware reset is executed. Issuing this command with LOCKED MODE conceled (in UNLOCK MODE) has no affect on the UNLOCK counter.

Issuing this command in FROZEN MODE returns the Aborted Command error.

At command issuance (I-O register contents)								
$1F7_h$(CM)	1	1	1	1	0	0	0	1
$1F6_h$(DH)	×	×	×	DV	xx			
$1F5_h$(CH)	xx							
$1F4_h$(CL)	xx							
$1F3_h$(SN)	xx							
$1F2_h$(SC)	xx							
$1F1_h$(FR)	xx							

At command completion (I-O register contents)					
$1F7_h$(ST)	Status information				
$1F6_h$(DH)	×	×	×	DV	xx
$1F5_h$(CH)	xx				
$1F4_h$(CL)	xx				
$1F3_h$(SN)	xx				
$1F2_h$(SC)	xx				
$1F1_h$(ER)	Error information				

(34) FLUSH CACHE (E7)

This command is used to order to write every write cache data stored by the device into the medium. BSY bit is held at "1" until every data has been written normally or a error has occurred. The device performs every error recovery so that the data are read correctly.

When executing this command, the reading of the data may take several seconds if much data are to be read.

Complete execution of this command may take 30 seconds or over.

In case a non-recoverable error has occurred while the data is being read, the error generation address is put into the command block register before ending the command. This error sector is deleted from the write cache data, and the remaining cache data is written into the medium by the execution of the next Flush Cache command.

At command issuance (I-O register contents)								
$1F7_h$(CM)	1	1	1	0	0	1	1	1
$1F6_h$(DH)	×	×	×	DV	xx			
$1F5_h$(CH)	xx							
$1F4_h$(CL)	xx							
$1F3_h$(SN)	xx							
$1F2_h$(SC)	xx							
$1F1_h$(FR)	xx							

At command completion (I-O register contents to be read)					
$1F7_h$(ST)	Status information				
$1F6_h$(DH)	×	×	×	DV	xx
$1F5_h$(CH)	xx				
$1F4_h$(CL)	xx				
$1F3_h$(SN)	xx				
$1F2_h$(SC)	xx				
$1F1_h$(ER)	Error information				

5.3.3 Error posting

Table 5.7 lists the defined errors that are valid for each command.

Table 5.13 Command code and parameters (1 of 2)

Command name	Error register (X'1F1')					Status register (X'1F7')		
	BBK	UNC	INDF	ABRT	TK0NF	DRDY	DWF	ERR
READ SECTOR(S)	V	V	V	V		V	V	V
WRITE SECTOR(S)	V		V	V		V	V	V
READ MULTIPLE	V	V	V	V		V	V	V
WRITE MULTIPLE	V		V	V		V	V	V
READ DMA	V	V	V	V		V	V	V
WRITE DMA	V		V	V		V	V	V

V: Valid on this command

*: See the command descriptioms.

Table 5.13 Command code and parameters (2 of 2)

Command name	Error register (X'1F1')					Status register (X'1F7')		
	BBK	UNC	INDF	ABRT	TK0NF	DRDY	DWF	ERR
WRITE VERIFY	V	V	V	V		V	V	V
READ VERIFY SECTOR(S)	V	V	V	V		V	V	V
RECALIBRATE				V	V	V	V	V
SEEK			V	V		V	V	V
INITIALIZE DEVICE PARAMETERS				V		V	V	V
IDENTIFY DEVICE				V		V	V	V
IDENTIFY DEVICE DMA				V		V	V	V
SET FEATURES				V		V	V	V
SET MULTIPLE MODE				V		V	V	V
EXECUTE DEVICE DIAGNOSTIC	*	*	*	*	*			V
READ LONG	V		V	V		V	V	V
WRITE LONG	V		V	V		V	V	V
READ BUFFER				V		V	V	V
WRITE BUFFER				V		V	V	V
IDLE				V		V	V	V
IDLE IMMEDIATE				V		V	V	V
STANDBY				V		V	V	V
STANDBY IMMEDIATE				V		V	V	V
SLEEP				V		V	V	V
CHECK POWER MODE				V		V	V	V
SMART			V	V		V	V	V
SECURITY DISABLE PASSWORD				V		V	V	V
SECURITY ERASE PREPARE				V		V	V	V
SECURITY ERASE UNIT				V		V	V	V
SECURITY FREEZE LOCK				V		V	V	V
SECURITY SET PASSWORD				V		V	V	V
FLUSH CACHE			V	V		V	V	V
Invalid command				V		V	V	V

V: Valid on this command

*: See the command descriptioms.

5.4 Command Protocol

The host should confirm that the BSY bit of the Status register of the device is 0 prior to issue a command. If BSY bit is 1, the host should wait for issuing a command until BSY bit is cleared to 0.

Commands can be executed only when the DRDY bit of the Status register is 1. However, the following commands can be executed even if DRDY bit is 0.

- EXECUTE DEVICE DIAGNOSTIC
- INITIALIZE DEVICE PARAMETERS

5.4.1 Data transferring commands from device to host

The execution of the following commands involves data transfer from the device to the host.

- IDENTIFY DEVICE.
- IDENTIFY DEVICE DMA
- READ SECTOR(S)
- READ LONG
- READ BUFFER
- SMART

The execution of these commands includes the transfer one or more sectors of data from the device to the host. In the READ LONG command, 516 bytes are transferred. Following shows the protocol outline.

a) The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder, and Device/Head registers.

b) The host writes a command code to the Command register.

c) The device sets the BSY bit of the Status register and prepares for data transfer.

d) When one sector of data is available for transfer to the host, the device sets DRQ bit and clears BSY bit. The drive then asserts INTRQ signal.

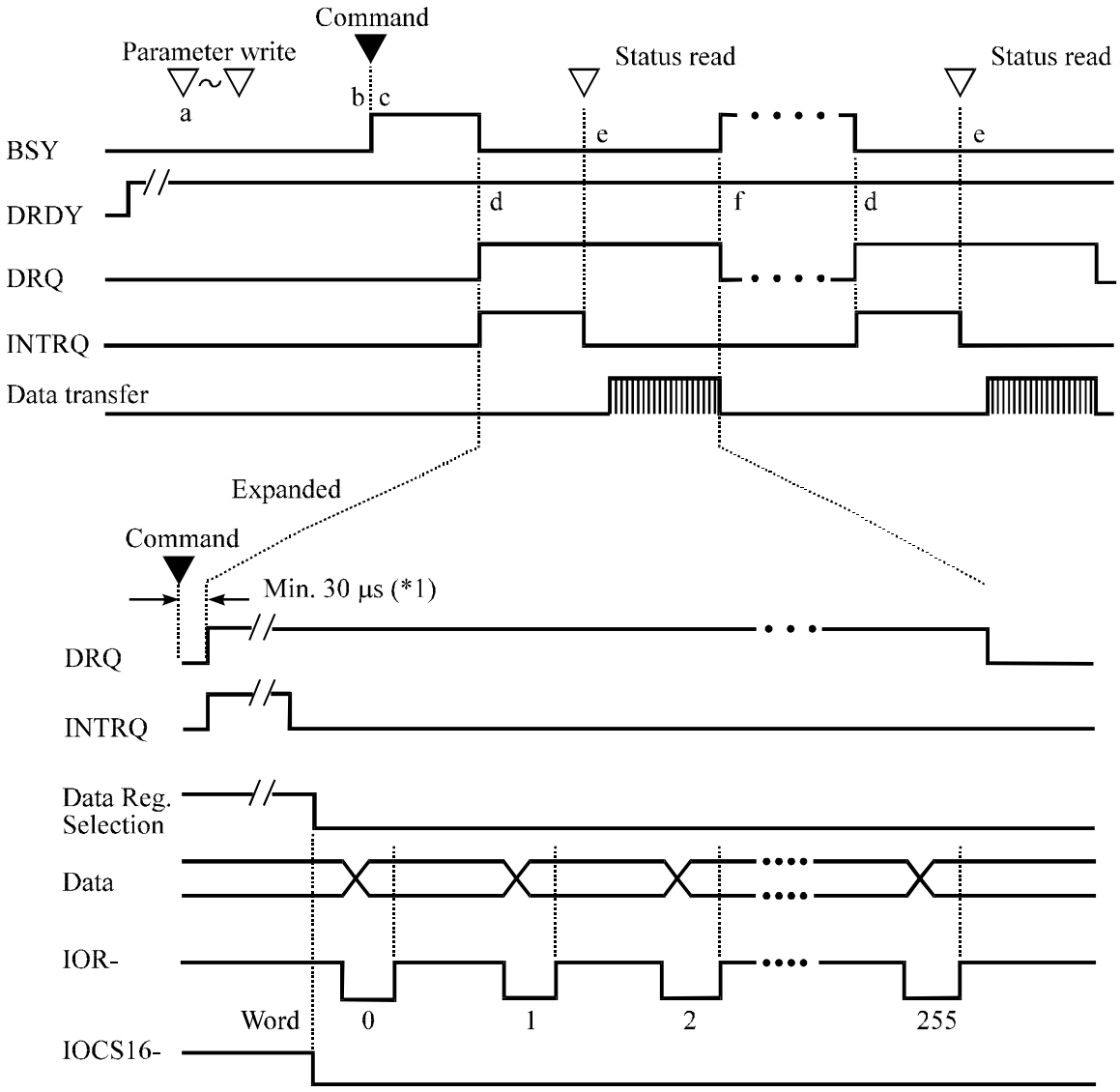
e) After detecting the INTRQ signal assertion, the host reads the Status register. The host reads one sector of data via the Data register. In response to the Status register being read, the device negates the INTRQ signal.

f) The drive clears DRQ bit to 0. If transfer of another sector is requested, the device sets the BSY bit and steps d) and after are repeated.

Even if an error is encountered, the device prepares for data transfer by setting the DRQ bit. Whether or not to transfer the data is determined for each host. In other

words, the host should receive the relevant sector of data (512 bytes of uninsured dummy data) or release the DRQ status by resetting.

Figure 5.3 shows an example of READ SECTOR(S) command protocol, and Figure 5.4 shows an example protocol for command abort.



*1 When the IDD receives a command that hits the cache data during read-ahead, and transfers data from the buffer without reading from the disk medium.

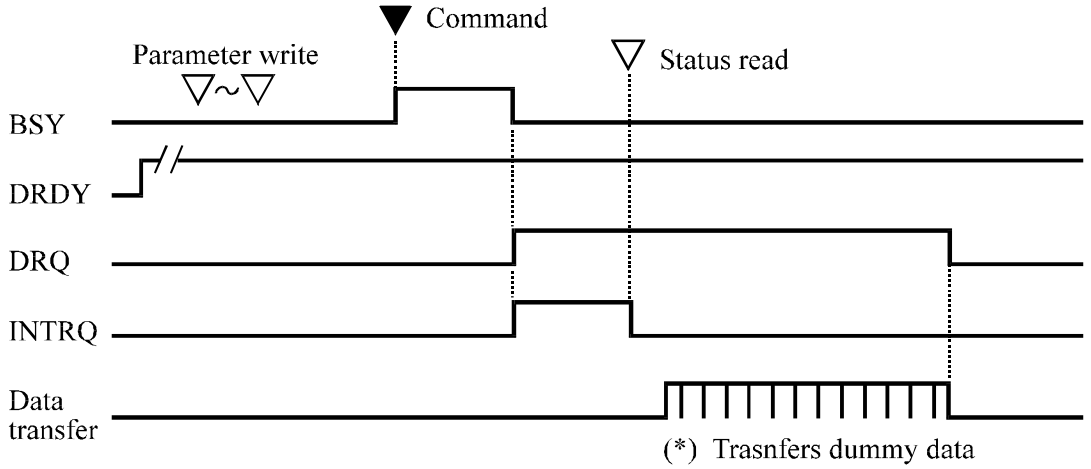
Figure 5.3 Read Sector(s) command protocol

Note:

For transfer of a sector of data, the host needs to read Status register (X'1F7') in order to clear INTRQ (interrupt) signal. The Status register should be read within a period from the DRQ setting by the device to 50 ms after the completion of the sector data transfer. Note that the host does not need to read the Status register for the reading of a single sector or the last

sector in multiple-sector reading. If the timing to read the Status register does not meet above condition, normal data transfer operation is not guaranteed.

When the host new command even if the device requests the data transfer (setting in DRQ bit), the correct device operation is not guaranteed.



*: The host should receive 512-byte dummy data or release the DRQ set state by resetting.

Figure 5.4 Protocol for command abort

5.4.2 Data transferring commands from host to device

The execution of the following commands involves Data transfer from the host to the drive.

- WRITE SECTOR(S)
- WRITE LONG
- WRITE BUFFER
- WRITE VERIFY
- SECURITY DISABLE PASSWORD
- SECURITY ERASE UNIT
- SECURITY SET PASSWORD
- SECURITY UNCLOK

The execution of these commands includes the transfer one or more sectors of data from the host to the device. In the WRITE LONG command, 516 bytes are transferred. Following shows the protocol outline.

a) The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder, and Device/Head registers.

b) The host writes a command code in the Command register. The drive sets the BSY bit of the Status register.

c) When the device is ready to receive the data of the first sector, the device sets DRQ bit and clears BSY bit.

d) The host writes one sector of data through the Data register.

e) The device clears the DRQ bit and sets the BSY bit.

f) When the drive completes transferring the data of the sector, the device clears BSY bit and asserts INTRQ signal. If transfer of another sector is requested, the drive sets the DRQ bit.

g) After detecting the INTRQ signal assertion, the host reads the Status register.

h) The device resets INTRQ (the interrupt signal).

I) If transfer of another sector is requested, steps d) and after are repeated.

Figure 5.5 shows an example of WRITE SECTOR(S) command protocol.

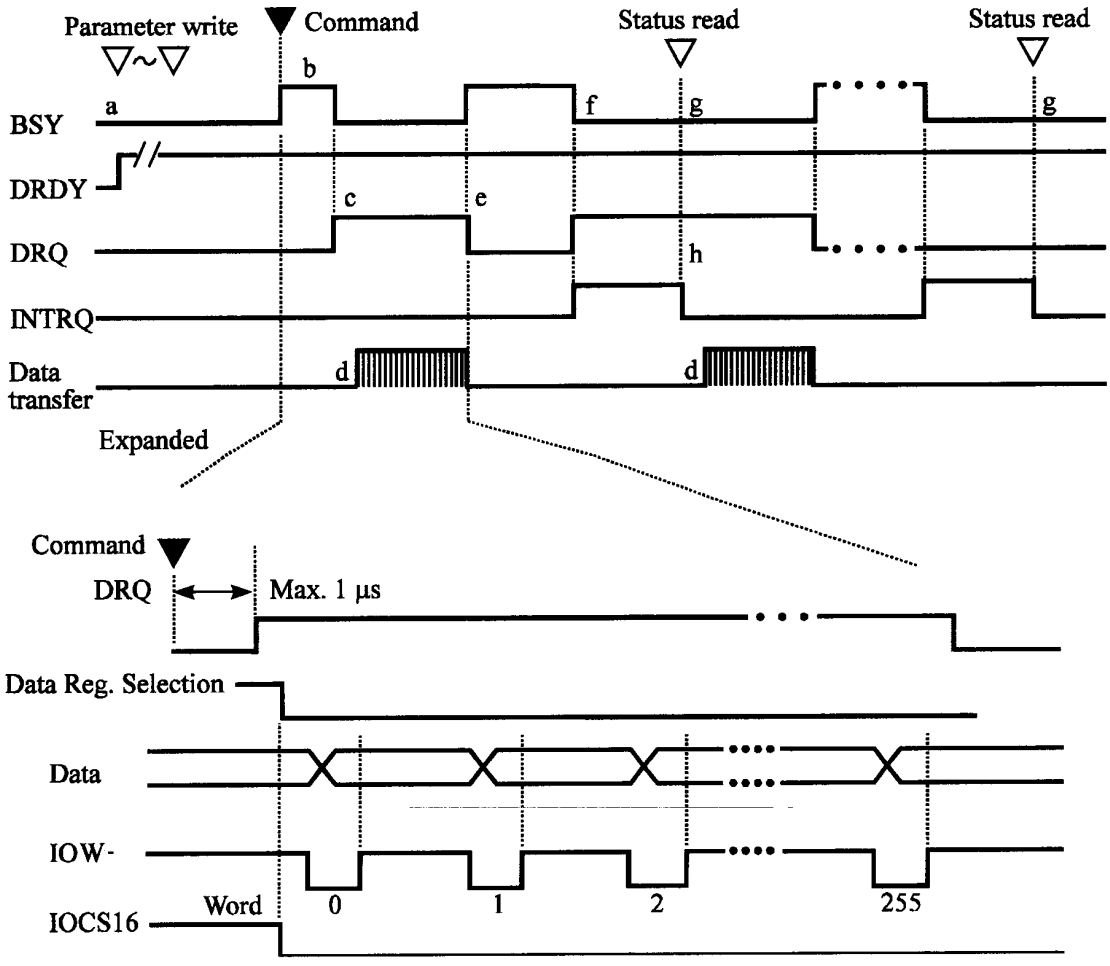


Figure 5.5 WRITE SECTOR(S) command protocol

Note:

For transfer of a sector of data, the host needs to read Status register (X'1F7') in order to clear INTRQ (interrupt) signal. The Status register should be read within a period from the DRQ setting by the device to 50 μs after the completion of the sector data transfer. Note that the host does not need to read the Status register for the first and the last sector to be transferred. If the timing to read the Status register does not meet above condition, normal data transfer operation is not assured guaranteed.

When the host issues the command even if the drive requests the data transfer (DRQ bit is set), or when the host executes resetting, the device correct operation is not guaranteed.

5.4.3 Commands without data transfer

Execution of the following commands does not involve data transfer between the host and the device.

- RECABLIBRATE
- SEEK
- READY VERIFY SECTOR(S)
- EXECUTE DEVICE DIAGNOSTIC
- INITIALIZE DEVICE PARAMETERS
- SET FEATURES
- SET MULTIPLE MODE
- IDLE
- IDLE IMMEDIATE
- STANDBY
- STANDBY IMMEDIATE
- CHECK POWER MODE
- SECURITY ERASE PREPARE
- SECURITY FREEZE LOCK
- FLUSH CACHE

Figure 5.6 shows the protocol for the command execution without data transfer.

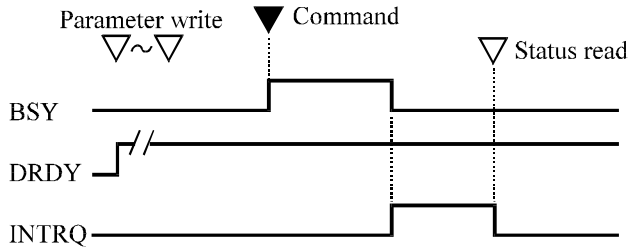


Figure 5.6 Protocol for the command execution without data transfer

5.4.4 Other commands

- READ MULTIPLE
- SLEEP
- WRITE MULTIPLE

See the description of each command.

5.4.5 DMA data transfer commands

- READ DMA
- WRITE DMA

Starting the DMA transfer command is the same as the READ SECTOR(S) or WRITE SECTOR(S) command except the point that the host initializes the DMA channel preceding the command issurance.

Interruption processing for DMA transfer does not issue interruptions in any intermediate sector when a multisector command is executed.

The following outlines the protocol:

The interrupt processing for the DMA transfer differs the following point.

- The interrupt processing for the DMA transfer differs the following point.

a) The host writes any parameters to the Features, Sector Count, Sector Number, Cylinder, and Device/Head register.

b) The host initializes the DMA channel

c) The host writes a command code in the Command register.

d) The device sets the BSY bit of the Status register.

e) The device asserts the DMARQ signal after completing the preparation of data transfer. The device asserts either the BSY bit or DRQ bit during DMA data transfer.

f) When the command execution is completed, the device clears both BSY and DRQ bits and asserts the INTRQ signal. Then, the host reads the Status register.

g) The host resets the DMA channel.

Figure 5.7 shows the correct DMA data transfer protocol.

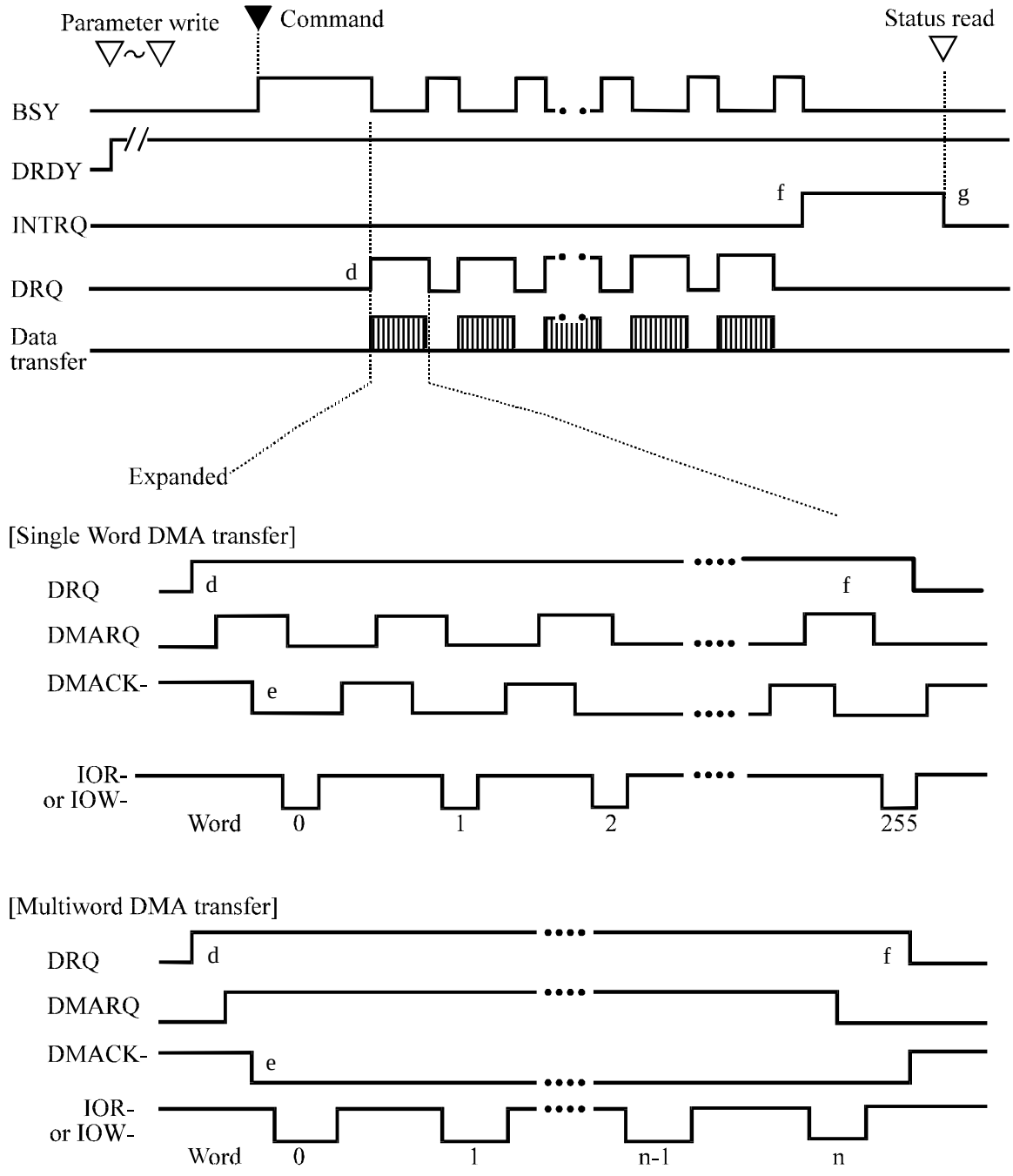


Figure 5.7 Normal DMA data transfer

5.5 Ultra DMA Feature Set

5.5.1 Overview

Ultra DMA is a data transfer protocol used with the READ DMA and WRITE DMA commands. When this protocol is enabled it shall be used instead of the Multiword DMA protocol when these commands are issued by the host. This protocol applies to the Ultra DMA data burst only. When this protocol is used there are no changes to other elements of the ATA protocol (e.g.: Command Block Register access).

Several signal lines are redefined to provide new functions during an Ultra DMA burst. These lines assume these definitions when 1) an Ultra DMA Mode is selected, and 2) a host issues a READ DMA or a WRITE DMA, command requiring data transfer, and 3) the host asserts DMACK-. These signal lines revert back to the definitions used for non-Ultra DMA transfers upon the negation of DMACK- by the host at the termination of an Ultra DMA burst. All of the control signals are unidirectional. DMARQ and DMACK- retain their standard definitions.

With the Ultra DMA protocol, the control signal (STROBE) that latches data from DD (15:0) is generated by the same agent (either host or device) that drives the data onto the bus. Ownership of DD (15:0) and this data strobe signal are given either to the device during an Ultra DMA data in burst or to the host for an Ultra DMA data out burst.

During an Ultra DMA burst a sender shall always drive data onto the bus, and after a sufficient time to allow for propagation delay, cable settling, and setup time, the sender shall generate a STROBE edge to latch the data. Both edges of STROBE are used for data transfers so that the frequency of STROBE is limited to the same frequency as the data. The highest fundamental frequency on the cable shall be 16.67 million transitions per second or 8.33 MHz (the same as the maximum frequency for PIO Mode 4 and DMA Mode 2).

Words in the IDENTIFY DEVICE data indicate support of the Ultra DMA feature and the Ultra DMA Modes the device is capable of supporting. The Set transfer mode subcommand in the SET FEATURES command shall be used by a host to select the Ultra DMA Mode at which the system operates. The Ultra DMA Mode selected by a host shall be less than or equal to the fastest mode of which the device is capable. Only the Ultra DMA Mode shall be selected at any given time. All timing requirements for a selected Ultra DMA Mode shall be satisfied. Devices supporting Ultra DMA Mode 2 shall also support Ultra DMA Modes 0 and 1. Devices supporting Ultra DMA Mode 1 shall also support Ultra DMA Mode 0.

An Ultra DMA capable device shall retain its previously selected Ultra DMA Mode after executing a Software reset sequence. An Ultra DMA capable device shall clear any previously selected Ultra DMA Mode and revert to its default non-Ultra DMA Modes after executing a Power on or hardware reset.

Both the host and device perform a CRC function during an Ultra DMA burst. At the end of an Ultra DMA burst the host sends the its CRC data to the device. The device compares its CRC data to the data sent from the host. If the two values do not match the device reports an error in the error register at the end of the command. If an error occurs during one or more Ultra DMA bursts for any one command, at the end of the command, the device shall report the first error that occurred.

5.5.2 Phases of operation

An Ultra DMA data transfer is accomplished through a series of Ultra DMA data in or data out bursts. Each Ultra DMA burst has three mandatory phases of operation: the initiation phase, the data transfer phase, and the Ultra DMA burst termination phase. In addition, an Ultra DMA burst may be paused during the data transfer phase (see 5.5.3 and 5.5.4 for the detailed protocol descriptions for each of these phases, 5.6.4 defines the specific timing requirements). In the following rules DMARDY- is used in cases that could apply to either DDMARDY- or HDMARDY-, and STROBE is used in cases that could apply to either DSTROBE or HSTROBE. The following are general Ultra DMA rules.

a) An Ultra DMA burst is defined as the period from an assertion of DMACK- by the host to the subsequent negation of DMACK-.

b) A recipient shall be prepared to receive at least two data words whenever it enters or resumes an Ultra DMA burst.

5.5.2.1 Ultra DMA burst initiation phase

a) The Ultra DMA burst initiation phase is started by the assertion of DMARQ signal by the device, and is ended when the transmitting side has inverted STROBE signal for transmitting the first data.

b) The Ultra DMA burst requires the assertion of DMARQ signal by the device.

c) The host asserts DMACK-signal when it is able to start the requested burst.

d) The host always asserts DMACK signal after detecting the first assertion of DMARQ signal.

e) Ultra DMA data in burst

The device starts transmission of the data to DD (15 : 0) when;

- DMACK-signal assertion has been detected,
- STOP signal negation has been detected, or
- HDMARDY-signal assertion has been detected.

f) Ultra DMA data out burst

The device should not invert the state of this signal in the period from the moment of DMARQ signal assertion or DDMARDY-signal assertion to the moment of inversion of the first STROBE signal.

g) Ultra DMA data in burst

The device should not invert the state of this signal in the period from the moment of STOP signal negation or HDMARDY-signal assertion to the moment of inversion of the first STROBE signal.

5.5.2.2 Data transfer phase

a) The Data transfer phase is defined as the period from The Ultra DMA burst initiation phase to Ultra DMA burst termination phase.

b) The receiving side stops the Ultra DMA burst temporarily by negating DMARDY-signal, and then restarts the Ultra DMA burst by asserting again.

c) The transmitting side stops the Ultra DMA burst temporarily by not-performing inversion of STROBE signal, and then restarts the Ultra DMA burst by restarting the inversion.

d) When the transmitting side has stopped the inversion of STROBE signal, the receiving side should not output termination request signal immediately.

The receiving side should negate DMARDY signal when no termination request signal has been received from the transmission side, and then should output the termination request signal when a certain wait time has elapsed.

e) The transmitting side is allowed to send STROBE signal at a transfer speed that is lower than the one in the transferable fastest Ultra DMA mode, but is not allowed to send the STROBE signal at a higher speed than this.

The receiving side should be able to receive the data in the transferable fastest Ultra DMA mode.

5.5.2.3 Ultra DMA burst termination phase

a) The transmitting side or receiving side is allowed to end the Ultra DMA burst.

b) The Ultra DMA burst termination is not the end of the command execution. When the Ultra DMA burst termination has occurred before the ending of the command, the command should be ended by starting a new Ultra DMA burst, or the host should issue command abort by outputting hard reset or soft reset to the device.

c) The Ultra DMA burst should be stopped temporarily before the receiving side outputs the ending request.

d) The host outputs the ending request by asserting STOP signal, and then the device negates DMARQ signal to confirm it.

e) The device outputs the ending request by negating DMARQ signal, and then the host asserts STOP signal to confirm it.

f) Once the transmitting side has outputted the ending request, the output state of STROBE signal should not be changed unless the receiving side has confirmed it. Then, if the STROBE signal is not in asserted state, The transmitting side should assert the STROBE signal. However, the assertion of the STROBE signal should not cause the data transfer to occur.

g) The transmitting side should return the STROBE signal to its asserted state immediately after receiving the ending request from the receiving side.

However, the returning of the STROBE signal to its asserted state should not cause the data transfer to occur and CRC to be perform.

h) Once the receiving side has outputted the ending request, the negated state of the DMARDY signal should not be changed for the remaining Ultra DMA burst to be performed.

i) The receiving side should neglect the inversion of the STROBE signal if DMARQ signal has been negated or STOP signal has been asserted.

5.5.3 Ultra DMA data in commands

5.5.3.1 Initiating an Ultra DMA data in burst

The following steps shall occur in the order they are listed unless otherwise specifically allowed (see 5.6.4.1 and 5.6.4.2 for specific timing requirements):

1) The host shall keep DMACK- in the negated state before an Ultra DMA burst is initiated.

2) The device shall assert DMARQ to initiate an Ultra DMA burst. After assertion of DMARQ the device shall not negate DMARQ until after the first negation of DSTROBE.

3) Steps (3), (4) and (5) may occur in any order or at the same time. The host shall assert STOP.

4) The host shall negate HDMARDY-.

5) The host shall negate CS0-, CS1-, DA2, DA1, and DA0. The host shall keep CS0-, CS1-, DA2, DA1, and DA0 negated until after negating DMACK- at the end of the burst.

6) Steps (3), (4) and (5) shall have occurred at least t_{ACK} before the host asserts DMACK-. The host shall keep DMACK- asserted until the end of an Ultra DMA burst.

7) The host shall release DD (15:0) within t_{AZ} after asserting DMACK-.

8) The device may assert DSTROBE t_{ZIORDY} after the host has asserted DMACK-. Once the device has driven DSTROBE the device shall not release DSTROBE until after the host has negated DMACK- at the end of an Ultra DMA burst.

9) The host shall negate STOP and assert HDMARDY- within t_{ENV} after asserting DMACK-. After negating STOP and asserting HDMARDY-, the host shall not change the state of either signal until after receiving the first transition of DSTROBE from the device (i.e., after the first data word has been received).

10) The device shall drive DD (15:0) no sooner than t_{ZAD} after the host has asserted DMACK-, negated STOP, and asserted HDMARDY-.

11) The device shall drive the first word of the data transfer onto DD (15:0). This step may occur when the device first drives DD (15:0) in step (10).

12) To transfer the first word of data the device shall negate DSTROBE within t_{FS} after the host has negated STOP and asserted HDMARDY-. The device shall negate DSTROBE no sooner than t_{DVS} after driving the first word of data onto DD (15:0).

5.5.3.2 The data in transfer

The following steps shall occur in the order they are listed unless otherwise specifically allowed (see 5.6.4.3 and 5.6.4.2):

1) The device shall drive a data word onto DD (15:0).

2) The device shall generate a DSTROBE edge to latch the new word no sooner than t_{DVS} after changing the state of DD (15:0). The device shall generate a DSTROBE edge no more frequently than t_{CYC} for the selected Ultra DMA Mode. The device shall not generate two rising or two falling DSTROBE edges more frequently than $2t_{CYC}$ for the selected Ultra DMA mode.

3) The device shall not change the state of DD (15:0) until at least t_{DVH} after generating a DSTROBE edge to latch the data.

4) The device shall repeat steps (1), (2) and (3) until the data transfer is complete or an Ultra DMA burst is paused, whichever occurs first.

5.5.3.3 Pausing an Ultra DMA data in burst

The following steps shall occur in the order they are listed unless otherwise specifically allowed (see 5.6.4.4 and 5.6.4.2 for specific timing requirements).

a) Device pausing an Ultra DMA data in burst

   1) The device shall not pause an Ultra DMA burst until at least one data word of an Ultra DMA burst has been transferred.

   2) The device shall pause an Ultra DMA burst by not generating DSTROBE edges.

      NOTE - The host shall not immediately assert STOP to initiate Ultra DMA burst termination when the device stops generating STROBE edges. If the device does not negate DMARQ, in order to initiate ULTRA DMA burst termination, the host shall negate HDMARDY- and wait t_{RP} before asserting STOP.

3) The device shall resume an Ultra DMA burst by generating a DSTROBE edge.

b) Host pausing an Ultra DMA data in burst

1) The host shall not pause an Ultra DMA burst until at least one data word of an Ultra DMA burst has been transferred.

2) The host shall pause an Ultra DMA burst by negating HDMARDY-.

3) The device shall stop generating DSTROBE edges within t_{RFS} of the host negating HDMARDY-.

4) If the host negates HDMARDY- within t_{SR} after the device has generated a DSTROBE edge, then the host shall be prepared to receive zero or one additional data words. If the host negates HDMARDY- greater than t_{SR} after the device has generated a DSTROBE edge, then the host shall be prepared to receive zero, one or two additional data words. The additional data words are a result of cable round trip delay and t_{RFS} timing for the device.

5) The host shall resume an Ultra DMA burst by asserting HDMARDY-.

5.5.3.4 Terminating an Ultra DMA data in burst

a) Device terminating an Ultra DMA data in burst

The following steps shall occur in the order they are listed unless otherwise specifically allowed (see 5.6.4.5 and 5.6.4.2 for specific timing requirements):

1) The device shall initiate termination of an Ultra DMA burst by not generating DSTROBE edges.

2) The device shall negate DMARQ no sooner than t_{SS} after generating the last DSTROBE edge. The device shall not assert DMARQ again until after the Ultra DMA burst is terminated.

3) The device shall release DD (15:0) no later than t_{AZ} after negating DMARQ.

4) The host shall assert STOP within t_{LI} after the device has negated DMARQ. The host shall not negate STOP again until after the Ultra DMA burst is terminated.

5) The host shall negate HDMARDY- within t_{LI} after the device has negated DMARQ. The host shall continue to negate HDMARDY- until the Ultra DMA burst is terminated. Steps (4) and (5) may occur at the same time.

6) The host shall drive DD (15:0) no sooner than t_{ZAH} after the device has negated DMARQ. For this step, the host may first drive DD (15:0) with the result of its CRC calculation (see 5.5.5):

7) If DSTROBE is negated, the device shall assert DSTROBE within t_{LI} after the host has asserted STOP. No data shall be transferred during this assertion. The host shall ignore this transition on DSTROBE. DSTROBE shall remain asserted until the Ultra DMA burst is terminated.

8) If the host has not placed the result of its CRC calculation on DD (15:0) since first driving DD (15:0) during (6), the host shall place the result of its CRC calculation on DD (15:0) (see 5.5.5).

9) The host shall negate DMACK- no sooner than t_{MLI} after the device has asserted DSTROBE and negated DMARQ and the host has asserted STOP and negated HDMARDY-, and no sooner than t_{DVS} after the host places the result of its CRC calculation on DD (15:0).

10) The device shall latch the host's CRC data from DD (15:0) on the negating edge of DMACK-.

11) The device shall compare the CRC data received from the host with the results of its own CRC calculation. If a miscompare error occurs during one or more Ultra DMA bursts for any one command, at the end of the command the device shall report the first error that occurred (see 5.5.5).

12) The device shall release DSTROBE within t_{IORDYZ} after the host negates DMACK-.

13) The host shall not negate STOP no assert HDMARDY- until at least t_{ACK} after negating DMACK-.

14) The host shall not assert DIOR-, CS0-, CS1-, DA2, DA1, or DA0 until at least t_{ACK} after negating DMACK.

b) Host terminating an Ultra DMA data in burst

The following steps shall occur in the order they are listed unless otherwise specifically allowed (see 5.6.4.6 and 5.6.4.2 for specific timing requirements):

1) The host shall not initiate Ultra DMA burst termination until at least one data word of an Ultra DMA burst has been transferred.

2) The host shall initiate Ultra DMA burst termination by negating HDMARDY-. The host shall continue to negate HDMARDY- until the Ultra DMA burst is terminated.

3) The device shall stop generating DSTROBE edges within t_{RFS} of the host negating HDMARDY-.

4) If the host negates HDMARDY- within t_{SR} after the device has generated a DSTROBE edge, then the host shall be prepared to receive zero or one additional data words. If the host negates HDMARDY- greater than t_{SR} after the device has generated a DSTROBE edge, then the host shall be prepared to receive zero, one or two additional data words. The additional data words are a result of cable round trip delay and t_{RFS} timing for the device.

5) The host shall assert STOP no sooner than t_{RP} after negating HDMARDY-. The host shall not negate STOP again until after the Ultra DMA burst is terminated.

6) The device shall negate DMARQ within t_{LI} after the host has asserted STOP. The device shall not assert DMARQ again until after the Ultra DMA burst is terminated.

7) If DSTROBE is negated, the device shall assert DSTROBE within t_{LI} after the host has asserted STOP. No data shall be transferred during this assertion. The host shall ignore this transition on DSTROBE. DSTROBE shall remain asserted until the Ultra DMA burst is terminated.

8) The device shall release DD (15:0) no later than t_{AZ} after negating DMARQ.

9) The host shall drive DD (15:0) no sooner than t_{ZAH} after the device has negated DMARQ. For this step, the host may first drive DD (15:0) with the result of its CRC calculation (see 5.5.5).

10) If the host has not placed the result of its CRC calculation on DD (15:0) since first driving DD (15:0) during (9), the host shall place the result of its CRC calculation on DD (15:0) (see 5.5.5).

11) The host shall negate DMACK- no sooner than t_{MLI} after the device has asserted DSTROBE and negated DMARQ and the host has asserted STOP and negated HDMARDY-, and no sooner than t_{DVS} after the host places the result of its CRC calculation on DD (15:0).

12) The device shall latch the host's CRC data from DD (15:0) on the negating edge of DMACK-.

13) The device shall compare the CRC data received from the host with the results of its own CRC calculation. If a miscompare error occurs during one or more Ultra DMA burst for any one command, at the end of the command, the device shall report the first error that occurred (see 5.5.5).

14) The device shall release DSTROBE within t_{IORDYZ} after the host negates DMACK-.

15) The host shall neither negate STOP nor assert HDMARDY- until at least t_{ACK} after the host has negated DMACK-.

16) The host shall not assert DIOR-, CS0-, CS1-, DA2, DA1, or DA0 until at least t_{ACK} after negating DMACK.

5.5.4 Ultra DMA data out commands

5.5.4.1 Initiating an Ultra DMA data out burst

The following steps shall occur in the order they are listed unless otherwise specifically allowed (see 5.6.4.7 and 5.6.4.2 for specific timing requirements):

1) The host shall keep DMACK- in the negated state before an Ultra DMA burst is initiated.

2) The device shall assert DMARQ to initiate an Ultra DMA burst.

3) Steps (3), (4), and (5) may occur in any order or at the same time. The host shall assert STOP.

4) The host shall assert HSTROBE.

5) The host shall negate CS0-, CS1-, DA2, DA1, and DA0. The host shall keep CS0-, CS1-, DA2, DA1, and DA0 negated until after negating DMACK- at the end of the burst.

6) Steps (3), (4), and (5) shall have occurred at least t_{ACK} before the host asserts DMACK-. The host shall keep DMACK- asserted until the end of an Ultra DMA burst.

7) The device may negate DDMARDY- t_{ZIORDY} after the host has asserted DMACK-. Once the device has negated DDMARDY-, the device shall not release DDMARDY- until after the host has negated DMACK- at the end of an Ultra DMA burst.

8) The host shall negate STOP within t_{ENV} after asserting DMACK-. The host shall not assert STOP until after the first negation of HSTROBE.

9) The device shall assert DDMARDY- within t_{LI} after the host has negated STOP. After asserting DMARQ and DDMARDY- the device shall not negate either signal until after the first negation of HSTROBE by the host.

10) The host shall drive the first word of the data transfer onto DD (15:0). This step may occur any time during Ultra DMA burst initiation.

11) To transfer the first word of data: the host shall negate HSTROBE no sooner than t_{LI} after the device has asserted DDMARDY-. The host shall negate HSTROBE no sooner than t_{DVS} after the driving the first word of data onto DD (15:0).

5.5.4.2 The data out transfer

The following steps shall occur in the order they are listed unless otherwise specifically allowed (see 5.6.4.8 and 5.6.4.2 for specific timing requirements):

1) The host shall drive a data word onto DD (15:0).

2) The host shall generate an HSTROBE edge to latch the new word no sooner than t_{DVS} after changing the state of DD (15:0). The host shall generate an

HSTROBE edge no more frequently than t_{CYC} for the selected Ultra DMA Mode. The host shall not generate two rising or falling HSTROBE edges more frequently than 2 t_{CYC} for the selected Ultra DMA mode.

3) The host shall not change the state of DD (15:0) until at least t_{DVH} after generating an HSTROBE edge to latch the data.

4) The host shall repeat steps (1), (2) and (3) until the data transfer is complete or an Ultra DMA burst is paused, whichever occurs first.

5.5.4.3 Pausing an Ultra DMA data out burst

The following steps shall occur in the order they are listed unless otherwise specifically allowed (see 5.6.4.9 and 5.6.4.2 for specific timing requirements).

a) Host pausing an Ultra DMA data out burst

1) The host shall not pause an Ultra DMA burst until at least one data word of an Ultra DMA burst has been transferred.

2) The host shall pause an Ultra DMA burst by not generating an HSTROBE edge.

Note: The device shall not immediately negate DMARQ to initiate Ultra DMA burst termination when the host stops generating HSTROBE edges. If the host does not assert STOP, in order to initiate Ultra DMA burst termination, the device shall negate DDMARDY- and wait t_{RP} before negating DMARQ.

3) The host shall resume an Ultra DMA burst by generating an HSTROBE edge.

b) Device pausing an Ultra DMA data out burst

1) The device shall not pause an Ultra DMA burst until at least one data word of an Ultra DMA burst has been transferred.

2) The device shall pause an Ultra DMA burst by negating DDMARDY-.

3) The host shall stop generating HSTROBE edges within t_{RFS} of the device negating DDMARDY-.

4) If the device negates DDMARDY- within t_{SR} after the host has generated an HSTROBE edge, then the device shall be prepared to receive zero or one additional data words. If the device negates DDMARDY- greater than t_{SR} after the host has generated an HSTROBE edge, then the device shall be prepared to receive zero, one or two additional data words. The additional data words are a result of cable round trip delay and t_{RFS} timing for the host.

5) The device shall resume an Ultra DMA burst by asserting DDMARDY-.

5.5.4.4 Terminating an Ultra DMA data out burst

a) Host terminating an Ultra DMA data out burst

The following stops shall occur in the order they are listed unless otherwise specifically allowed (see 5.6.4.10 and 5.6.4.2 for specific timing requirements):

1) The host shall initiate termination of an Ultra DMA burst by not generating HSTROBE edges.

2) The host shall assert STOP no sooner than t_{SS} after it last generated an HSTROBE edge. The host shall not negate STOP again until after the Ultra DMA burst is terminated.

3) The device shall negate DMARQ within t_{LI} after the host asserts STOP. The device shall not assert DMARQ again until after the Ultra DMA burst is terminated.

4) The device shall negate DDMARDY- with t_{LI} after the host has negated STOP. The device shall not assert DDMARDY- again until after the Ultra DMA burst termination is complete.

5) If HSTROBE is negated, the host shall assert HSTROBE with t_{LI} after the device has negated DMARQ. No data shall be transferred during this assertion. The device shall ignore this transition on HSTROBE. HSTROBE shall remain asserted until the Ultra DMA burst is terminated.

6) The host shall place the result of its CRC calculation on DD (15:0) (see 5.5.5)

7) The host shall negate DMACK- no sooner than t_{MLI} after the host has asserted HSTROBE and STOP and the device has negated DMARQ and DDMARDY-, and no sooner than t_{DVS} after placing the result of its CRC calculation on DD (15:0).

8) The device shall latch the host's CRC data from DD (15:0) on the negating edge of DMACK-.

9) The device shall compare the CRC data received from the host with the results of its own CRC calculation. If a miscompare error occurs during one or more Ultra DMA bursts for any one command, at the end of the command, the device shall report the first error that occurred (see 5.5.5).

10) The device shall release DDMARDY- within t_{IORDYZ} after the host has negated DMACK-.

11) The host shall neither negate STOP nor negate HSTROBE until at least t_{ACK} after negating DMACK-.

12) The host shall not assert DIOW-, CS0-, CS1-, DA2, DA1, or DA0 until at least t_{ACK} after negating DMACK.

b) Device terminating an Ultra DMA data out burst

The following steps shall occur in the order they are listed unless otherwise specifically allowed (see 5.6.4.11 and 5.6.4.2 for specific timing requirements):

1) The device shall not initiate Ultra DMA burst termination until at least one data word of an Ultra DMA burst has been transferred.

2) The device shall initiate Ultra DMA burst termination by negating DDMARDY-.

3) The host shall stop generating an HSTROBE edges within t_{RFS} of the device negating DDMARDY-.

4) If the device negates DDMARDY- within t_{SR} after the host has generated an HSTROBE edge, then the device shall be prepared to receive zero or one additional data words. If the device negates DDMARDY- greater than t_{SR} after the host has generated an HSTROBE edge, then the device shall be prepared to receive zero, one or two additional data words. The additional data words are a result of cable round trip delay and t_{RFS} timing for the host.

5) The device shall negate DMARQ no sooner than t_{RP} after negating DDMARDY-. The device shall not assert DMARQ again until after the Ultra DMA burst is terminated.

6) The host shall assert STOP with t_{LI} after the device has negated DMARQ. The host shall not negate STOP again until after the Ultra DMA burst is terminated.

7) If HSTROBE is negated, the host shall assert HSTROBE with t_{LI} after the device has negated DMARQ. No data shall be transferred during this assertion. The device shall ignore this transition of HSTROBE. HSTROBE shall remain asserted until the Ultra DMA burst is terminated.

8) The host shall place the result of its CRC calculation on DD (15:0) (see 5.5.5).

9) The host shall negate DMACK- no sooner than t_{MLI} after the host has asserted HSTROBE and STOP and the device has negated DMARQ and DDMARDY-, and no sooner than t_{DVS} after placing the result of its CRC calculation on DD (15:0).

10) The device shall latch the host's CRC data from DD (15:0) on the negating edge of DMACK-.

11) The device shall compare the CRC data received from the host with the results of its own CRC calculation. If a miscompare error occurs during one or more Ultra DMA bursts for any one command, at the end of the command, the device shall report the first error that occurred (see 5.5.5).

12) The device shall release DDMARDY- within t_{IORDYZ} after the host has negated DMACK-.

13) The host shall neither negate STOP nor HSTROBE until at least t_{ACK} after negating DMACK-.

14) The host shall not assert DIOW-, CS0-, CS1-, DA2, DA1, or DA0 until at least t_{ACK} after negating DMACK.

5.5.5 Ultra DMA CRC rules

The following is a list of rules for calculating CRC, determining if a CRC error has occurred during an Ultra DMA burst, and reporting any error that occurs at the end of a command.

a) Both the host and the device shall have a 16-bit CRC calculation function.

b) Both the host and the device shall calculate a CRC value for each Ultra DMA burst.

c) The CRC function in the host and the device shall be initialized with a seed of 4ABAh at the beginning of an Ultra DMA burst before any data is transferred.

d) For each STROBE transition used for data transfer, both the host and the device shall calculate a new CRC value by applying the CRC polynomial to the current value of their individual CRC functions and the word being transferred. CRC is not calculated for the return of STROBE to the asserted state after the Ultra DMA burst termination request has been acknowledged.

e) At the end of any Ultra DMA burst the host shall send the results of its CRC calculation function to the device on DD (15:0) with the negation of DMACK-.

f) The device shall then compare the CRC data from the host with the calculated value in its own CRC calculation function. If the two values do not match, the device shall save the error and report it at the end of the command. A subsequent Ultra DMA burst for the same command that does not have a CRC error shall not clear an error saved from a previous Ultra DMa burst in the same command. If a miscompare error occurs during one or more Ultra DMA bursts for any one command, at the end of the command, the device shall report the first error that occurred.

g) For READ DMA or WRITE DMA commands: When a CRC error is detected, it shall be reported by setting both ICRC and ABRT (bit 7 and bit 2 in the Error register) to one. ICRC is defined as the "Interface CRC Error" bit. The host shall respond to this error by re-issuing the command.

h) A host may send extra data words on the last Ultra DMA burst of a data out command. If a device determines that all data has been transferred for a command, the device shall terminate the burst. A device may have already received more data words than were required for the command. These extra words are used by both the host and the device to calculate the CRC, but, on an Ultra DMA data out burst, the extra words shall be discarded by the device.

i) The CRC generator polynomial is : $G(X) = X^{16} + X^{12} + X^5 + 1$.

Note: Since no bit clock is available, the recommended approach for calculating CRC is to use a word clock derived from the bus strobe. The combinational logic shall then be equivalent to shifting sixteen bits serially through the generator polynominal where DD0 is shifted in first and DD15 is shifted in last.

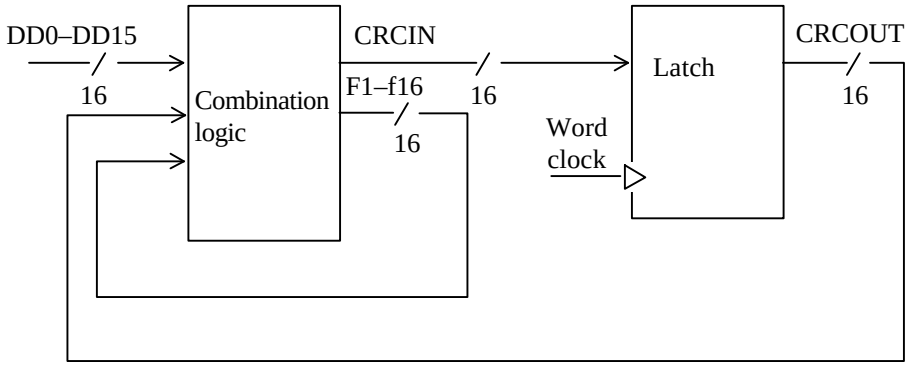


Figure 5.8 An example of generation of parallel CRC

Table 5.14 Parallel generation equation of CRC polynomial

CRCINO=f_{16}	CRCIN8 = f_8 XOR f_{13}
CRCIN1=f_{15}	CRCIN9 = f_7 XOR f_{12}
CRCIN2=f_{14}	CRCIN10 = f_6 XOR f_{11}
CRCIN3=f_{13}	CRCIN11 = f_5 XOR f_{10}
CRCIN4=f_{12}	CRCIN12 = f_4 XOR f_9 XOR f_{16}
CRCIN5=f_{11} XOR f	CRCIN13 = f_3 XOR f_8 XOR f_{15}
CRCIN6=f_{10} XOR f_{15}	CRCIN14 = f_2 XOR f_7 XOR f_{14}
CRCIN7=f_9 XOR f_{14}	CRCIN15 = f_1 XOR f_6 XOR f_{13}

f_1 = DD0 XOR $CRCOUT_{15}$
f_2 = DD1 XOR $CRCOUT_{14}$
f_3 = DD2 XOR $CRCOUT_{13}$
f_4 = DD3 XOR $CRCOUT_{12}$
f_5 = DD4 XOR $CRCOUT_{11}$ XOR f_1
f_6 = DD5 XOR $CRCOUT_{10}$ XOR f_2
f_7 = DD6 XOR $CRCOUT_9$ XOR f_3
f_8 = DD7 XOR $CRCOUT_8$ XOR f_4

f_9 = DD8 XOR CRCOUT7 XOR f_5
f_{10} = DD9 XOR CRCOUT6 XOR f_6
f_{11} = DD10 XOR CRCOUT5 XOR f_7
f_{12} = DD11 XOR CRCOUT4 XOR f_1 XOR f_8
f_{13} = DD12 XOR CRCOUT3 XOR f_2 XOR f_9
f_{14} = DD13 XOR CRCOUT2 XOR f_3 XOR f_{10}
f_{15} = DD14 XOR CRCOUT1 XOR f_4 XOR f_{11}
f_{16} = DD15 XOR CRCOUT0 XOR f_5 XOR f_{12}

DD : Data from bust f : Feedback
CRCIN : Output of combination logic (the next CRC)
CROUT : Result of 16 bit latch (current CRC)

5.5.6 Series termination required for Ultra DMA

Series termination resistors are required at both the host and the device for operation in any of the Ultra DMA Modes. The following table describes recommended values for series termination at the host and the device.

Table 5.15 Recommended series termination for Ultra DMA

Signal	Host Termination	Device Termination
DIOR-:HDMARDY-:HSTROBE	33 ohm	82 ohm
DIOW-:STOP	33 ohm	82 ohm
CS0-, CS1-	33 ohm	82 ohm
DA0, DA1, DA2	33 ohm	82 ohm
DMACK-	33 ohm	82 ohm
DD15 through DD0	33 ohm	240 ohm (100 MHz)
DMARQ	82 ohm	33 ohm
INTRQ	82 ohm	33 ohm
IORDY:DDMARDY-:DSTROBE	82 ohm	22 ohm
Note: Only those signals requiring termination are listed in this table. If a signal is not listed, series termination is not required for operation in an Ultra DMA Mode. For signals also requiring a pull-up or pull-down resistor at the host see Figure 5.9.		

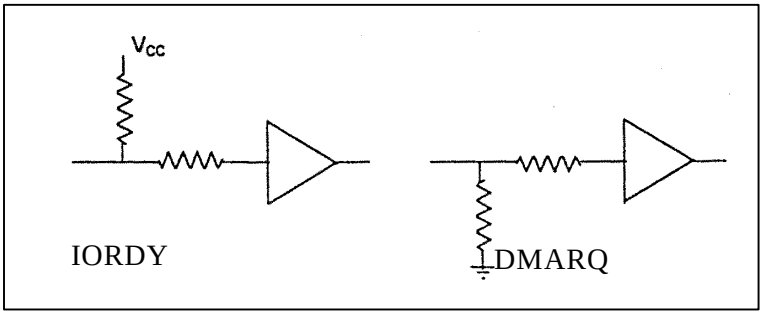


Figure 5.9 Ultra DMA termination with pull-up or pull-down

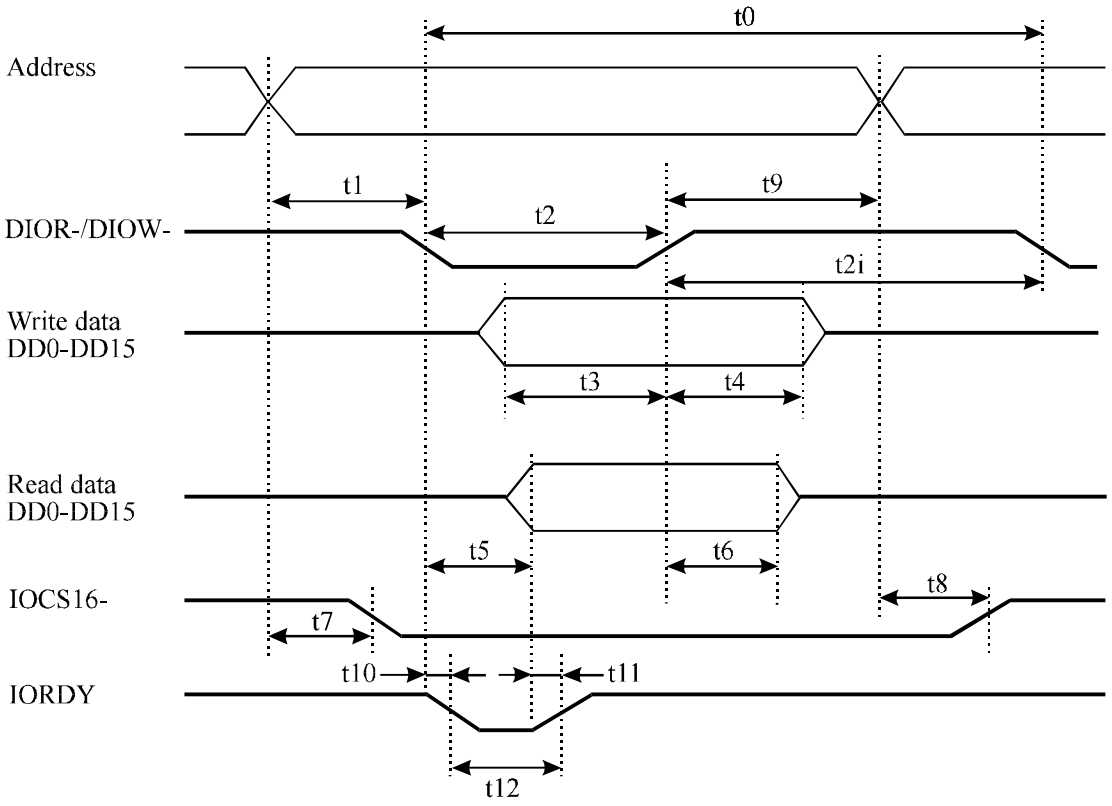
Configuration of cable

For the configuration of the cable (common use of primary port and secondary port), DMACK signal should not be used in common. It is not recommended to use DIOR-, DIOW- and IORDY signal in common.

5.6 Timing

5.6.1 PIO data transfer

Figure 5.10 shows of the data transfer timing between the device and the host system.

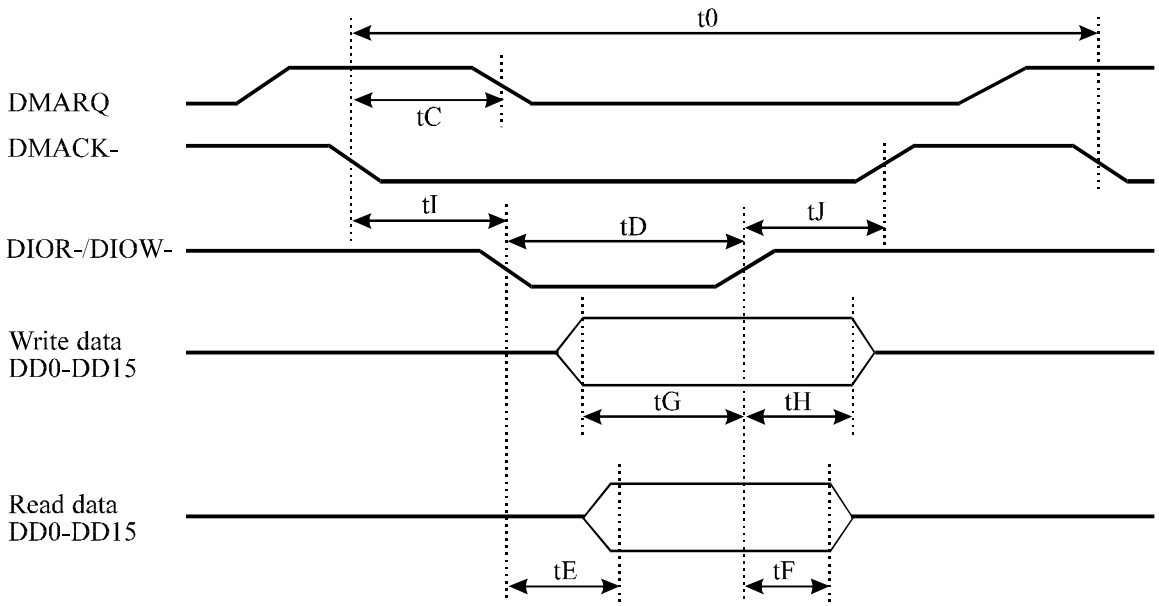


Symbol	Timing parameter	Min.	Max.	Unit
t0	Cycle time	120	—	ns
t1	Data register selection setup time for DIOR-/DIOW-	25	—	ns
t2	Pulse width of DIOR-/DIOW-	70	—	ns
t2i	Recovery time of DIOR-/DIOW-	25	—	ns
t3	Data setup time for DIOW-	20	—	ns
t4	Data hold time for DIOW-	10	—	ns
t5	Time from DIOR- assertion to read data available	—	20	ns
t6	Data hold time for DIOR-	5	—	ns
t7	Time from Data register selection to IOCS16- assertion	—	20	ns
t8	Time from Data register selection reset to IOCS16- negation	—	5	ns
t9	Data register selection hold time for DIOR-/DIOW-	10	—	ns
t10	Time from DIOR-/DIOW- assertion to IORDY "low" level	—	35	ns
t11	Time from validity of read data to IORDY "high" level	0	—	ns
t12	Pulse width of IORDY	—	1,250	ns

Figure 5.10 Data transfer timing

5.6.2 Single word DMA data transfer

Figure 5.9 show the single word DMA data transfer timing between the device and the host system.

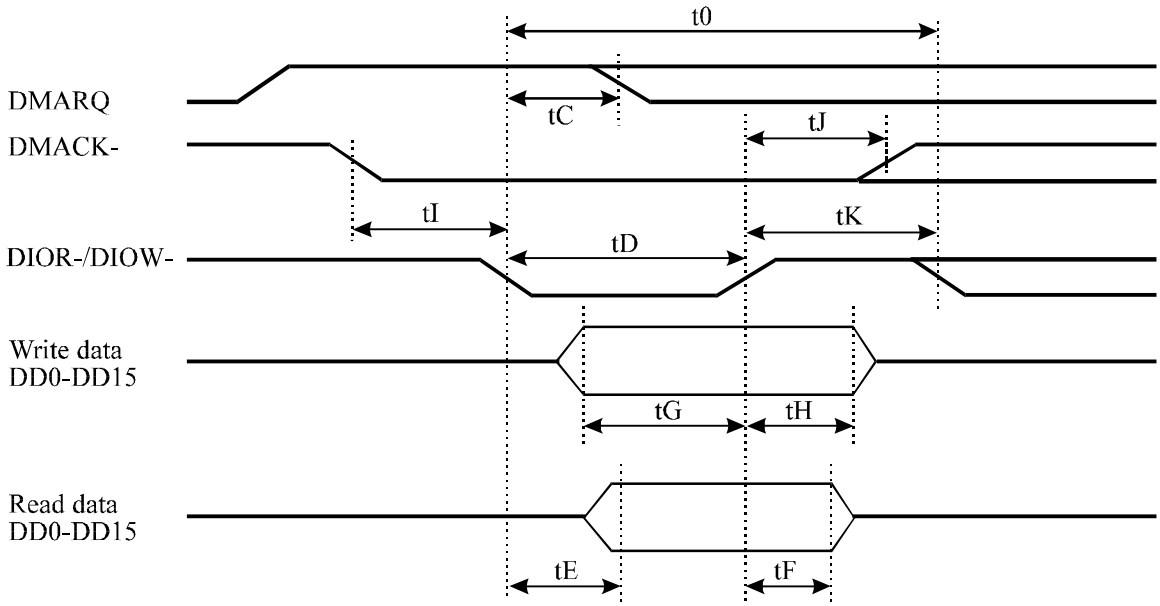


Symbol	Timing parameter	Min.	Max.	Unit
t0	Cycle time	240	—	ns
tC	Delay time from DMACK assertion to DMARQ negation	—	80	ns
tD	Pulse width of DIOR-/DIOW-	120	—	ns
tE	Data setup time for DIOR-	—	60	ns
tF	Data hold time for DIOR-	5	—	ns
tG	Data setup time for DIOW-	35	—	ns
tH	Data hold time for DIOW-	20	—	ns
tI	DMACK setup time for DIOR-/DIOW-	0	—	ns
tJ	DMACK hold time for DIOR-/DIOW-	0	—	ns

Figure 5.11 Single word DMA data transfer timing (mode 2)

5.6.3 Multiword DMA data transfer

Figure 5.10 shows the multiword DMA data transfer timing between the device and the host system.



Symbol	Timing parameter	Min.	Max.	Unit
t0	Cycle time	120	—	ns
tC	Delay time from DIOR-/DIOW- assertion to DMARQ negation	—	35	ns
tD	Pulse width of DIOR-/DIOW-	70	—	ns
tE	Data setup time for DIOR-	—	30	ns
tF	Data hold time for DIOR-	5	—	ns
tG	Data setup time for DIOW-	20	—	ns
tH	Data hold time for DIOW-	10	—	ns
tI	DMACK setup time for DIOR-/DIOW-	0	—	ns
tJ	DMACK hold time for DIOR-/DIOW-	5	—	ns
tK	Continuous time of high level for DIOR-/DIOW-	25	—	ns

Figure 5.12 Multiword DMA data transfer timing (mode 2)

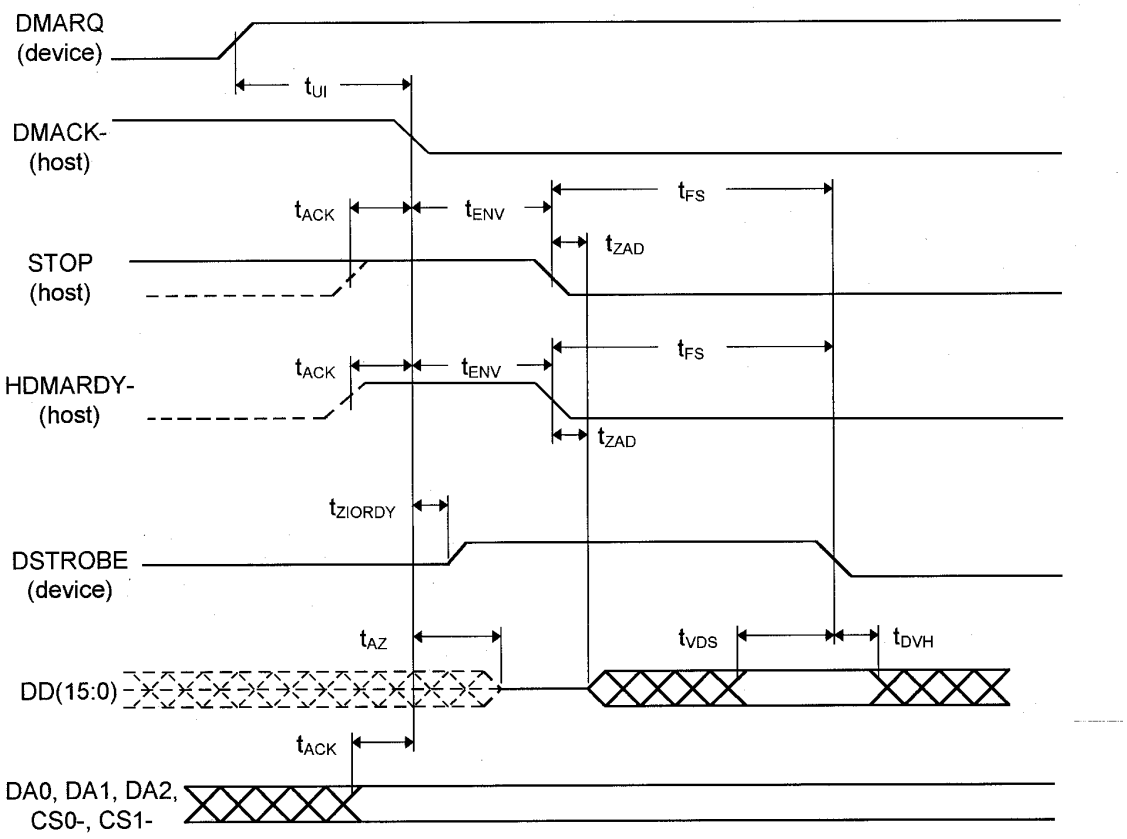
5.6.4 Transfer of Ultra DMA data

Figures 5.13 to 5.22 define the timings concerning every phase for the Ultra DMA Burst.

Table 5.13 includes the timing for each Ultra DMA mode.

5.6.4.1 Starting of Ultra DMA data In Burst

The timing for each Ultra DMA mode is included in 5.6.4.2.



Note : The definitions of STOP, HDMARDY- and DSTROBE signals are valid before the assertion of DMACK signal.

Figure 5.13 Starting of Ultra DMA data In Burst transfer

5.6.4.2 Ultra DMA data burst timing requirements

Table 5.16 Ultra DMA data burst timing requirements (1 of 2)

NAME	MODE 0 (in ns)		MODE 1 (in ns)		MODE 2 (in ns)		COMMENT
	MIN	MAX	MIN	MAX	MIN	MAX	
t_{CYC}	114		75		55		Cycle time (from STROBE edge to STROBE edge)
$t2_{CYC}$	235		156		117		Two cycle time (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)
t_{DS}	15		10		7		Data setup time (at recipient)
t_{DH}	3		3		3		Data hold time (at recipient)
t_{DVS}	70		48		34		Data valid setup time at sender (from data bus being valid until STROBE edge)
t_{DVH}	6		6		6		Data valid hold time at sender (from STROBE edge until data may become invalid)
t_{FS}	0	230	0	200	0	170	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)
t_{LI}	0	150	0	150	0	150	Limited interlock time (see Note 1)
t_{MLI}	20		20		20		Interlock time with minimum (see Note 1)
t_{UI}	0		0		0		Unlimited interlock time (see Note 1)
t_{AZ}		10		10		10	Maximum time allowed for output drivers to release (from being asserted or negated)
t_{ZAH}	20		20		20		Minimum delay time required for output drivers to assert or negate (from released state)
t_{ZAD}	0		0		0		
t_{ENV}	20	70	20	70	20	70	Envelope time (from DMACK- to STOP and HDMARDY- during data in burst initiation and from DMACK to STOP during data out burst initiation)
t_{SR}		50		30		20	STROBE-to-DMARDY-time (if DMARDY- is negated before this long after STROBE edge, the recipient shall receive no more than one additional data word)

Table 5.16 Ultra DMA data burst timing requirements (2 of 2)

NAME	MODE 0 (in ns)		MODE 1 (in ns)		MODE 2 (in ns)		COMMENT
	MIN	MAX	MIN	MAX	MIN	MAX	
t_{RFS}		75		60		50	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of DMARDY)
t_{RP}	160		125		100		Ready-to-pause time (that recipient shall wait to initiate pause after negating DMARDY-)
t_{IORDYZ}		20		20		20	Pull-up time before allowing IORDY to be released
t_{ZIORDY}	0		0		0		Minimum time device shall wait before driving IORDY
t_{ACK}	20		20		20		Setup and hold times for DMACK- (before assertion or negation)
t_{SS}	50		50		50		Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)

Notes:

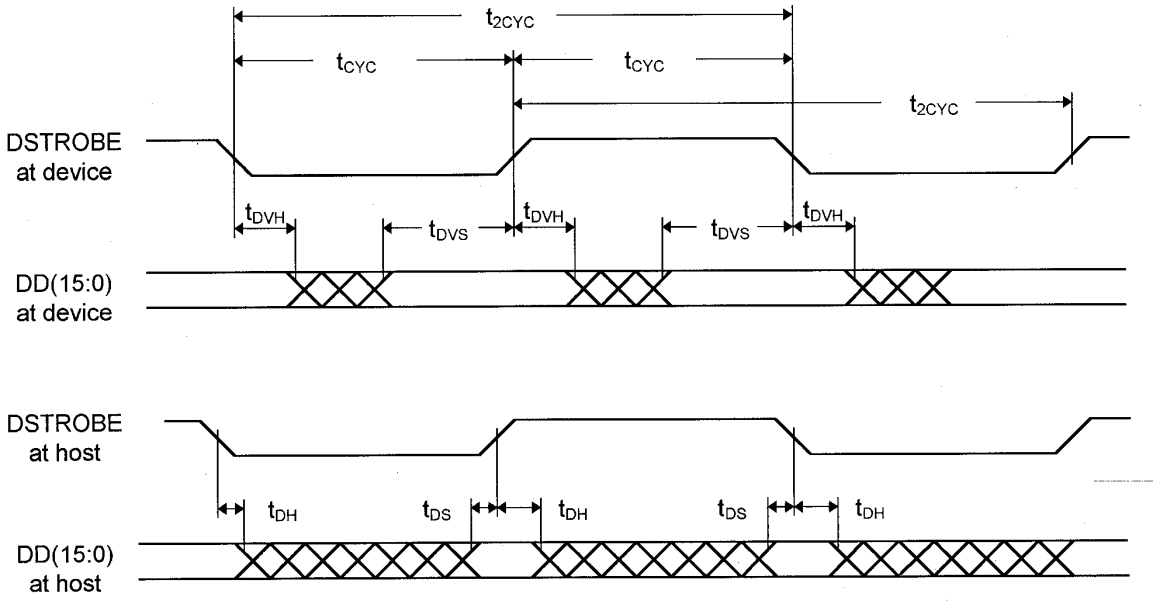
1) t_{UI}, t_{MLI} and t_{LI} indicate sender -to-recipient or recipient-to-sender interlocks, that is, one agent (either sender or recipient) is waiting for the other agent to respond with a signal before proceeding. t_{UI} is an unlimited interlock, that has no maximum time value. t_{MLI} is a limited time-out that has a defined minimum. t_{LI} is a limited time-out, that has a defined maximum.

2) All timing parameters are measured at the connector of the device to which the parameter applies. For example, the sender shall stop generating STROBE edges t_{RFS} after the negation of DMARDY-. Both STROBE and DMARDY- timing measurements are taken at the connector of the sender.

3) All timing measurement switching points (low to high and high to low) are to be taken at 1.5 V.

5.6.4.3 Sustained Ultra DMA data in burst

5.6.4.2 contains the values for the timings for each of the Ultra DMA Modes.

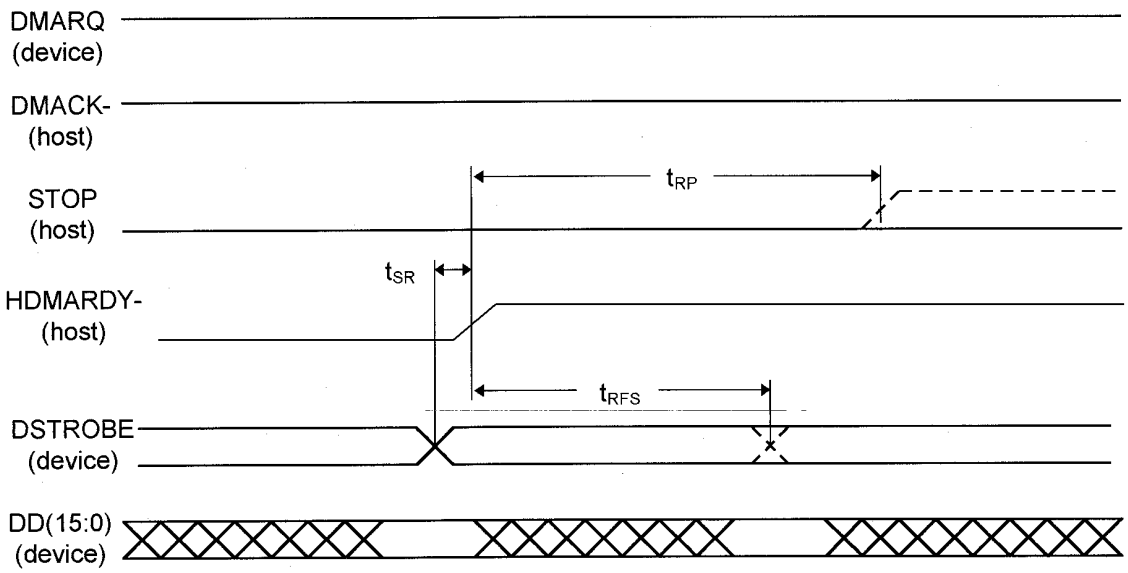


Note: DD (15:0) and DSTROBE are shown at both the host and the device to emphasize that cable setting time as well as cable propagation delay shall not allow the data signals to be considered stable at the host until some time after they are driven by the device.

Figure 5.14 Sustained Ultra DMA data in burst

5.6.4.4 Host pausing an Ultra DMA data in burst

5.6.4.2 contains the values for the timings for each of the Ultra DMA Modes.



Notes:

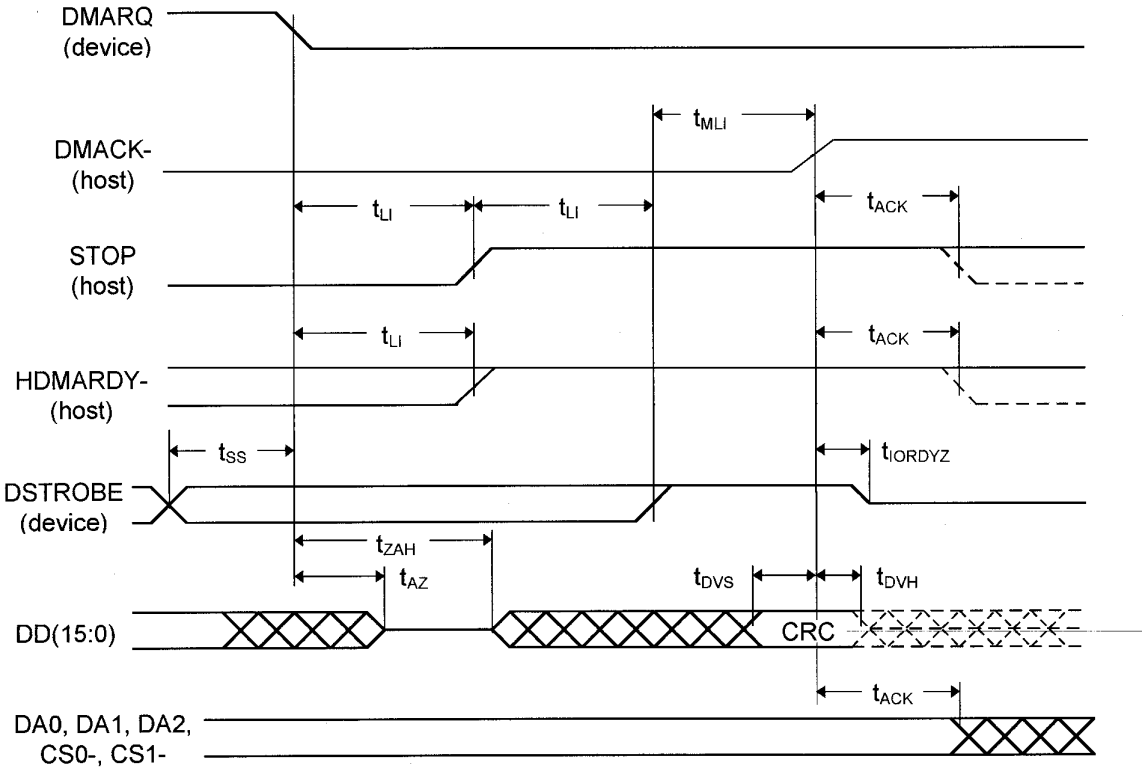
1) The host may assert STOP to request termination of the Ultra DMA burst no sooner than t_{RP} after HDMARDY- is negated.

2) If the t_{SR} timing is not satisfied, the host may receive zero, one or two more data words from the device.

Figure 5.15 Host pausing an Ultra DMA data in burst

5.6.4.5 Device terminating an Ultra DMA data in burst

5.6.4.2 contains the values for the timings for each of the Ultra DMA Modes.

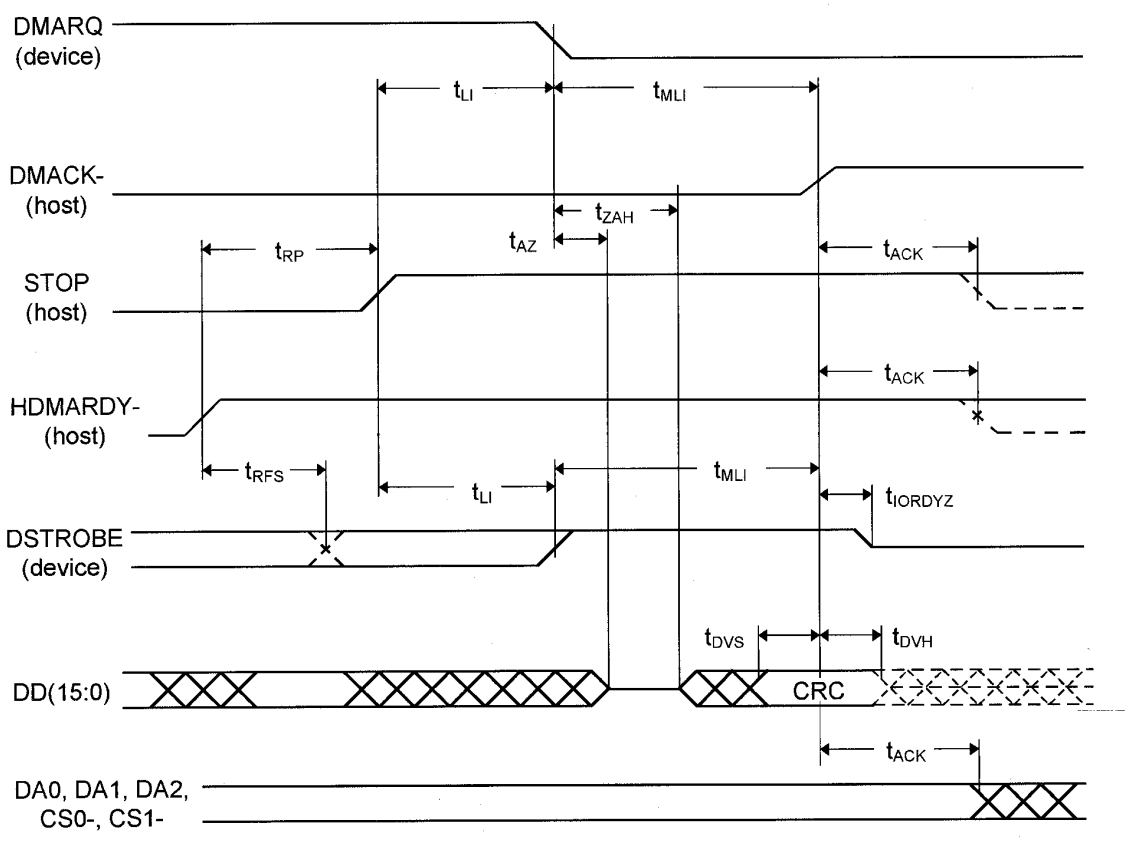


Note: The definitions for the STOP, HDMARDY- and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

Figure 5.16 Device terminating an Ultra DMA data in burst

5.6.4.6 Host terminating an Ultra DMA data in burst

5.6.4.2 contains the values for the timings for each of the Ultra DMA Modes.

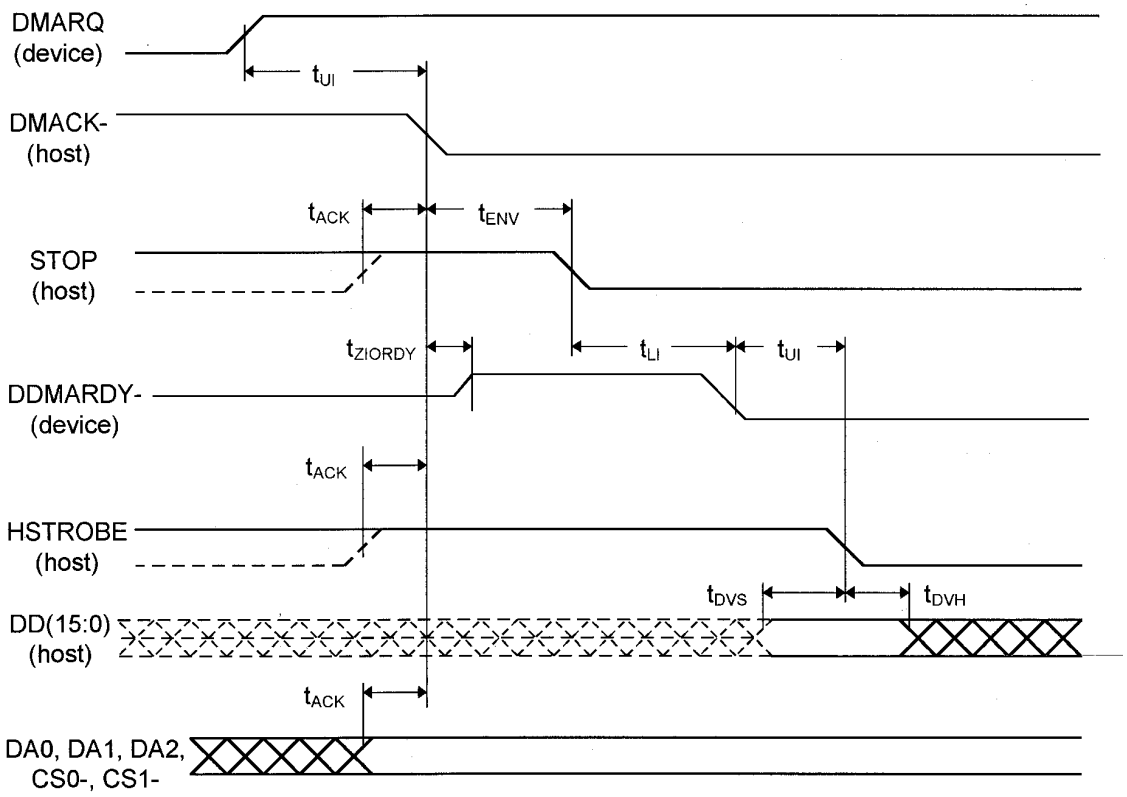


Note: The definitions for the STOP, HDMARDY- and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

Figure 5.17 Host terminating an Ultra DMA data in burst

5.6.4.7 Initiating an Ultra DMA data out burst

5.6.4.2 contains the values for the timings for each of the Ultra DMA Modes.

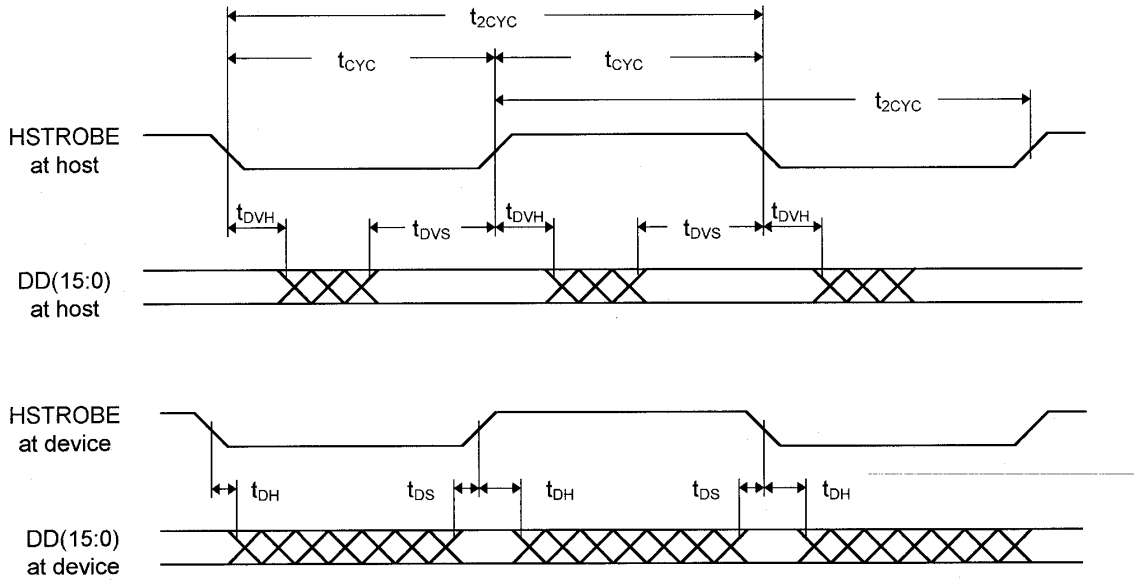


Note: The definitions for the STOP, DDMARDY- and HSTROBE signal lines are not in effect until DMARQ and DMACK are asserted.

Figure 5.18 Initiating an Ultra DMA data out burst

5.6.4.8 Sustained Ultra DMA data out burst

5.6.4.2 contains the values for the timings for each of the Ultra DMA Modes.

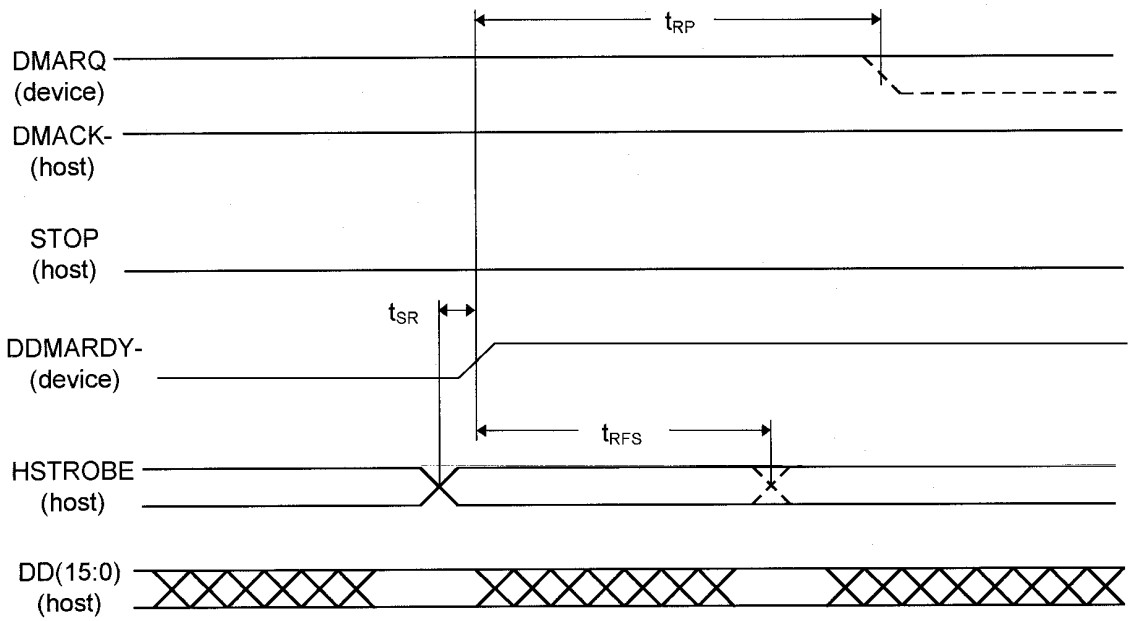


Note: DD (15:0) and HSTROBE signals are shown at both the device and the host to emphasize that cable setting time as well as cable propagation delay shall not allow the data signals to be considered stable at the device until some time after they are driven by the host.

Figure 5.19 Sustained Ultra DMA data out burst

5.6.4.9 Device pausing an Ultra DMA data out burst

5.6.4.2 contains the values for the timings for each of the Ultra DMA Modes.



Notes:

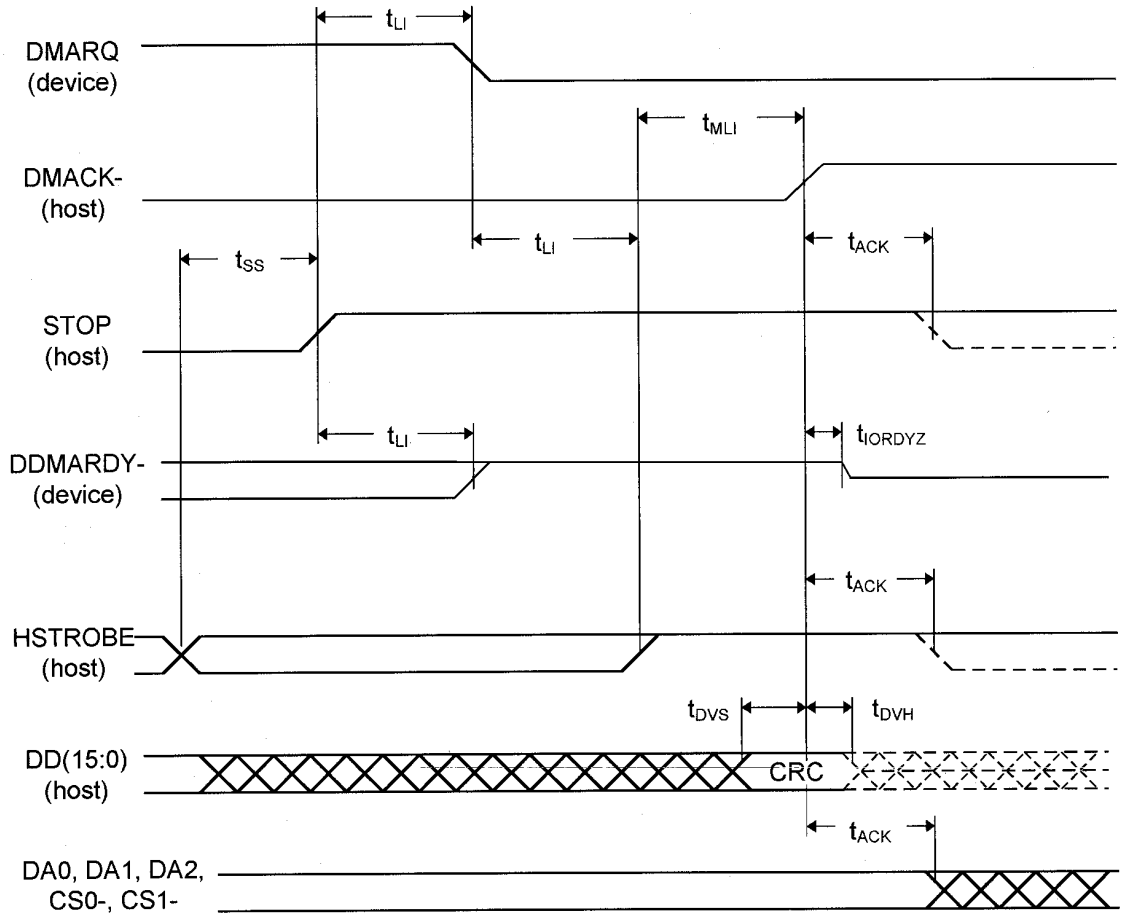
1) The device may negate DMARQ to request termination of the Ultra DMA burst no sooner than t_{RP} after DDMARDY- is negated.

2) If the t_{SR} timing is not satisfied, the device may receive zero, one or two more data words from the host.

Figure 5.20 Device pausing an Ultra DMA data out burst

5.6.4.10 Host terminating an Ultra DMA data out burst

5.6.4.2 contains the values for the timings for each of the Ultra DMA Modes.

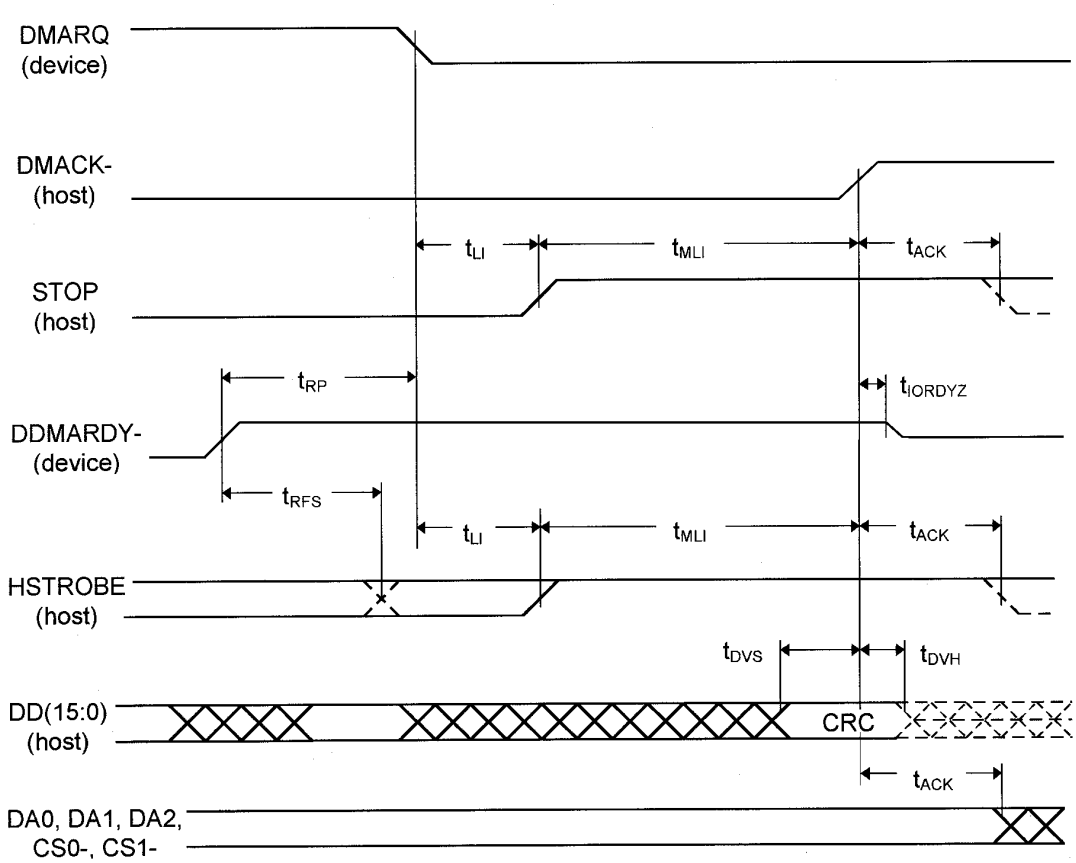


Note: The definitions for the STOP, DDMARDY- and HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

Figure 5.21 Host terminating an Ultra DMA data out burst

5.6.4.11 Device terminating an Ultra DMA data in burst

5.6.4.2 contains the values for the timings for each of the Ultra DMA Modes.



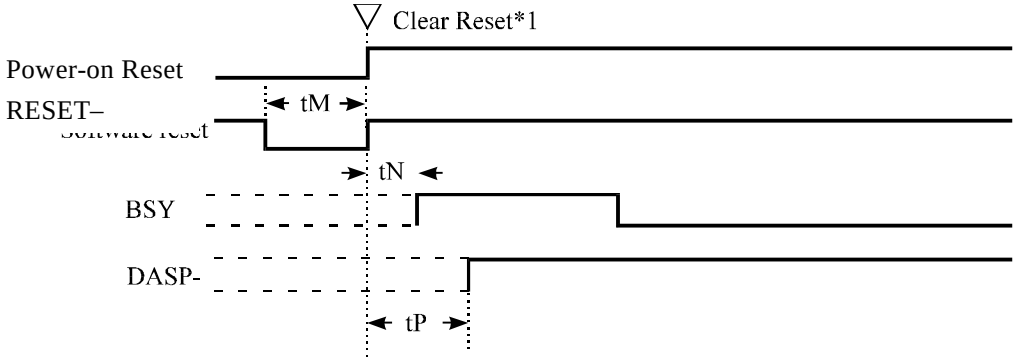
Note: The definitions for the STOP, DDMARDY- and HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

Figure 5.22 Device terminating an Ultra DMA data out burst

5.6.5 Power-on and reset

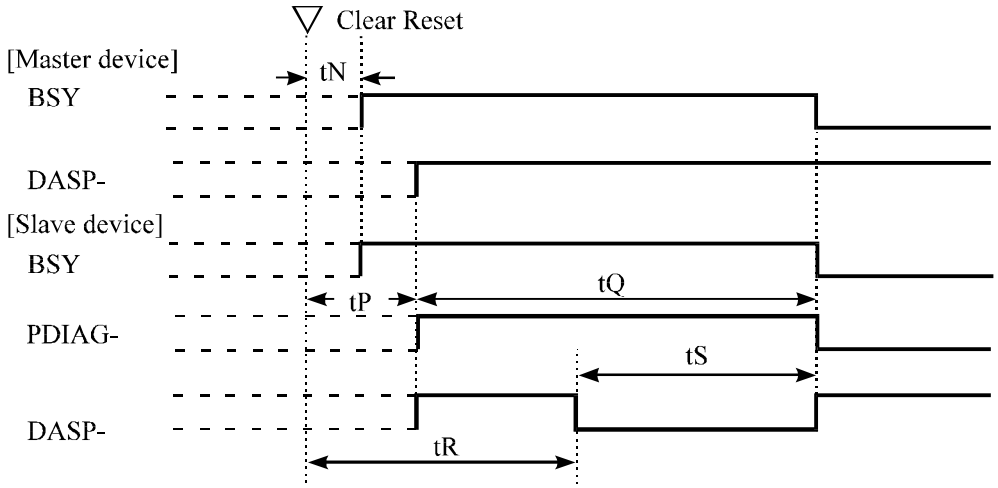
Figure 5.11 shows power-on and reset (hardware and software reset) timing.

(1) Only master device is present



*1: Reset means including Power-on-Reset, Hardware Reset (RESET-), and Software Reset.

(2) Master and slave devices are present (2-drives configulation)



Symbol	Timing parameter	Min.	Max.	Unit
tM	Pulse width of RESET-	25	—	µs
tN	Time from RESET- negation to BSY set	—	400	ns
tP	Time from RESET- negation to DASP- or PDIAG- negation	—	1	ms
tQ	Self-diagnostics execution time	—	15	s
tR	Time from RESET- negation to DASP- assertion (slave device)	—	400	ms
tS	Duration of DASP- assertion	—	31	s

Figure 5.23 Power on Reset Timing

CHAPTER 6 Operations

6.1 Device Response to the Reset

This section describes how the PDIAG- and DASP- signals responds when the power of the IDD is turned on or the IDD receives a reset or diagnostic command.

6.1.1 Response to power-on

After the master device (device 0) releases its own power-on reset state, the master device shall check a DASP- signal for up to 450 ms to confirm presence of a slave device (device 1). The master device recognizes presence of the slave device when it confirms assertion of the DASP- signal. Then, the master device checks a PDIAG- signal to see if the slave device has sucessfully completed the power-on diagnostics.

If the master device cannot confirm assertion of the DASP- signal within 450 ms, the master device recognizes that no slave device is connected.

After the slave device (device 1) releases its own power-on reset state, the slave device shall report its presence and the result of power-on diagnostics to the master device as described below:

DASP- signal: Asserted within 400 ms.

PDIAG- signal: Negated within 1 ms and asserted within 30 seconds.

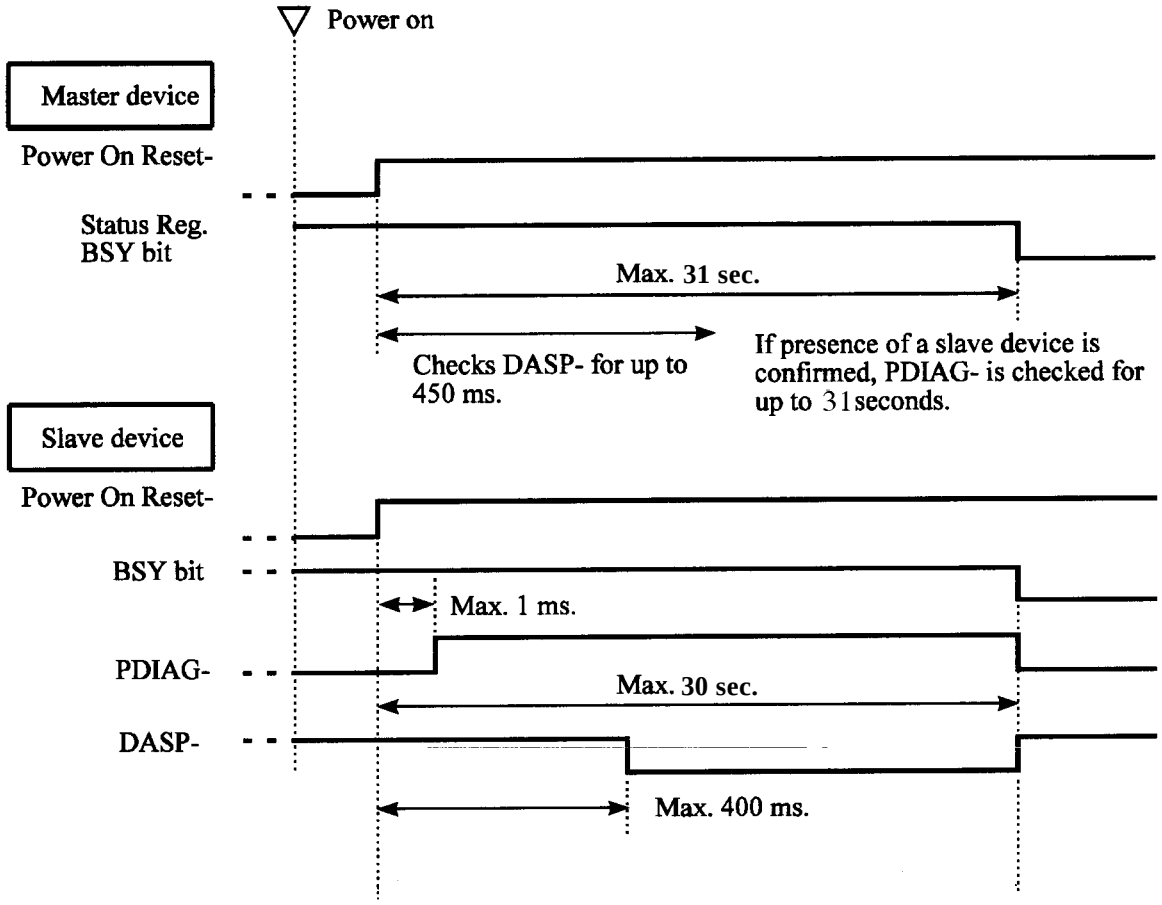


Figure 6.1 Response to power-on

6.1.2 Response to hardware reset

Response to RESET- (hardware reset through the interface) is similar to the power-on reset.

Upon receipt of hardware reset, the master device checks a DASP- signal for up to 450 ms to confirm presence of a slave device. The master device recognizes the presence of the slave device when it confirms assertion of the DASP- signal. Then the master device checks a PDIAG- signal to see if the slave device has successfully completed the self-diagnostics.

If the master device cannot confirm assertion of the DASP- signal within 450 ms, the master device recognizes that no slave device is connected.

After the slave device receives the hardware reset, the slave device shall report its presense and the result of the self-diagnostics to the master device as described below:

DASP- signal: Asserted within 400 ms.

PDIAG- signal: Negated within 1 ms and asserted within 30 seconds.

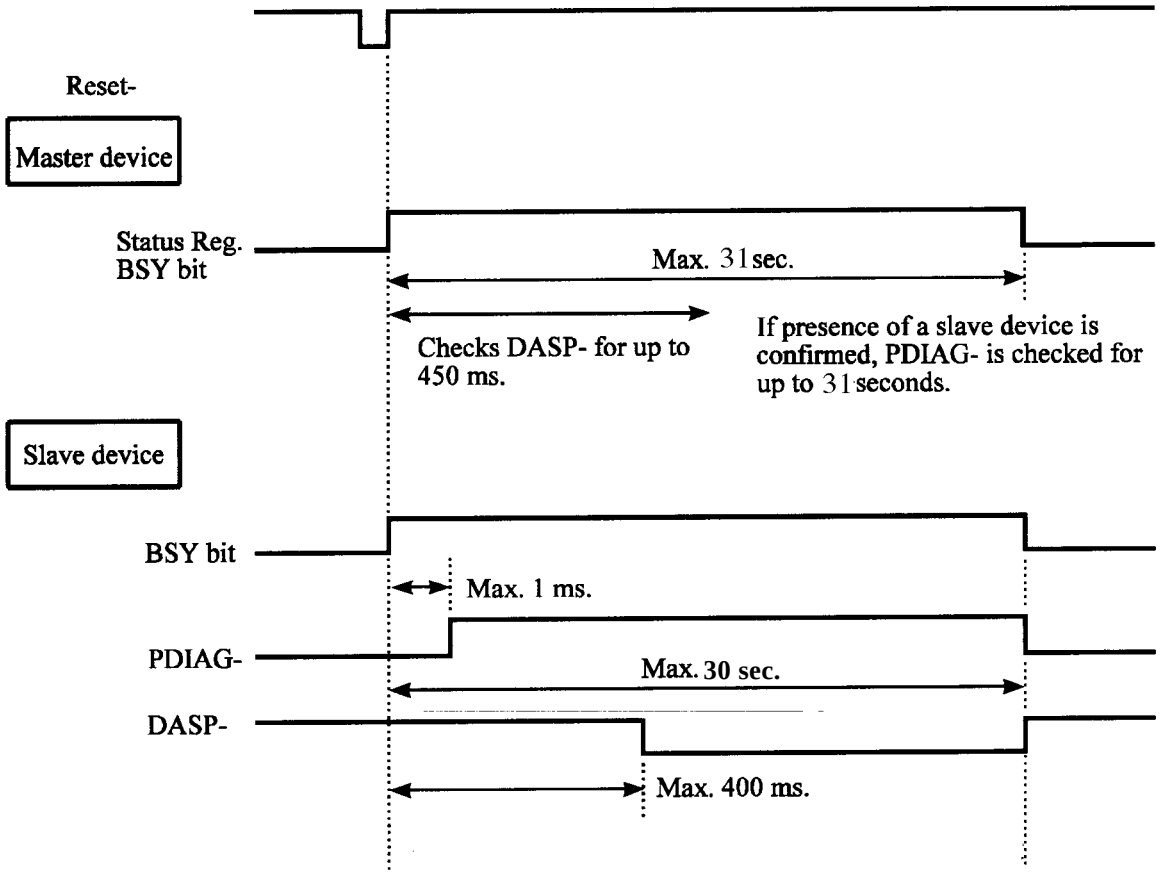


Figure 6.2 Response to hardware reset

6.1.3 Response to software reset

The master device does not check the DASP- signal for a software reset. If a slave device is present, the master device checks the PDIAG- signal for up to 15 seconds to see if the slave device has completed the self-diagnosis successfully.

After the slave device receives the software reset, the slave device shall report its presense and the result of the self-diagnostics to the master device as described below:

PDIAG- signal: negated within 1 ms and asserted within 30 seconds

When the IDD is set to a slave device, the IDD asserts the DASP- signal when negating the PDIAG- signal, and negates the DASP- signal when asserting the PDIAG- signal.

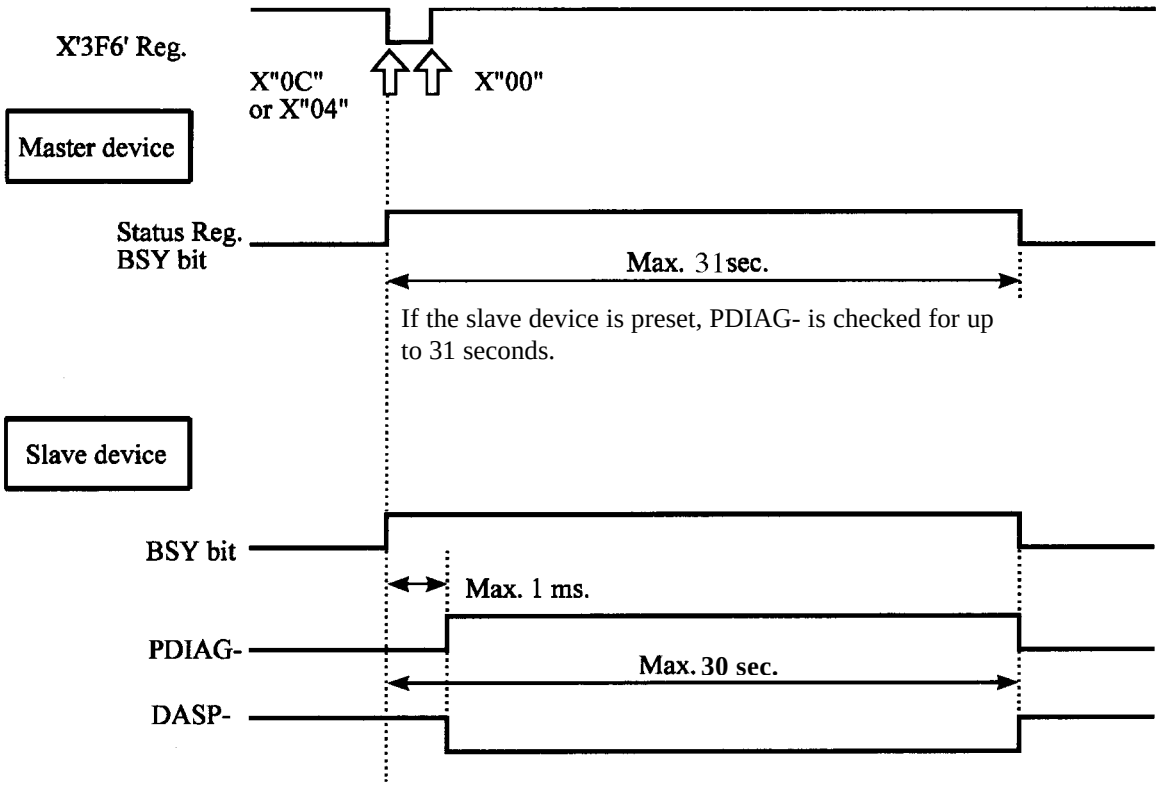


Figure 6.3 Response to software reset

6.1.4 Response to diagnostic command

When the master device receives an EXECUTE DEVICE DIAGNOSTIC command and the slave device is present, the master device checks the PDIAG- signal for up to 6 seconds to see if the slave device has completed the self-diagnosis successfully.

The master device does not check the DASP- signal.

After the slave device receives the EXECUTE DEVICE DIAGNOSTIC command, it shall report the result of the self-diagnostics to the master device as described below:

PDIAG- signal: negated within 1 ms and asserted within 5 seconds

When the IDD is set to a slave device, the IDD asserts the DASP- signal when negating the PDIAG- signal, and negates the DASP- signal when asserting the PDIAG- signal.

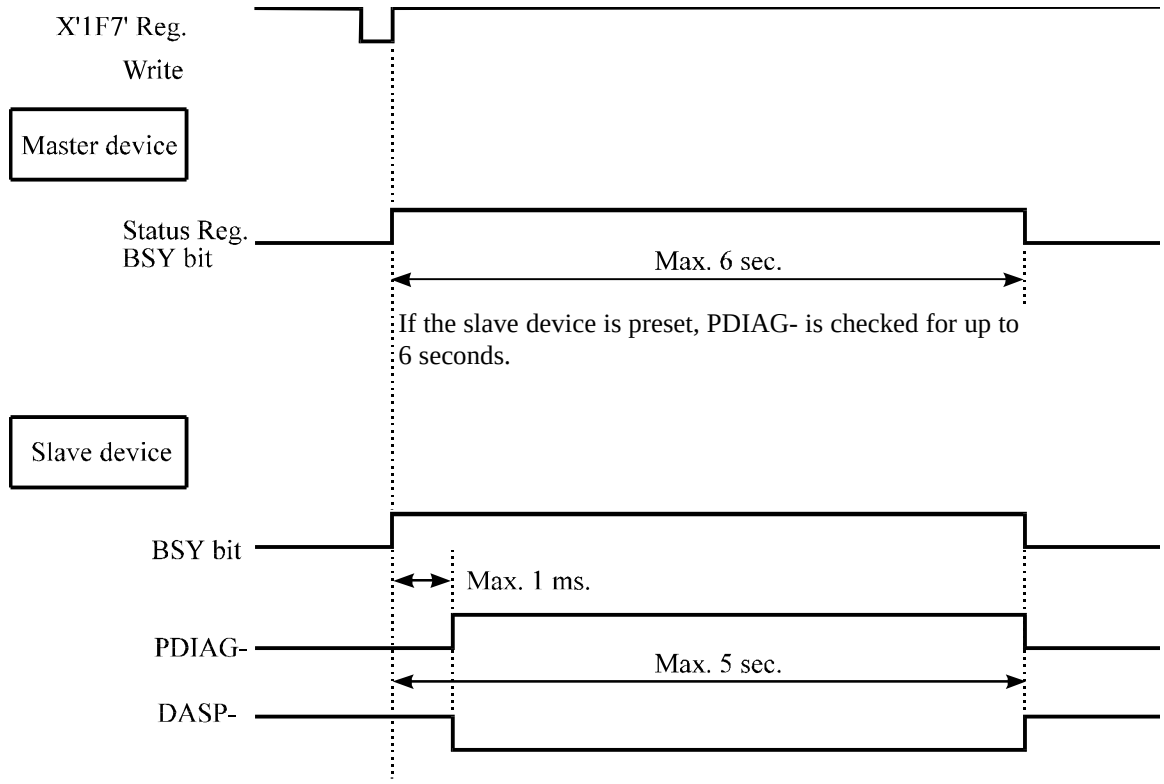


Figure 6.4 Response to diagnostic command

6.2 Address Translation

When the IDD receives any command which involves access to the disk medium, the IDD always implements the address translation from the logical address (a host-specified address) to the physical address (logical to physical address translation).

Following subsections explains the CHS translation mode.

6.2.1 Default parameters

In the logical to physical address translation, the logical cylinder, head, and sector addresses are translated to the physical cylinder, head, and sector addresses based on the number of heads and the number of sectors per track which are specified with an INITIALIZE DEVICE PARAMETERS command. This is called as the current translation mode.

If the number of heads and the number of sectors are not specified with an INITIALIZE DEVICE PARAMETERS command, the default values listed in Table 6.1 are used. This is called sa the default translation mode. The parameters in Table 6.1 are called BIOS specification.

Table 6.1 Default parameters

		MHC2032AT	MHC2040AT	MHD2021AT	MHD2032AT
Parameters (logical)	Number of cylinders	6,304	7,944	4,200	6,304
	Number of heads	16	16	16	16
	Number of sectors/track	63	63	63	63
Formatted capacity (MB)		3,253.4	4,099.8	2167.6	3253.4

As long as the formatted capacity of the IDD does not exceed the value shown on Table 6.1, the host can freely specify the number of cylinders, heads, and sectors per track.

Generally, the device recognizes the number of heads and sectors per track with the INITIALIZE DEVICE PARAMETER command. However, it cannot recognizes the number of cylinders. In other words, there is no way for the device to recognize a host access area on logical cylinders. Thus the host should manage cylinder access to the device.

The host can specify a logical address freely within an area where an address can be specified (within the specified number of cylinders, heads, and sectors per track) in the current translation mode.

The host can read an addressable parameter information from the device by the IDENTIFY DEVICE command (Words 54 to 56).

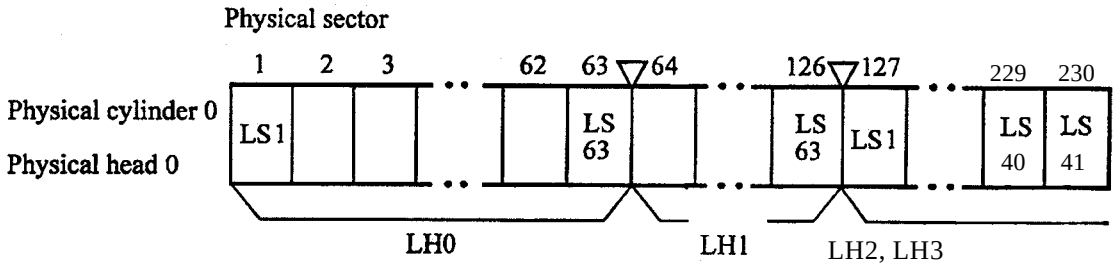
6.2.2 Logical address

(1) CHS mode

Logical address assignment starts from physical cylinder (PC) 0, physical head (PH) 0, and physical sector (PS) 1 and is assigned by calculating the number of sectors per track that is specified by the INITIALIZE DEVICE PARAMETERS command. If the last sector in a zone of a physical head is used, the track is switched and the next logical sector is placed in the initial sector in the same zone of the subsequent physical head.

After the last physical sector of the last physical head is used in the zone, the subsequent zone is used and logical sectors are assigned from physical head 0 in the same way.

Figure 6.5 shows an example of 6 heads configuration. (assuming there is no track skew).



ex: Zone 0 in 6-head device

Physical parameter
- Physical head : 0 to 5
- Physical sector : 1 to 230

Specifcation of INITIALIZE DEVICE PARAMETERS command
- Logical head : LH = 0 to 15
- Logical sector : LS = 1 to 63

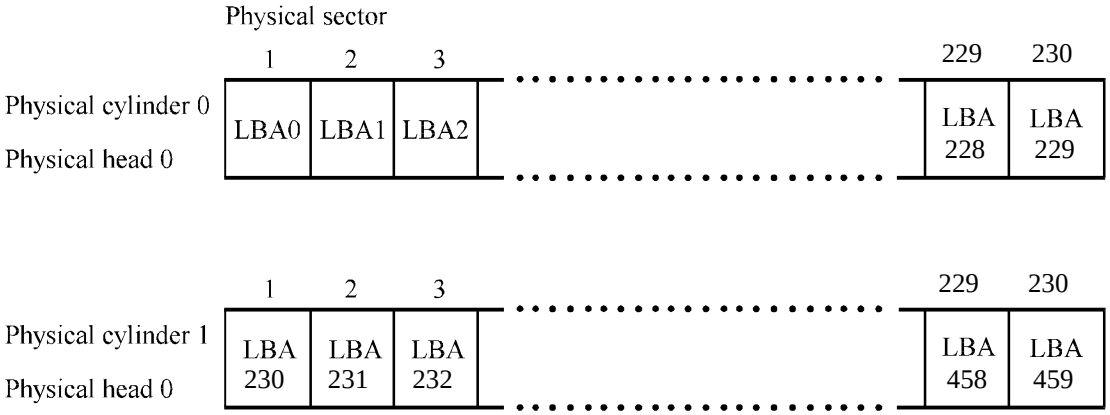
Figure 6.5 Address translation (example in CHS mode)

(2) LBA mode

Logical address assignment in the LBA mode starts from physical cylinder 0, physical head 0, and physical sector 1. If the last sector in a zone of a physical head is used, the track is switched and the next LBA is assigned to the initial sector in the same zone of the subsequent physical head.

After the last physical sector of the last physical head is used in the zone, the subsequent zone is used and LBA is assigned from physical head 0 in the same way.

Figure 6.6 shows an example of 4 heads configuration (assuming there is no track skew).



ex: Zone 0 in 6-head device

Physical parameter
– Physical head : 0 to 5
– Physical sector : 1 to 230

Figure 6.6 Address translation (example in LBA mode)

6.3 Power Save

The host can change the power consumption state of the device by issuing a power command to the device.

6.3.1 Power save mode

There are four types of power consumption state of the device including active mode where all circuits are active.

In the power save mode, power supplying to the part of the circuit is turned off. There are three types of power save modes:

- Idle mode

- Standby mode
- Sleep mode

The drive moves from the Active mode to the idle mode by itself.

Regardless of whether the power down is enabled, the device enters the idle mode. The device also enters the idle mode in the same way after power-on sequence is completed.

And, the automatic power-down is executed if no command is coming for 30 min. (default)

(1) Active mode

In this mode, all the electric circuit in the device are active or the device is under seek, read or write operation.

A device enters the active mode under the following conditions:

- A command other than power commands is issued.
- A reset command is received.

(2) Idle mode

In this mode, circuits on the device is set to power save mode.

The device enters the Idle mode under the following conditions:

- After completion of power-on sequence.
- After completion of the command execution other than SLEEP and STANDBY commands.
- After completion of the reset sequence

(3) Standby mode

In this mode, the VCM circuit is turned off and the spindle motor is stopped.

The device can receive commands through the interface. However if a command with disk access is issued, response time to the command under the standby mode takes longer than the active or Idle mode because the access to the disk medium cannot be made immediately.

The drive enters the standby mode under the following conditions:

- A STANDBY or STANDBY IMMEDIATE command is issued in the active or idle mode.
- When automatic power down sequence is enabled, the timer has elapsed.
- A reset is issued in the sleep mode.

When one of following commands is issued, the command is executed normally and the device is still stayed in the standby mode.

- Reset (hardware or software)
- STANDBY command
- STANDBY IMMEDIATE command
- INITIALIZE DEVICE PARAMETERS command
- CHECK POWER MODE command

(4) Sleep mode

The power consumption of the drive is minimal in this mode. The drive enters only the standby mode from the sleep mode. The only method to return from the standby mode is to execute a software or hardware reset.

The drive enters the sleep mode under the following condition:

- A SLEEP command is issued.

Issued commands are invalid (ignored) in this mode.

6.3.2 Power commands

The following commands are available as power commands.

- IDLE
- IDLE IMMEDIATE
- STANDBY
- STANDBY IMMEDIATE
- SLEEP
- CHECK POWER MODE

6.4 Defect Management

Defective sectors of which the medium defect location is registered in the system space are replaced with spare sectors in the formatting at the factory shipment.

All the user space area are formatted at shipment from the factory based on the default parameters listed in Table 6.1.

6.4.1 Spare area

Following two types of spare area are provided for every physical head.

1) Spare cylinder for sector slip:

   used for alternating defective sectors at formatting in shipment (4 cylinders)

2) Spare cylinder for alternative assignment:

   used for automatic alternative assignment at read error occurrence.
   (2 cylinders)

6.4.2 Alternating defective sectors

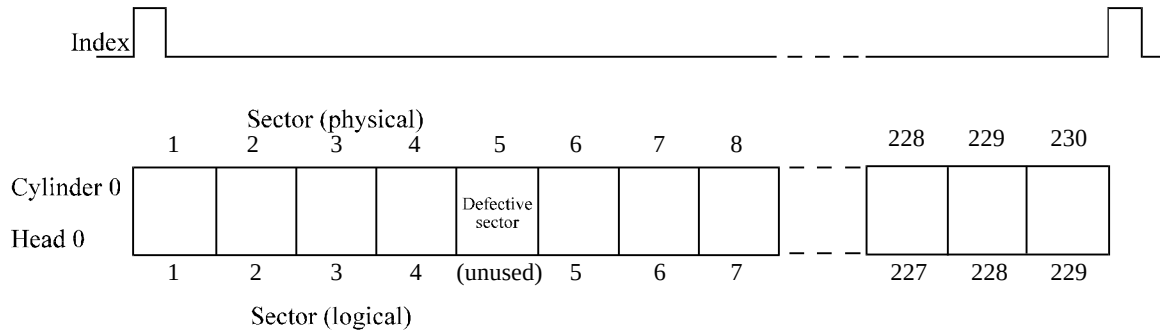
The two alternating methods described below are available:

(1) Sector slip processing

A defective sector is not used and is skipped and a logical sector address is assigned to the subsequent normal sector (physically adjacent sector to the defective sector).

When defective sector is present, the sector slip processing is performed in the formatting.

Figure 6.7 shows an example where (physical) sector 5 is defective on head 0 in cylinder 0.



Note: If an access request to physical sector 5 is specified, the device accesses physical sector 6 instead of sector 5.

Figure 6.7 Sector slip processing

(2) Alternate cylinder assignment

A defective sector is assigned to the spare sector in the alternate cylinder.

This processing is performed when the alternate assignment is specified in the FORMAT TRACK command or when the automatic alternate processing is performed at read error occurrence.

Figure 6.8 shows an example where (physical) sector 5 is detective on head 0 in cylinder 0.

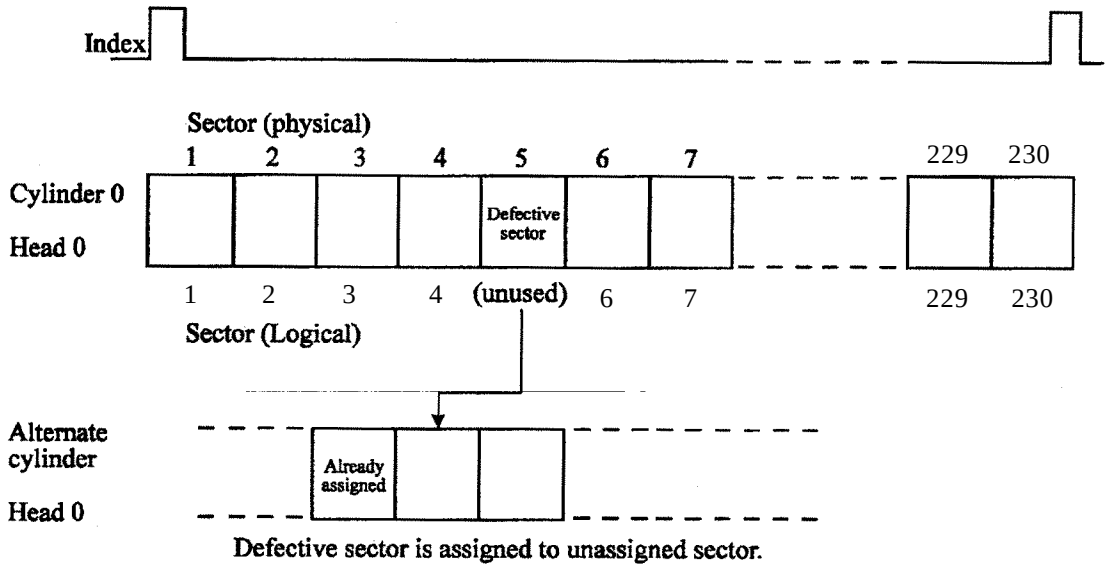


Figure 6.8 Alternate cylinder assignment

2 alternate cylinders are provided for each head in zone 12 (inner side).

When an access request to physical sector 5 is specified, the device accesses the alternated sector in the alternate cylinder instead of sector 5. When an access request to sectors next to sector 5 is specified, the device seeks to cylinder 0, head 0, and continues the processing.

(3) Automatic alternate assignment

The device performs the automatic alternate assignment when ECC correction performance is increased during read error retry, a read error is recovered. Before automatic alternate assignment, the device performs rewriting the corrected data to the erred sector and rereading. If no error occurs at rereading, the automatic alternate assignment is not performed.

An unrecoverable write error occurs during write error retry, automatic alternate assignment is performed.

6.5 Read-Ahead Cache

After read command which involes read data from the disk medium is completed, the read-ahead cache function reads the subsequent data blocks automatically and stores the data to the data buffer.

When the next command requests to read the read-ahead data, the data can be transferred from the data buffer without accessing the disk medium. The host can thus access data at higher speed.

6.5.1 Data buffer configuration

The drive has a 512-KB data buffer. The buffer is used by divided into three parts; for read commands, for write commands, and for MPU work (see Figure 6.9).

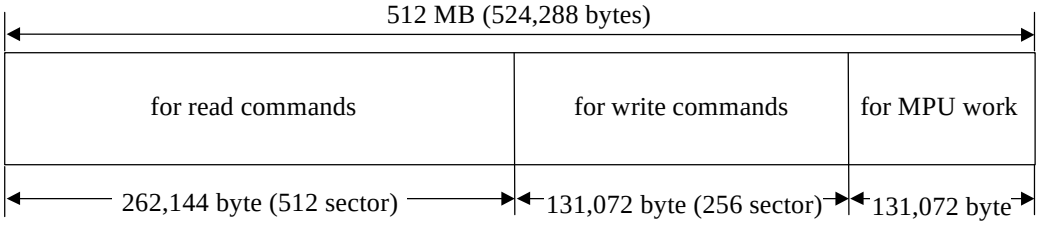


Figure 6.9 Data buffer configuration

The read-ahead operation is performed at execution of the READ SECTOR(S), READ MULTIPLE, or READ DMA command, and read-ahead data is stored in the buffer for read commands.

6.5.2 Caching operation

Caching operation is performed only at issurance of the following commands. The device transfers data from the data buffer to the host system at issurance of following command if following data exist in the data buffer.

- All sectors to be processed by the command
- A part of data including load sector to be processed by the command

When a part of data to be processed exist in the data buffer, remaining data are read from the medium and are transferred to the host system.

(1) Commands that are object of caching operation

Follow commands are object of caching operation.

- READ SECTOR (S)
- READ MULTIPLE
- READ DMA

When caching operation is disabled by the SET FEATURES command, no caching operation is performed.

(2) Data that are object of caching operation

Follow data are object of caching operation.

1) Read-ahead data read from the medium to the data buffer after completion of the command that are object of caching operation.

2) Data transferred to the host system once by requesting with the command that are object of caching operation (except for the cache invalid data by some reasons).

3) Remaining data in the data buffer (for write command) transferred from the host system by the command that writes data onto the disk medium, such as the WRITE SECTOR (S), WRITE DMA, WRITE MULTIPLE.

Followings are definition of in case that the write data is treated as a cache data. However, since the hit check at issurance of read command is performed to the data buffer for read command prioritily, caching write data is limited to the case that the hit check is missed at the data buffer for read command.

- When all data requested by the read command are stored in the data buffer for write command (hit all), the device transfers data from the data buffer for write command. At this time, the read-ahead operation to the data subsequent to the requested data is not performed.
- Even if a part of data requested by the read command are stored in the data buffer for write command (hit partially), all data are read from the disk medium without transferring from the data buffer for write command.

(3) Invalidating caching data

Caching data in the data buffer is invalidated in the following case.

1) Following command is issued to the same data block as caching data.
   - WRITE SECTOR(S)
   - WRITE DMA
   - WRITE MULTIPLE

2) Command other than following commands is issued (all caching data are invalidated)
   - READ SECTOR (S)
   - READ DMA

- READ MULTIPLE
- WRITE SECTOR(S)
- WRITE MULTIPLE
- WRITE VERIFY SECTOR(S)

3) Caching operation is inhibited by the SET FEATURES command.

4) Issued command is terminated with an error.

5) Soft reset or hard reset occurs, or power is turned off.

6) The device enters the sleep mode.

7) Under the state that the write data is kept in the data buffer for write command as a caching data, new write command is issued. (write data kept until now are invalidated)

6.5.3 Usage of read segment

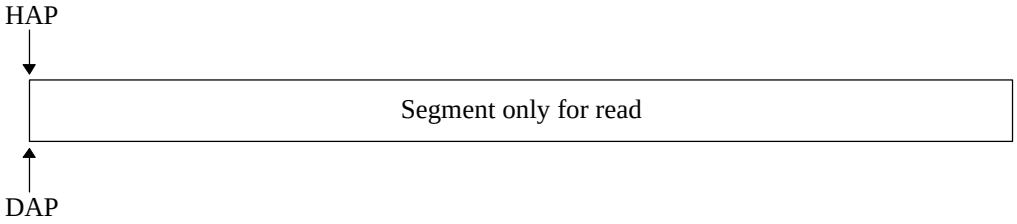
This subsection explains the usage of the read segment buffer at following cases.

6.5.3.1 Mis-hit (no hit)

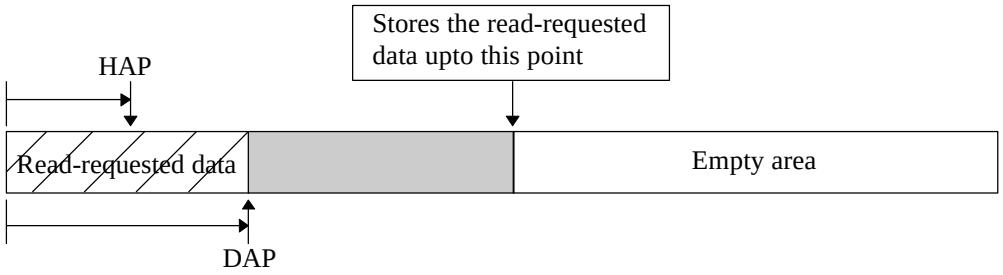
A lead block of the read-requested data is not stored in the data buffer. The requested data is read from the disk media.

The read-ahead operation is performed only when the last sector address of the previous read command and the lead sector address of this read command is sequential (see item (2)).

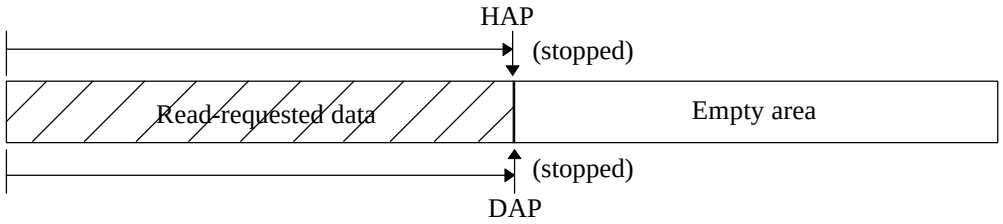
1) Sets the host address pointer (HAP) and the disk address pointer (DAP) to the lead of segment.



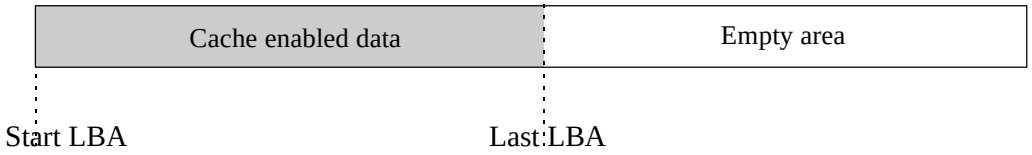
2) Transfers the requested data that already read to the host system with reading the requested data from the disk media.



3) After reading the requested data and transferring the requested data to the host system had been completed, the disk drive stops command execution without performing the read-ahead operation.



4) Following shows the cache enabled data for next read command.



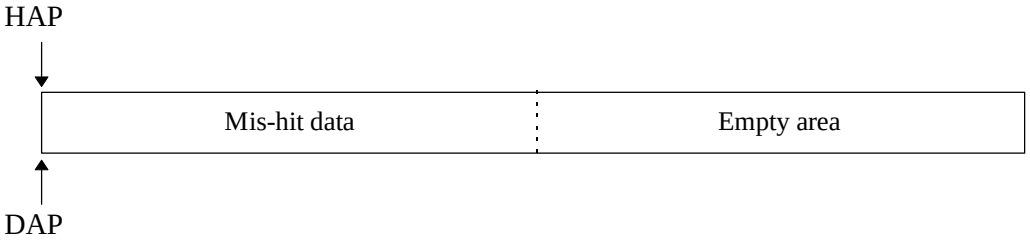
6.5.3.2 Sequential read

When the disk drive receives the read command that targets the sequential address to the previous read command, the disk drive starts the read-ahead operation.

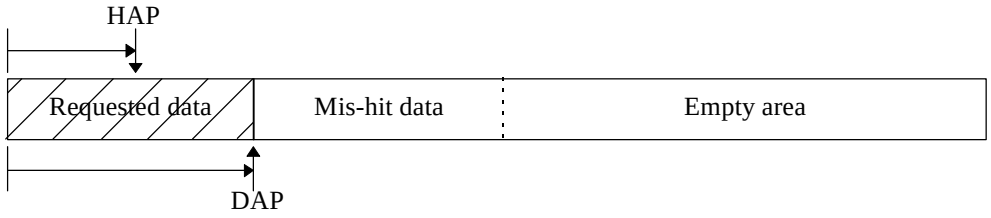
a. Sequential command just after non-sequential command

When the previously executed read command is an non-sequential command and the last sector address of the previous read command is sequential to the lead sector address of the received read command, the disk drive assumes the received command is a sequential command and performs the read-ahead operation after reading the requested data.

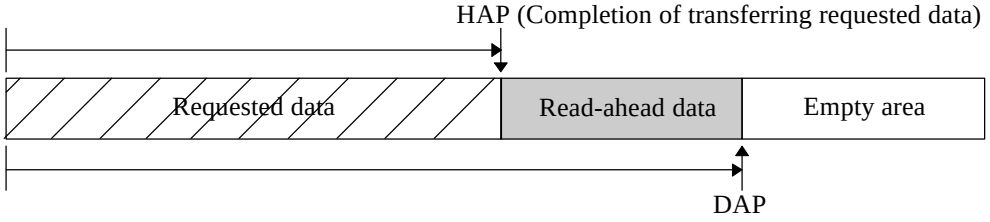
1) At receiving the sequential read command, the disk drive sets the DAP and HAP to the start address of the segment and reads the requested data from the load of the segment.



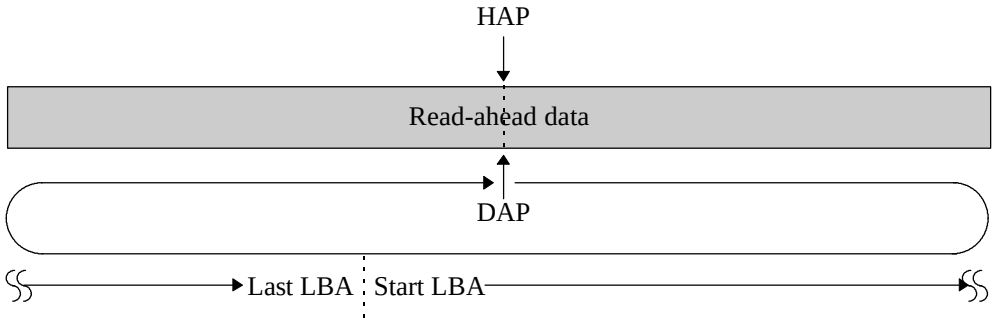
2) The disk drive transfers the requested data that is already read to the host system with reading the requested data.



3) After completion of the reading and transferring the requested data to the host system, the disk drive performs the read-ahead operation continuously.



4) The disk drive performs the read-ahead operation for all area of segment with overwriting the requested data. Finally, the cache data in the buffer is as follows.

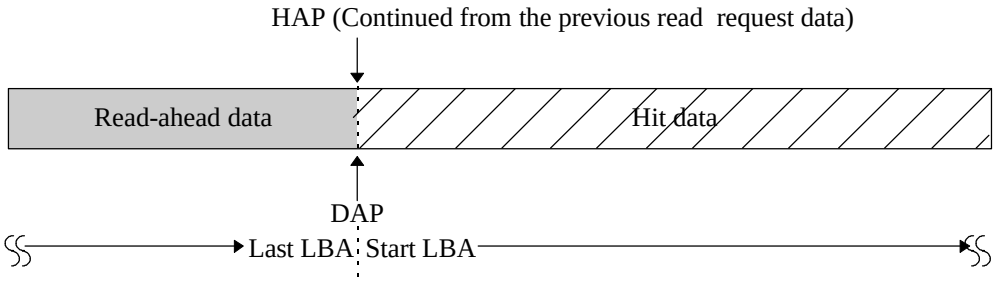


b. Sequential hit

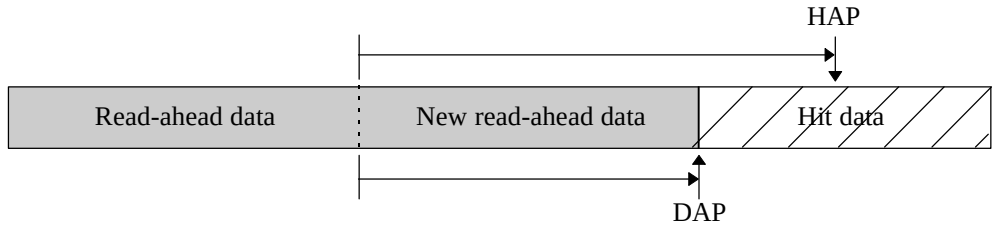
When the previously executed read command is the sequential command and the last sector address of the previous read command is sequential to the lead sector address of the received read command, the disk drive transfers the hit data in the buffer to the host system.

The disk drive performs the read-ahead operation of the new continuous data to the empty area that becomes vacant by data transfer at the same time as the disk drive starts transferring data to the host system.

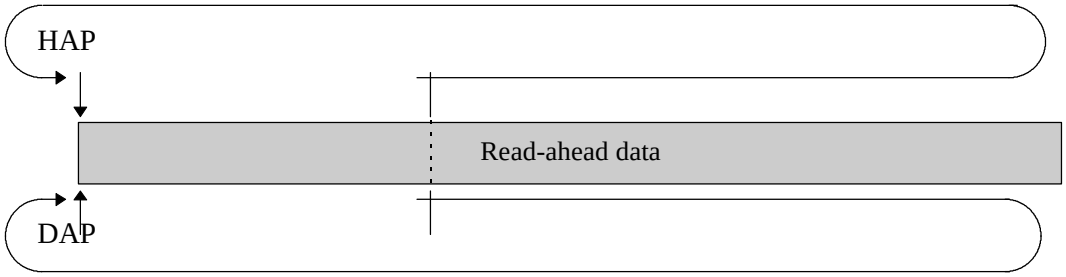
1) In the case that the contents of buffer is as follows at receiving a read command;



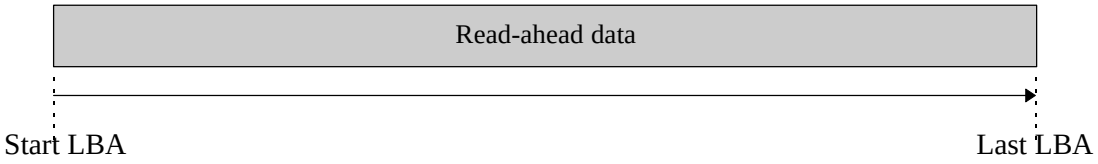
2) The disk drive starts the read-ahead operation to the empty area that becomes vacant by data transfer at the same time as the disk drive starts transferring hit data.



3) After completion of data transfer of hit data, the disk drive performs the read-ahead operation for the data area of which the disk drive transferred hit data.



4) Finally, the cache data in the buffer is as follows.



c. Non-sequential command immediately after sequential command

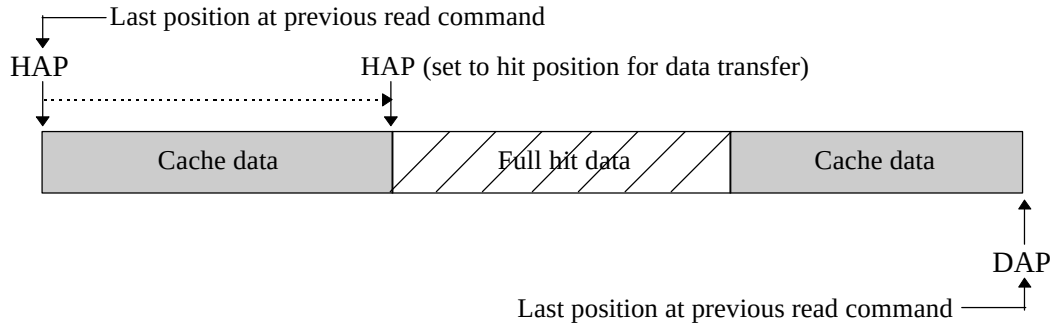
When a sequential read command (first read) has been executed, the first read operation should be stopped if a non-sequential read command has been received and then, ten or more of the non-sequential read commands have been received. (Refer to 6.5.3.1.)

The figure that describes the first read operation is the same as that shown in the sub-section a.

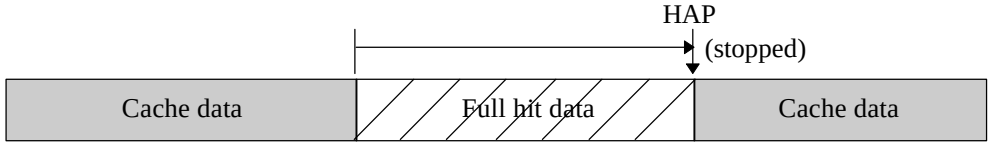
6.5.3.3 Full hit (hit all)

All requested data are stored in the data buffer. The disk drive starts transferring the requested data from the address of which the requested data is stored. After completion of command, a previously existed cache data before the full hit reading are still kept in the buffer, and the disk drive does not perform the read-ahead operation.

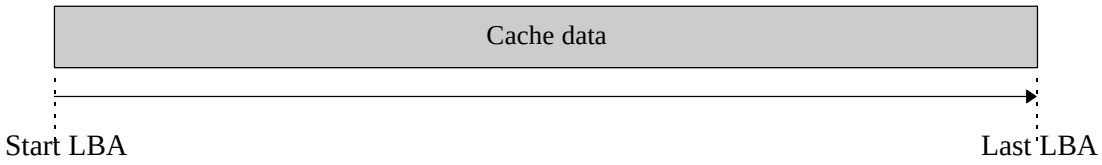
1) In the case that the contents of the data buffer is as follows for example and the previous command is a sequential read command, the disk drive sets the HAP to the address of which the hit data is stored.



2) The disk drive transfers the requested data but does not perform the read-ahead operation.



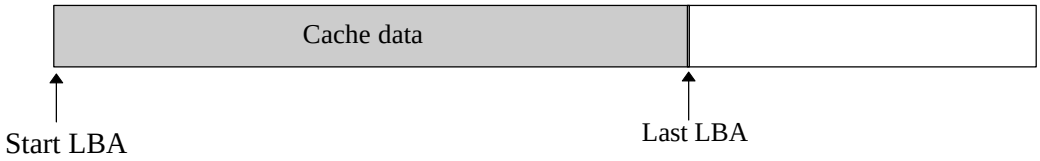
3) The cache data for next read command is as follows.



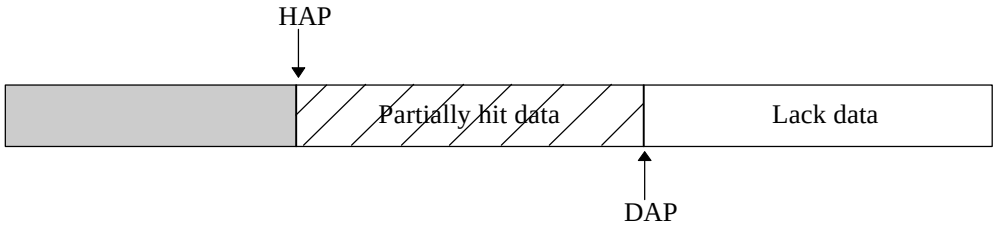
6.5.3.4 Partially hit

A part of requested data including a lead sector are stored in the data buffer. The disk drive starts the data transfer from the address of the hit data corresponding to the lead sector of the requested data, and reads remaining requested data from the disk media directly. The disk drive does not perform the read-ahead operation after data transfer.

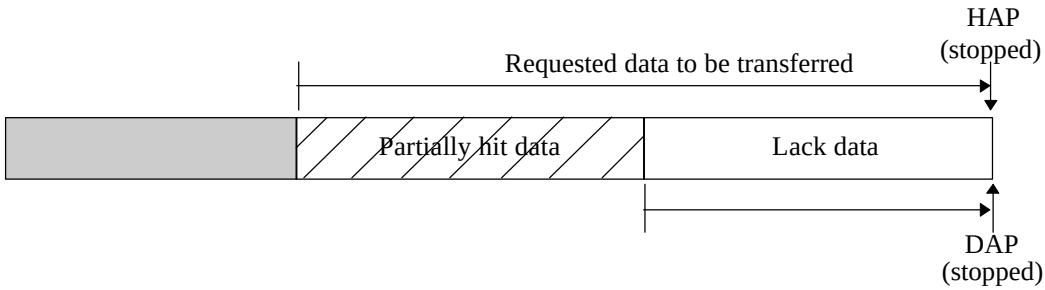
Following is an example of partially hit to the cache data.



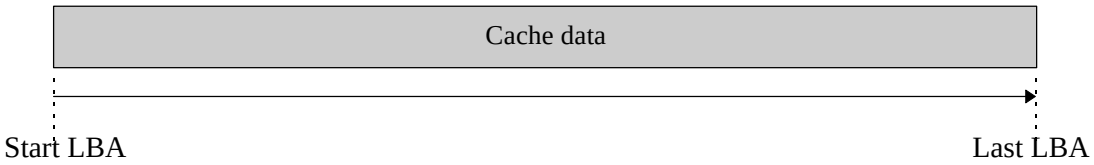
1) The disk drive sets the HAP to the address where the partially hit data is stored, and sets the DAP to the address just after the partially hit data.



2) The disk drive starts transferring partially hit data and reads lack data from the disk media at the same time. However, the disk drive does not perform the read-ahead operation newly.



3) The cache data for next read command is as follows.



6.6 Write Cache

The write cache function of the drive makes a high speed processing in the case that data to be written by a write command is physically sequent the data of previous command and random write operation is performed.

When the drive receives a write command, the drive starts transferring data of sectors requested by the host system and writing on the disk medium. After transferring data of sectors requested by the host system, the drive generates the interrupt of command complete. Also, the drive sets the normal end status in the Status register.

The drive continues writing data on the disk medium. When all data requested by the host are written on the disk medium, actual write operation is completed.

The drive receives the next command continuously. If the received command is a "sequential write" (data to be written by a command is physically sequent to data of previous command), the drive starts data transfer and receives data of sectors requested by the host system. At this time, if the write operation of the previous command is still been executed, the drive continuously executes the write operation of the next command from the sector next to the last sector of the previous write operation. Thus, the latency time for detecting a target sector of the next command is eliminated. This shortens the access time.

The drive generates an interrupt of command complete after completion of data transfer requested by the host system as same as at previous command.

When the write operation of the previous command had been completed, the latency time occurs to search the target sector.

If the received command is not a "sequential write", the drive receives data of sectors requested by the host system as same as "sequential write". The drive generates the interrupt of command complete after completion of data transfer requested by the host system. Received data is processed after completion of the write operation to the disk medium of the previous command.

Even if a hard reset or soft reset is received or the write cache function is disabled by the SET FEATURES command during unwritten data is kept, the instruction is not enabled until remaining unwritten data is written onto the disk medium.

The drive uses a cache data of the last write command as a read cache data. When a read command is issued to the same address after the write command (cache hit), the read operation to the disk medium is not performed.

If an error occurs during the write operation, the device retries the processing. If the error cannot be recovered by retry, automatic alternate assignment is performed. For details about automate alternate assignment, see item (3) of Section 6.4.2.

The write cache function is operated with the following command.

- WRITE SECTOR(S)
- WRITE MULTIPLE
- WRITE DMA (Ultra Write DMA)

IMPORTANT

When Write Cache is permitted, the writing of the data transferred from the host by the abovementioned Write Cache permit command into the disk medium may not be completed at the moment a normal ending interrupt has occurred.

In case a non-recoverable error has occurred during receiving more than one write command, it is difficult for the host to identify a command that caused the error.

(However, the error is not reported to the hose if an error at writing has been processed normally.)

Therefore, note that it is difficult for the host to retry an operation that caused a non-recoverable error.

Glossary

Actuator

Head positioning assembly. The actuator consists of a voice coil motor and head arm. If positions the read-write (R-W) head.

AT bus

A bus between the host CPU and adapter board

ATA (AT Attachment) standard

The ATA standard is for a PC AT interface regulated to establish compatibility between products manufactured by different vendors. Interfaces based on this standard are called ATA interfaces.

BIOS standard for drives

The BIOS standard collectively refers to the parameters defined by the host, which, for example, include the number of cylinders, the number of heads, and the number of sectors per track in the drive. The physical specifications of the drive do not always correspond to these parameters.

The BIOS of a PC AT cannot make full use of the physical specifications of these drivers. To make the best use of these drives, a BIOS that can handle the standard parameters of these drives is required.

Command

Commands are instructions to input data to and output data from a drive. Commands are written in command registers.

Data block

A data block is the unit used to transfer data. A data block normally indicates a single sector.

DE

Disk enclosure. The DE includes the disks, built-in spindle motor, actuator, heads, and air filter. The DE is sealed to protect these components from dust.

Master (Device 0)

The master is the first drive that can operate on the AT bus. The master is daisy-chained with the second drive which can operate in conformity with the ATA standard.

MTBF

Mean time between failures. The MTBF is calculated by dividing the total operation time (total power-on time) by the number of failures in the disk drive during operation.

MTTR

Mean time to repair. The MTTR is the average time required for a service person to diagnose and repair a faulty drive.

PIO (Programmed input-output)

Mode to transfer data under control of the host CPU

Positioning

Sum of the seek time and mean rotational delay

Power save mode

The power save modes are idle mode, standby mode, and sleep mode.

In idle mode, the drive is neither reading, writing, nor seeking data. In standby mode, the spindle motor is stopped and circuits other than the interface control circuit are sleeping. The drive enters sleep mode when the host issues the SLEEP command.

Reserved

Reserved bits, bytes, and fields are set to zero and unusable because they are reserved for future standards.

Rotational delay

Time delay due to disk rotation. The mean delay is the time required for half a disk rotation. The mean delay is the average time required for a head to reach a sector after the head is positioned on a track.

Seek time

The seek time is the time required for a head to move from the current track to another track. The seek time does not include the mean rotational delay.

Slave (Device 1)

The slave is a second drive that can operate on the AT bus. The slave is daisy-chained with the first drive operating in conformity with the ATA standard.

Status

The status is a piece of one-byte information posted from the drive to the host when command execution is ended. The status indicates the command termination state.

VCM

Voice coil motor. The voice coil motor is excited by one or more magnets. In this drive, the VCM is used to position the heads accurately and quickly.

Acronyms and Abbreviations

A

ABRT	Abored command
AIC	Automatic idle control
AMNF	Address mark not found
ATA	AT attachment
AWG	American wire gage

B

BBK	Bad block detected
BIOS	Basic input-output system

C

CORR	Corrected data
CH	Cylinder high register
CL	Cylinder low register
CM	Command register
CSR	Current sense register
CSS	Current start/stop
CY	Cylinder register

D

dBA	dB A-scale weighting
DE	Disk enclosure
DH	Device/head register
DRDY	Drive ready
DRQ	Ddata request bit
DSC	Drive seek complete
DWF	Drive write fault

E

ECC	Error checking and correction
ER	Error register
ERR	Error

F

FR	Feature register

H

HA	Host adapter
HDD	Hard disk drive

I

IDNF	ID not found
IRQ14	Interrupt request 14

L

LED	Light emitting diode

M

MB	Mega-byte
MB/S	Mega-byte per seconds
MPU	Micro processor unit

P

PCA	Printed circuit assembly
PIO	Programed input-output

R

RLL	Run-lrnght-limited

S

SA	System area
SC	Sector count register
SG	Signal ground
SN	Sector number register
ST	Status register

T

TPI	Track per inches
TRONF	Track 0 not found
Typ	Typical

U

UNC	Uncorrectable ECC error

V

VCM	Voice coil motor

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Comment Form

We would appreciate your comments and suggestions regarding this manual.

Manual code	C141-E050-02EN
Manual name	MHC2032AT, MHC2040AT, MHD2032AT, MHD2021AT DISK DRIVES PRODUCT MANUAL

Please mark each item: E(Excellent), G(Good), F(Fair), P(Poor).

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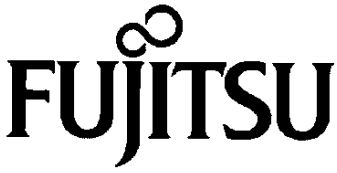
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