

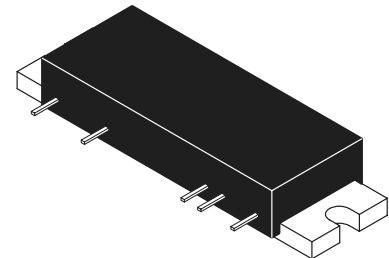
The RF Line
PCS Band
RF Linear LDMOS Amplifier

Designed for ultra-linear amplifier applications in 50 ohm systems operating in the PCS frequency band. A silicon FET Class A design provides outstanding linearity and gain. In addition, the excellent group delay and phase linearity characteristics are ideal for digital modulation systems, such as TDMA and CDMA.

- Third Order Intercept: 49.5 dBm Typ
- Power Gain: 29 dB Typ (@ f = 1960 MHz)
- Excellent Phase Linearity and Group Delay Characteristics
- Ideal for Feedforward Base Station Applications

MHL19936

1900–2000 MHz
 12 W, 29 dB
RF LINEAR LDMOS AMPLIFIER



CASE 301AY-01, STYLE 1

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	30	Vdc
RF Input Power	P_{in}	+16	dBm
Storage Temperature Range	T_{stg}	-40 to +100	$^\circ\text{C}$
Operating Case Temperature Range	T_C	-20 to +100	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($V_{DD} = 26$ Vdc, $T_C = 25^\circ\text{C}$; 50 Ω System)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current	I_{DD}	—	1.4	1.45	A
Power Gain (f = 1960 MHz)	G_p	28	29	30	dB
Gain Flatness (f = 1900–2000 MHz)	G_F	—	0.2	0.4	dB
Power Output @ 1 dB Comp. (f = 1950 MHz)	P_{1dB}	40	41	—	dBm
Input VSWR (f = 1900–2000 MHz)	$VSWR_{in}$	—	1.2:1	1.5:1	
Third Order Intercept (f1 = 1950 MHz, f2 = 1955 MHz)	ITO	49	49.5	—	dBm
Noise Figure (f = 2000 MHz)	NF	—	4.2	4.5	dB

TYPICAL CHARACTERISTICS

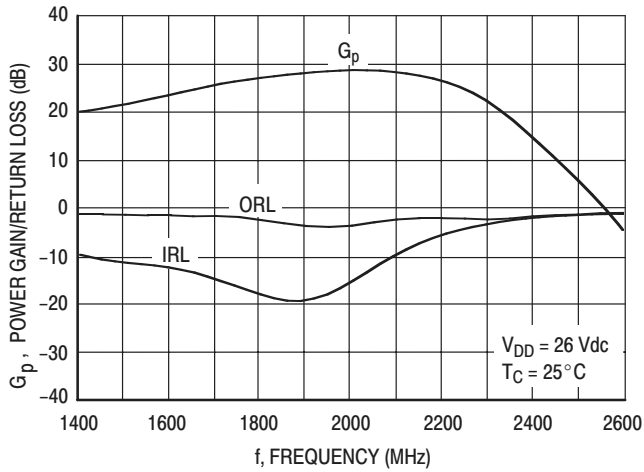


Figure 1. Power Gain, Input Return Loss, Output Return Loss versus Frequency

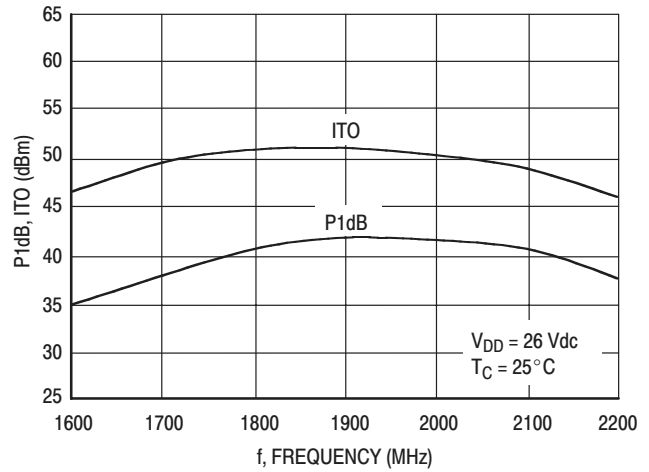


Figure 2. P1dB, ITO versus Frequency

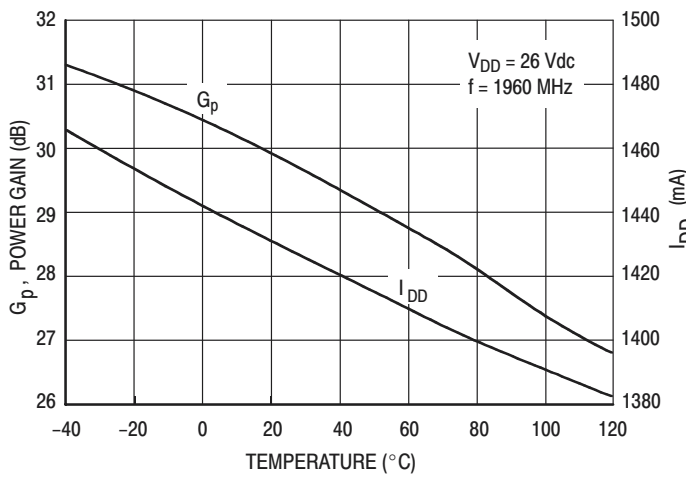


Figure 3. Power Gain, I_{DD} versus Temperature

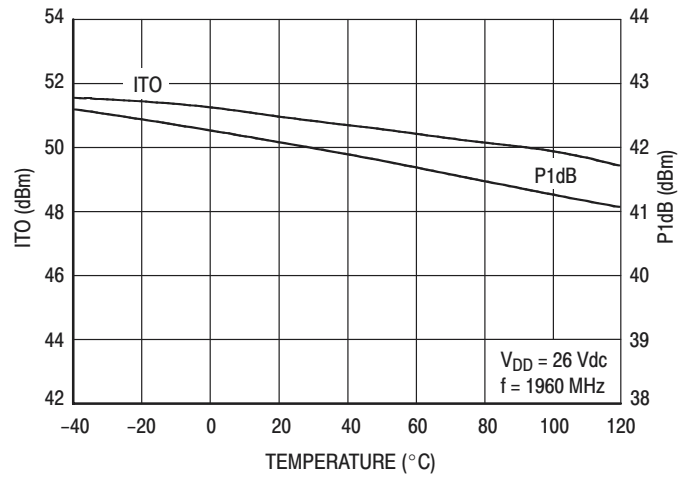


Figure 4. ITO, P1dB versus Temperature

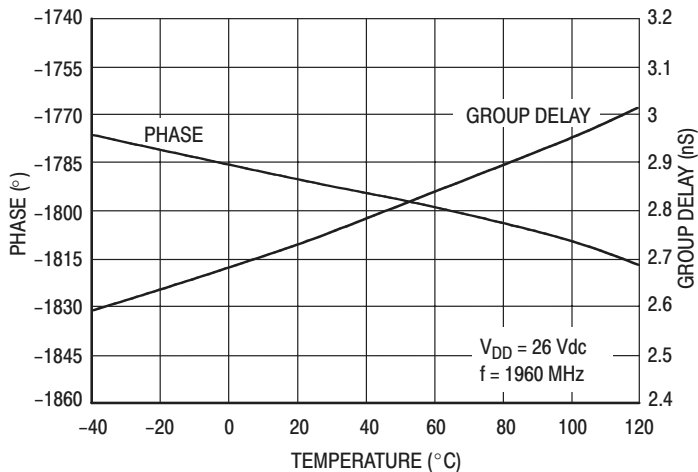


Figure 5. Phase⁽¹⁾, Group Delay⁽¹⁾ versus Temperature

⁽¹⁾In Production Test Fixture

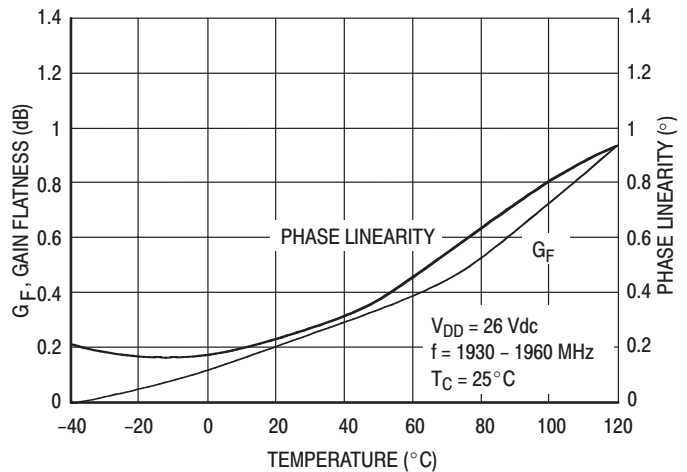


Figure 6. Gain Flatness, Phase Linearity versus Temperature

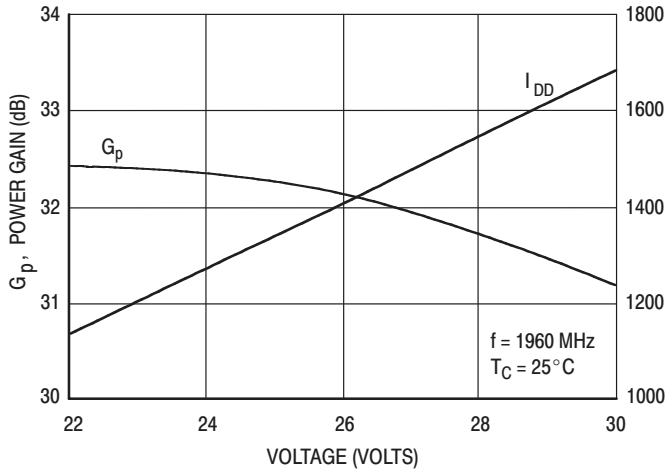


Figure 7. Power Gain, I_{DD} versus Voltage

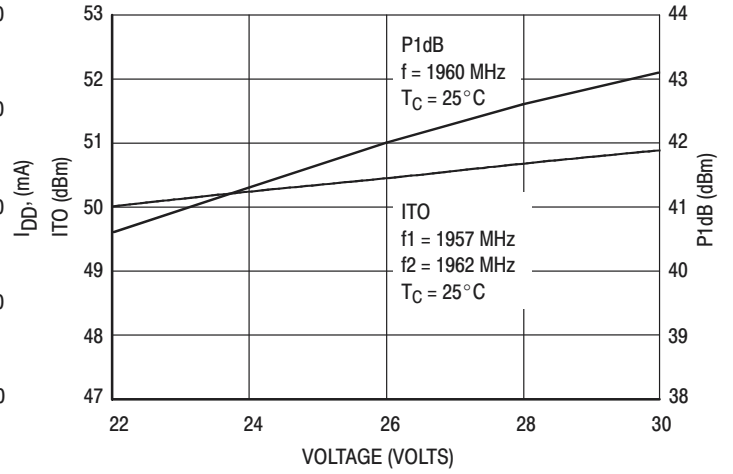


Figure 8. ITO, P1dB versus Voltage

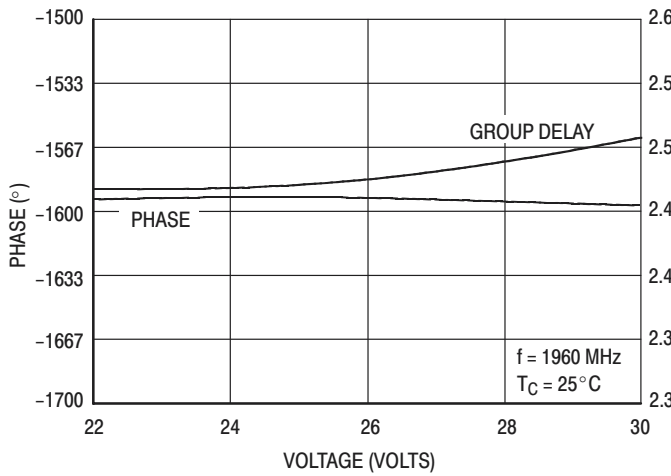


Figure 9. Phase⁽¹⁾, Group Delay⁽¹⁾ versus Voltage

⁽¹⁾In Production Test Fixture

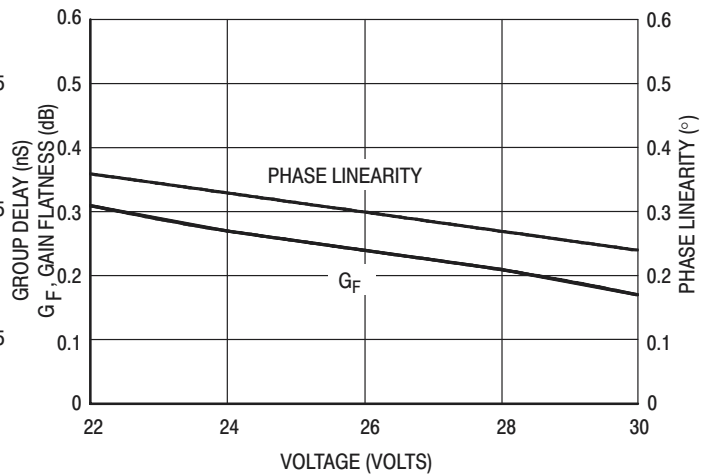
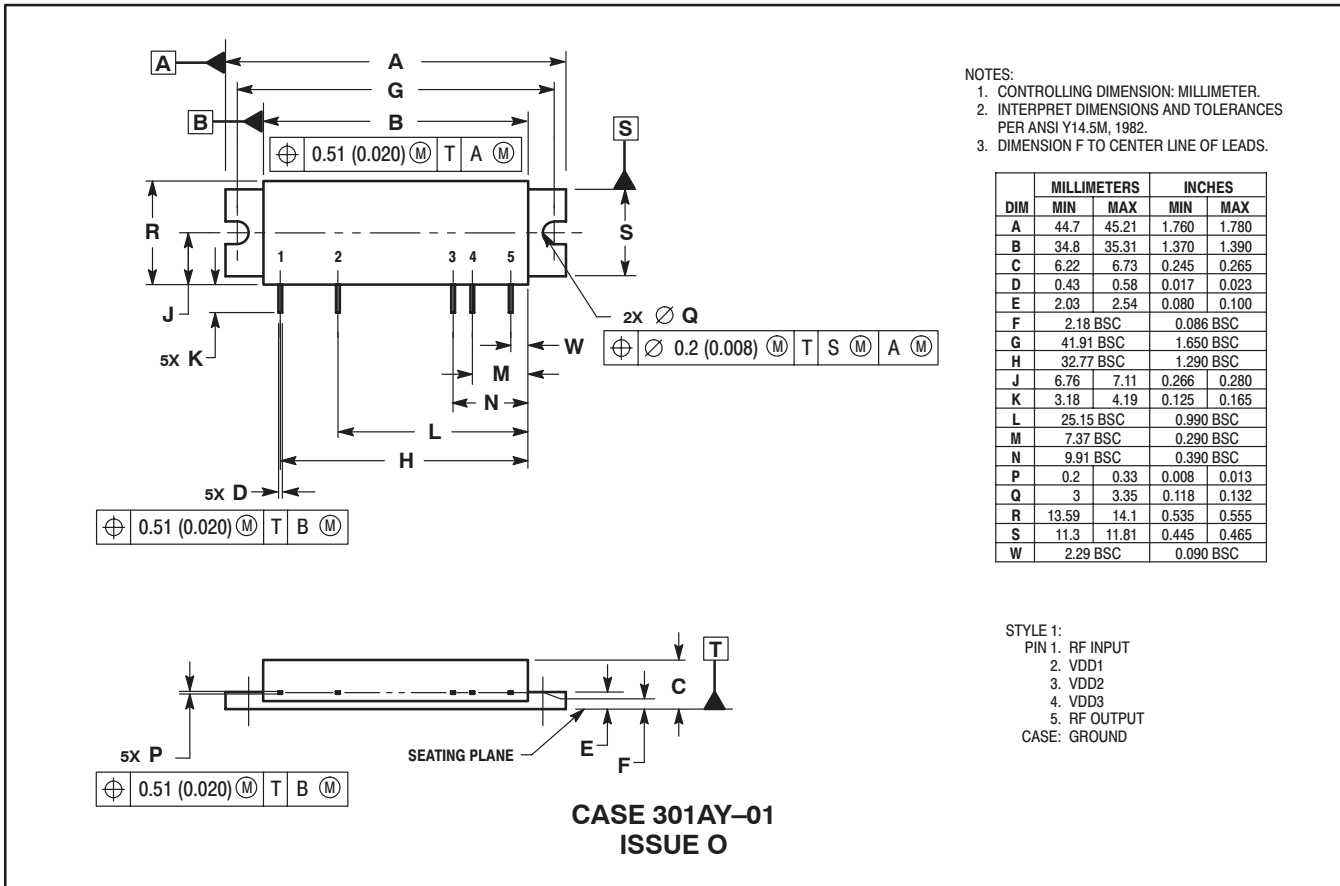


Figure 10. Phase Linearity, Gain Flatness versus Voltage

Freescale Semiconductor, Inc.

PACKAGE DIMENSIONS



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