

MHQ2369 (SILICON)

MPQ2369

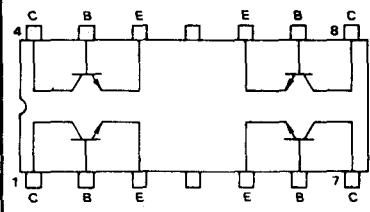
QUAD DUAL-IN-LINE NPN SILICON ANNULAR SWITCHING TRANSISTORS

... designed for low-current, high-speed switching and space saving applications.

- Choice of Ceramic or Plastic Package
- High Current-Gain-Bandwidth Product –
 $f_T = 550 \text{ MHz (Typ) @ } I_C = 10 \text{ mAdc}$
- Fast Switching Times – @ $V_{CC} = 3.0 \text{ Vdc}$
 $t_{on} = 9.0 \text{ ns (Typ)}$
 $t_{off} = 15 \text{ ns (Typ)}$
- Low Saturation Voltage –
 $V_{CE(sat)} = 0.25 \text{ Vdc (Max) @ } I_C = 10 \text{ mAdc}$
- Each Transistor Similar to 2N2369
- TO-116 Package – Compact Size Compatible With IC Automatic Insertion Equipment

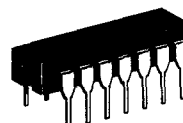
QUAD DUAL-IN-LINE NPN SILICON SWITCHING TRANSISTORS

CONNECTION DIAGRAM

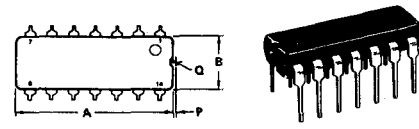
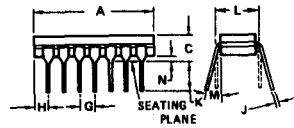
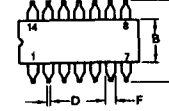


MAXIMUM RATINGS

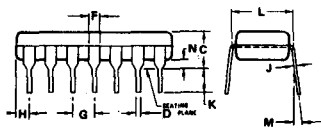
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	15	Vdc
Collector-Base Voltage	V_{CB}	40	Vdc
Emitter-Base Voltage	V_{EB}	4.5	Vdc
Collector Current – Peak	I_C	500	mAdc
		Each Transistor	Total Device
Total Device Dissipation @ $T_A = 25^\circ\text{C}$	P_D	0.5	1.5 Watts
Derate above 25°C	MHQ2369 MPQ2369	2.86 4.0	8.58 12 mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	MHQ2369 MPQ2369	T_J, T_{stg}	$-65 \text{ to } +200$ $-55 \text{ to } +150$ $^\circ\text{C}$



MHQ2369
CERAMIC
CASE 632-02
TO-116



MPQ2369
CASE 646
PLASTIC PACKAGE



DIM	MIN	MAX	MIN	MAX
A	18.18	19.80	0.715	0.740
B	6.10	6.60	0.240	0.260
C	4.98	4.57	0.198	0.180
D	0.38	0.61	0.015	0.020
E	1.02	1.52	0.040	0.060
F	2.54	8.52	0.100	0.335
G	1.27	1.83	0.052	0.072
H	0.20	0.30	0.008	0.012
I	2.82	3.43	0.115	0.135
J	7.37	7.81	0.290	0.310
K	—	1.02	—	0.040
L	0.51	1.02	0.020	0.040
M	0.13	0.36	0.005	0.015
N	0.51	0.76	0.020	0.030

- NOTES:
1. LEADS WITHIN 0.13 mm (0.006) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
 2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

DIM	MIN	MAX	MIN	MAX
A	18.9	19.9	0.680	0.785
B	5.59	7.11	0.220	0.280
C	—	5.08	—	0.200
D	0.381	0.584	0.015	0.023
F	0.77	1.77	0.030	0.070
G	2.54	BSC	0.100	BSC
J	0.203	0.381	0.008	0.015
K	2.54	—	0.100	—
L	7.62	BSC	0.300	BSC
M	—	15°	—	15°
N	0.51	0.78	0.020	0.030
P	—	8.25	—	0.325

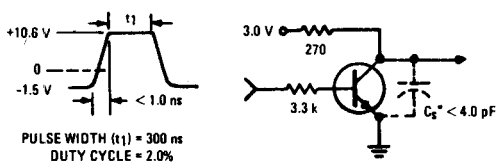
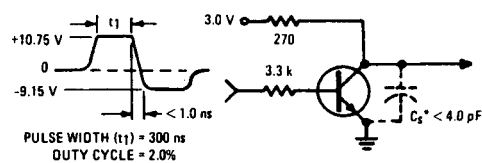
ALL JEDEC dimensions and notes apply.

NOTE:
DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage(1) ($I_C = 10\text{ mAdc}$, $I_B = 0$)	BV_{CEO}	15	—	—	Vdc
Collector-Base Breakdown Voltage ($I_C = 10\text{ }\mu\text{Adc}$, $I_E = 0$)	BV_{CBO}	40	—	—	Vdc
Emitter-Base Breakdown Voltage ($I_E = 10\text{ }\mu\text{Adc}$, $I_C = 0$)	BV_{EBO}	4.5	—	—	Vdc
Collector Cutoff Current ($V_{CB} = 20\text{ Vdc}$, $I_E = 0$)	I_{CBO}	—	—	0.4	μAdc
Emitter Cutoff Current ($V_{BE} = 3.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	0.5	μAdc
ON CHARACTERISTICS					
DC Current Gain(1) ($I_C = 10\text{ mAdc}$, $V_{CE} = 1.0\text{ Vdc}$) ($I_C = 100\text{ mAdc}$, $V_{CE} = 2.0\text{ Vdc}$)	h_{FE}	40 20	— —	— —	—
Collector-Emitter Saturation Voltage ($I_C = 10\text{ mAdc}$, $I_B = 1.0\text{ mAdc}$)	$V_{CE(sat)}$	—	—	0.25	Vdc
Base-Emitter Saturation Voltage ($I_C = 10\text{ mAdc}$, $I_B = 1.0\text{ mAdc}$)	$V_{BE(sat)}$	—	—	0.9	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain-Bandwidth Product (1) ($I_C = 10\text{ mAdc}$, $V_{CE} = 10\text{ Vdc}$, $f = 100\text{ MHz}$)	f_T	450	550	—	MHz
Output Capacitance ($V_{CB} = 5.0\text{ Vdc}$, $I_E = 0$, $f = 140\text{ kHz}$)	C_{ob}	—	2.5	4.0	pF
Input Capacitance ($V_{BE} = 0.5\text{ Vdc}$, $I_C = 0$, $f = 140\text{ kHz}$)	C_{ib}	—	3.0	5.0	pF
SWITCHING CHARACTERISTICS					
Turn-On Time ($V_{CC} = 3.0\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $I_C = 10\text{ mAdc}$, $I_{B1} = 3.0\text{ mAdc}$)	t_{on}	—	9.0	—	ns
Turn-Off Time ($V_{CC} = 3.0\text{ Vdc}$, $I_C = 10\text{ mAdc}$, $I_{B1} = 3.0\text{ mAdc}$, $I_{B2} = 1.5\text{ mAdc}$)	t_{off}	—	15	—	ns

(1) Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle = 2%.

SWITCHING TIME EQUIVALENT TEST CIRCUITS
FIGURE 1 — t_{on} CIRCUIT

FIGURE 2 — t_{off} CIRCUIT


*Total Shunt Capacitance of test jig and connectors.