

The Wideband IC Line

RF LDMOS Wideband Integrated Power Amplifier

The MHVIC2115R2 wideband integrated circuit is designed for base station applications. It uses Motorola's newest High Voltage (26 to 28 Volts) LDMOS IC technology and integrates a multi-stage structure. Its wideband On-Chip matching design makes it usable from 1600 to 2600 MHz. The linearity performances cover W-CDMA modulation formats.

Final Application

Typical W-CDMA Performance: -45 dBc ACPR, 2110-2170 MHz, $V_{DD} = 27$ Volts, $I_{DQ1} = 56$ mA, $I_{DQ2} = 61$ mA, $I_{DQ3} = 117$ mA, $P_{out} = 34$ dBm, 3GPP Test Model 1, Measured in a 1.0 MHz BW @ 4 MHz offset, 64 DTCH
 Power Gain — 30 dB
 PAE = 16%

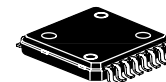
Driver Application

Typical W-CDMA Performance: -53 dBc ACPR, 2110-2170 MHz, $V_{DD} = 26$ Volts, $I_{DQ1} = 96$ mA, $I_{DQ2} = 204$ mA, $I_{DQ3} = 111$ mA, $P_{out} = 23$ dBm, 3GPP Test Model 1, Measured in a 3.84 MHz BW @ 5 MHz offset, 64 DTCH
 Power Gain — 34 dB

- Gain Flatness = 0.3 dB from 2110-2170 MHz
- P1dB = 15 Watts, Gain Flatness = 0.2 dB from 2110-2170 MHz
- Capable of Handling 3:1 VSWR, @ 26 Vdc, 2140 MHz, 15 Watts CW Output Power
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- On-Chip Matching (50 Ohm Input, DC Blocked, >5 Ohm Output)
- Integrated Temperature Compensation with Enable/Disable Function
- Integrated ESD Protection
- In Tape and Reel. R2 Suffix = 1,500 Units per 16 mm, 13 inch Reel.

MHVIC2115R2

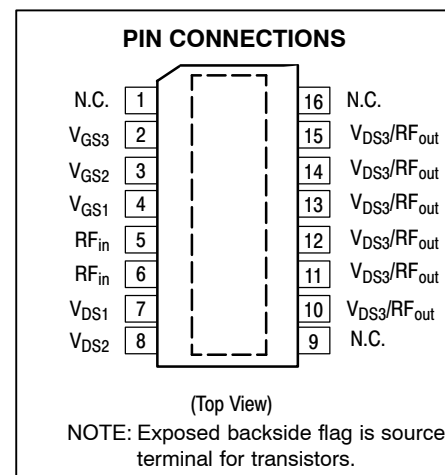
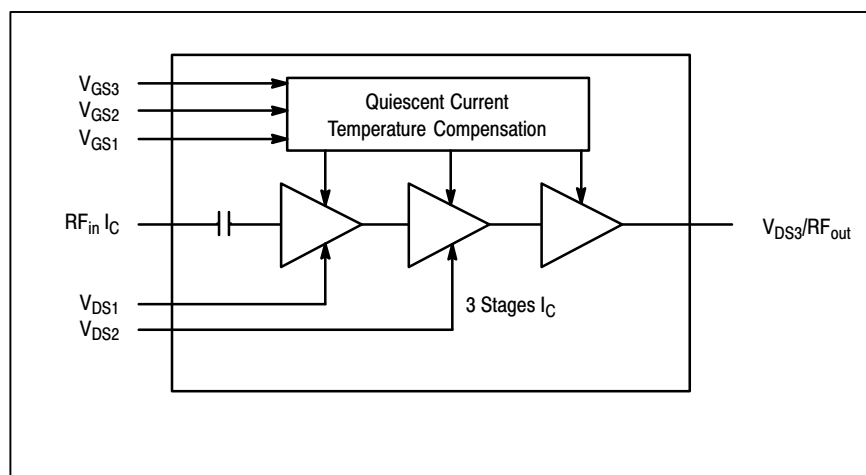
2170 MHz, 26 V, 23/34 dBm
 W-CDMA
 RF LDMOS WIDEBAND
 INTEGRATED POWER AMPLIFIER



CASE 978-03
 PFP-16

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Storage Temperature Range	T_{stg}	- 65 to +150	°C
Operating Junction Temperature	T_J	150	°C



(1) Refer to AN1987/D, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to <http://www.motorola.com/semiconductors/rf>. Select Documentation/Application Notes - AN1987.

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THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$		$^{\circ}C/W$
Driver Application ($P_{out} = +0.2 W CW$)	Stage 1, 26 Vdc, $I_{DQ} = 96 mA$ Stage 2, 26 Vdc, $I_{DQ} = 204 mA$ Stage 3, 26 Vdc, $I_{DQ} = 111 mA$	3.5	
Output Application ($P_{out} = +2.5 W CW$)	Stage 1, 27 Vdc, $I_{DQ} = 56 mA$ Stage 2, 27 Vdc, $I_{DQ} = 61 mA$ Stage 3, 27 Vdc, $I_{DQ} = 117 mA$	2.7	

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M1 (Minimum)
Charge Device Model	C2 (Minimum)

MOISTURE SENSITIVITY LEVEL

Test Methodology	Rating
Per JESD 22-A113	3

ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}C$ unless otherwise noted)

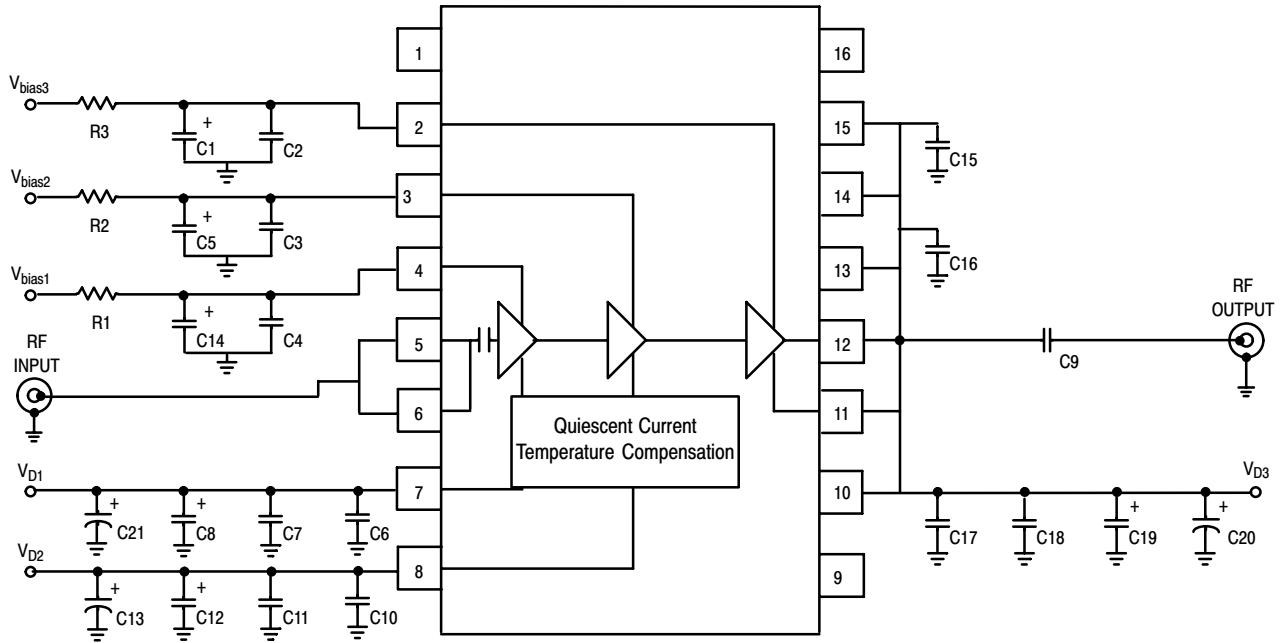
Characteristic	Symbol	Min	Typ	Max	Unit
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W-CDMA CHARACTERISTICS (In Motorola Test Fixture, 50 ohm system) $V_{DD} = 26 Vdc$, $I_{DQ1} = 96 mA$, $I_{DQ2} = 204 mA$, $I_{DQ3} = 111 mA$, $P_{out} = 23 dBm$, 2110-2170 MHz

Power Gain	G_{ps}	31	34	—	dB
Gain Flatness	G_F	—	0.3	0.5	dB
Input Return Loss	IRL	—	-12	-10	dB
Group Delay	—	—	1.7	—	ns
Phase Linearity	—	—	0.2	—	$^{\circ}$
1-Carrier W-CDMA Conditions: Adjacent Channel Power Ratio @ $P_{out} = 23 dBm$, 5 MHz Offset	ACPR	—	-53	-50	dBc
1-Carrier W-CDMA Conditions: Adjacent Channel Power Ratio @ $P_{out} = 28 dBm$, 5 MHz Offset	ACPR	—	-50	—	dBc

W-CDMA CHARACTERISTICS (In Motorola Test Fixture, 50 ohm system) $V_{DD} = 27 Vdc$, $I_{DQ1} = 56 mA$, $I_{DQ2} = 61 mA$, $I_{DQ3} = 117 mA$, $P_{out} = 34 dBm$, 2110-2170 MHz

Power Gain	G_{ps}	—	30	—	dB
Gain Flatness	G_F	—	0.2	—	dB
Input Return Loss	IRL	—	-12	—	dB
Power Added Efficiency	PAE	—	16	—	%
1-Carrier W-CDMA Conditions: Adjacent Channel Power Ratio @ $P_{out} = 34 dBm$, 4 MHz Offset	ACPR	—	-45	—	dBc



- | | | | |
|---------------------------|---|---------------|---|
| C1, C5, C8, C12, C14, C19 | 1 μ F SMT Tantalum Chip Capacitors | C13, C20, C21 | 330 μ F Electrolytic Capacitors (MCR35V337M10X16) |
| C2, C3, C4, C7, C11, C18 | 0.01 μ F Chip Capacitors (0805C103K5RACTR) | R1, R2, R3 | 1 k Ω Chip Resistors (0805) |
| C6, C10, C17 | 6.8 pF Chip Capacitors, ACCU-P (AVX 08051J6R8BBT) | PCB | Arlon, 0.020", $\epsilon_r = 2.55$ |
| C9, C15, C16 | 1.8 pF Chip Capacitors, ACCU-P (AVX 08051J1R8BBT) | | |

Figure 1. MHVIC2115R2 Demo Board Schematic

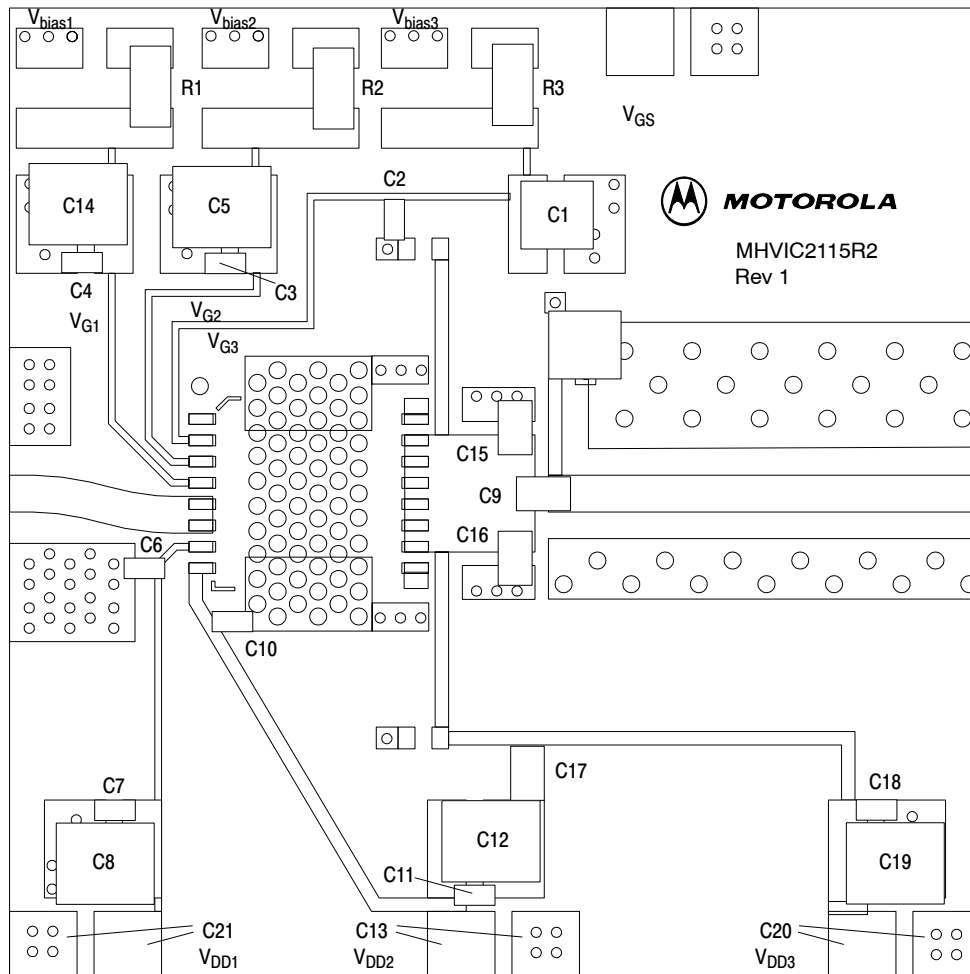


Figure 2. MHVIC2115R2 Demo Board Component Layout

TYPICAL CHARACTERISTICS

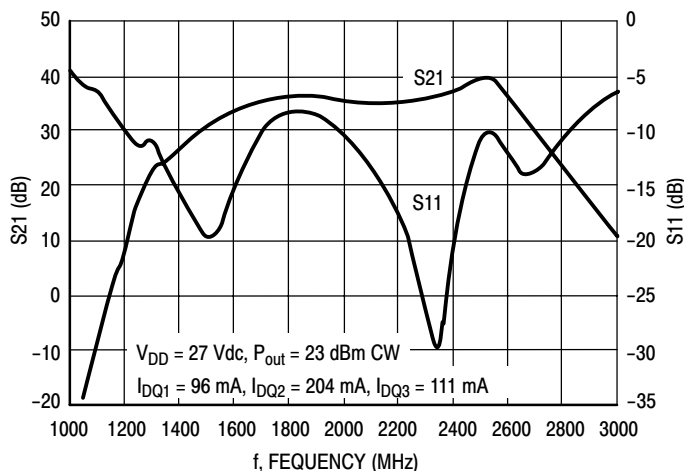


Figure 3. Broadband Frequency Response

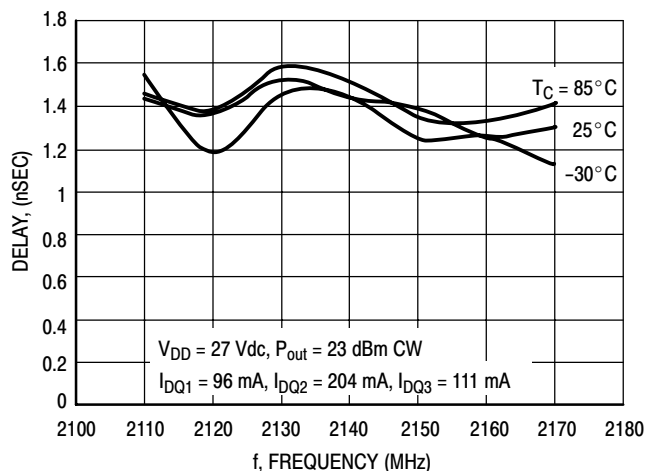


Figure 4. Delay versus Frequency

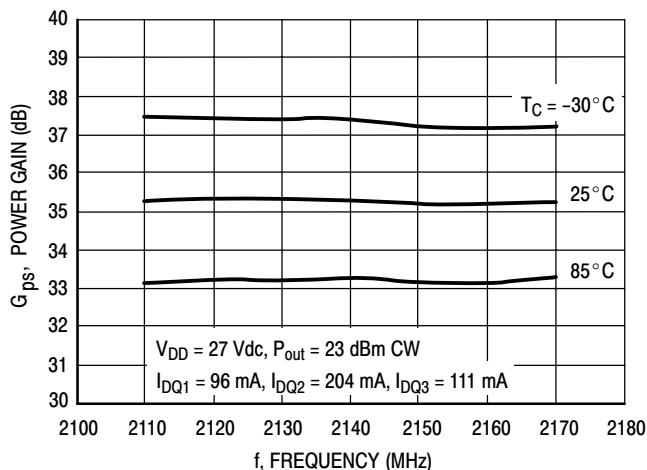


Figure 5. Power Gain versus Frequency

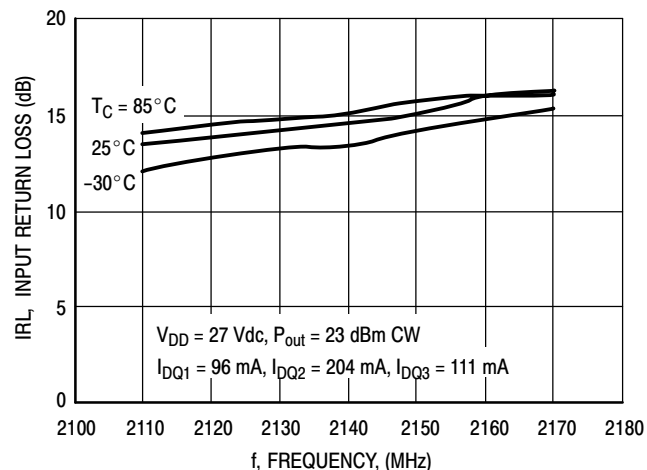


Figure 6. Input Return Loss versus Frequency

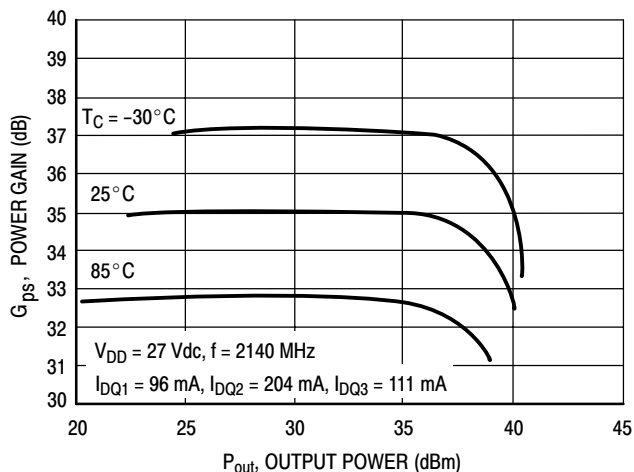


Figure 7. Power Gain versus Output Power

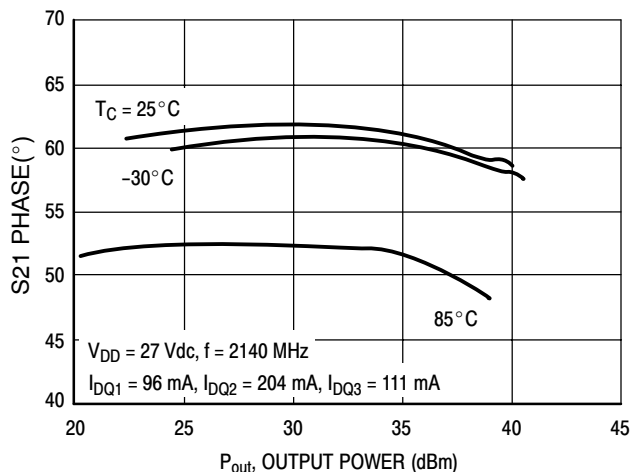


Figure 8. S21 Phase versus Output Power

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TYPICAL CHARACTERISTICS

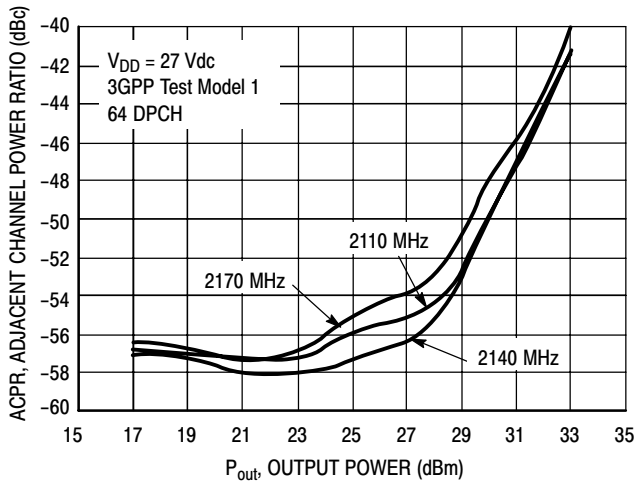


Figure 9. W-CDMA ACPR versus Output Power

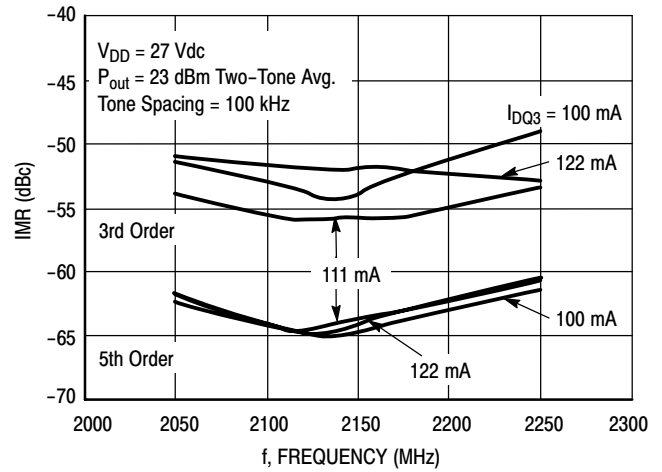


Figure 10. Two-Tone IMR versus Frequency

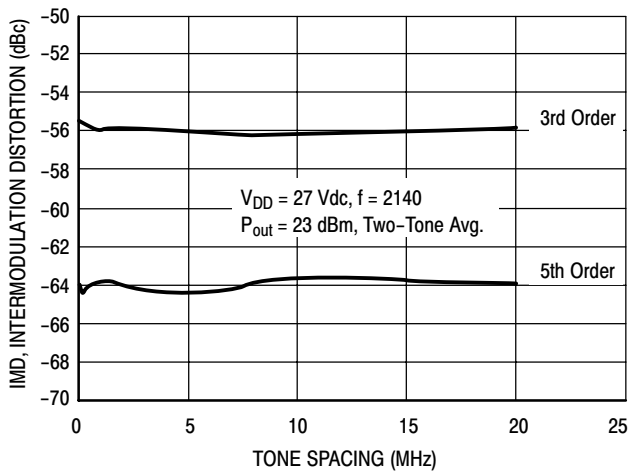


Figure 11. Two-Tone Broadband Performance

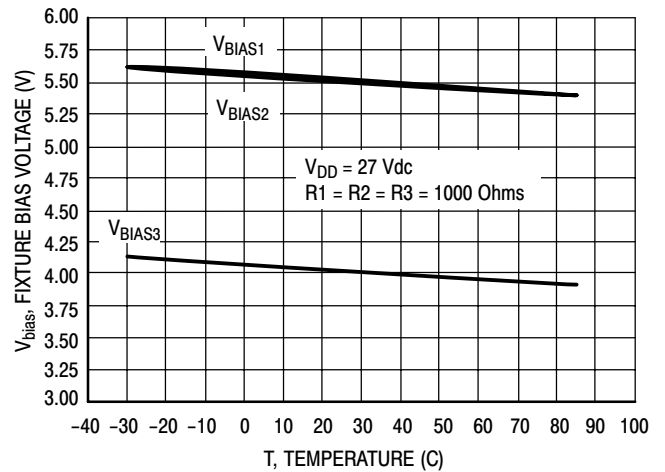


Figure 12. Fixture Bias versus Temperature

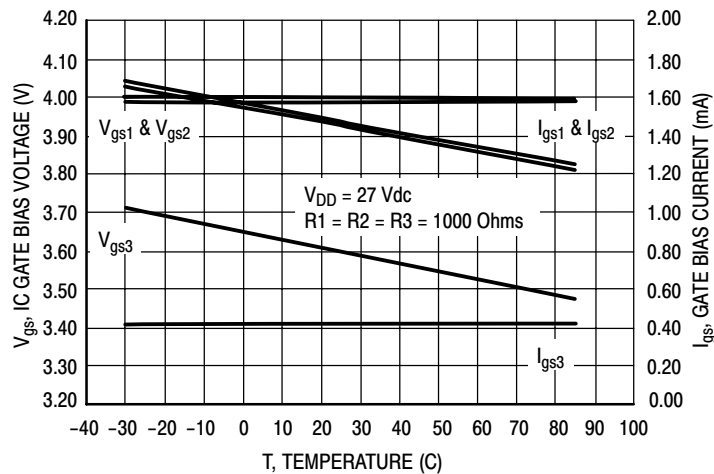
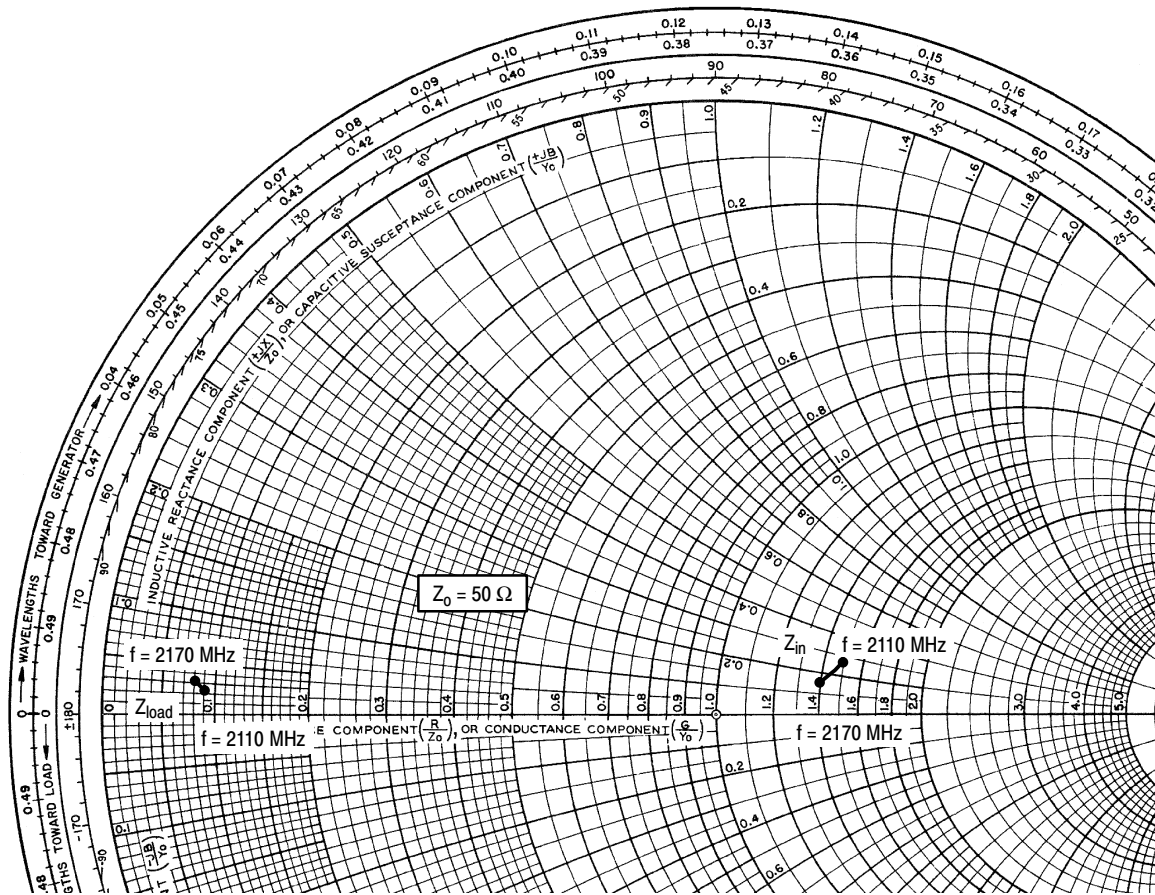


Figure 13. Gate Bias versus Temperature



$V_{DD} = 27 \text{ Vdc}$, $I_{DQ} = 1411 \text{ mA}$, $P_{out} = 15 \text{ W Avg.}$

f MHz	Z_{in} Ω	Z_{load} Ω
2110	$72.55 + j12.8$	$4.25 + j1.00$
2140	$71.40 + j9.9$	$4.13 + j1.37$
2170	$70.20 + j7.1$	$4.12 + j1.46$

Z_{in} = Device input impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

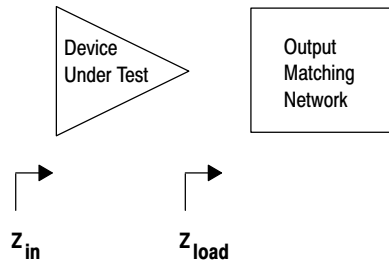
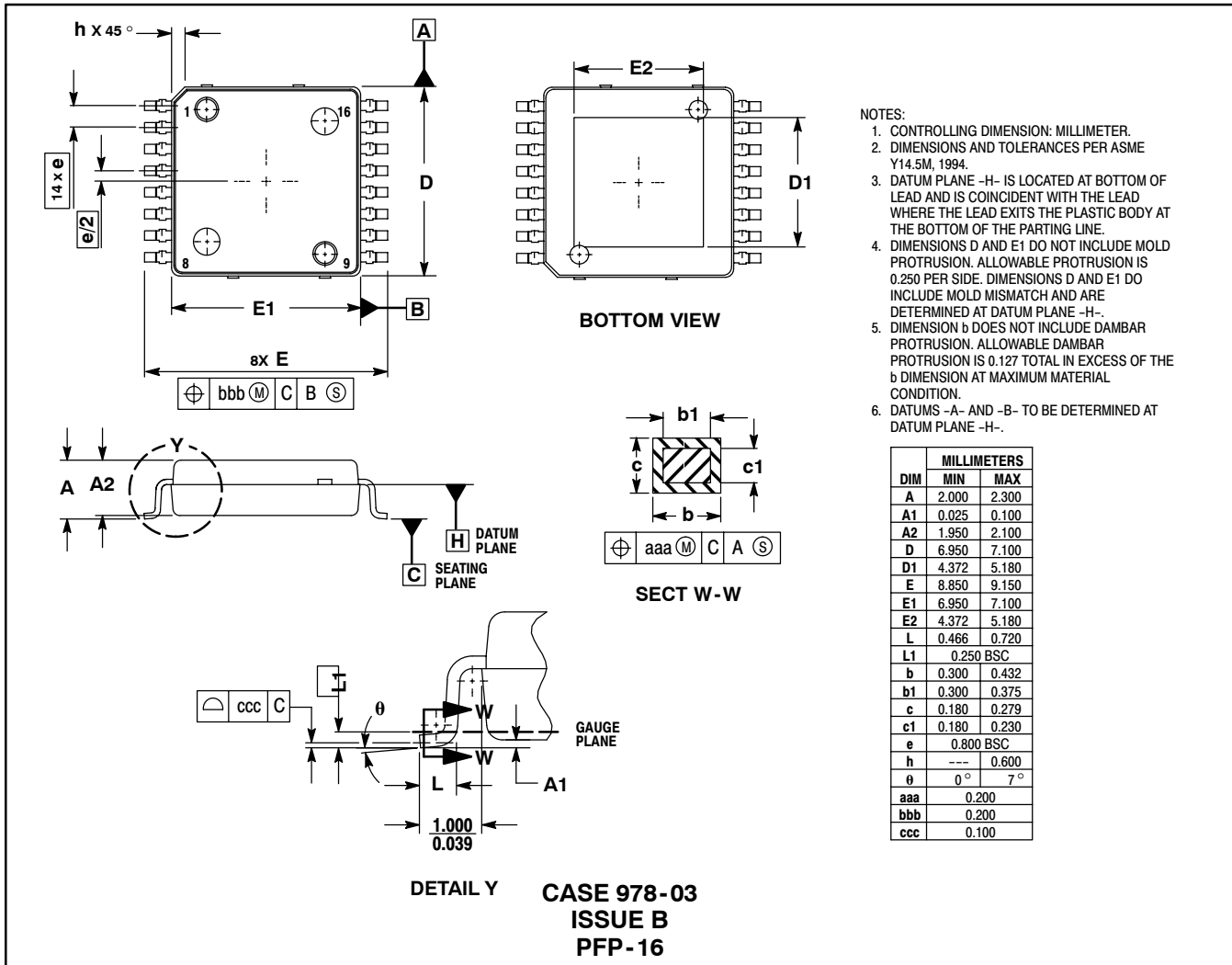


Figure 14. Series Equivalent Input and Load Impedance

NOTES

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PACKAGE DIMENSIONS



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