MULTI-INNO TECHNOLOGY CO., LTD.

LCD MODULE SPECIFICATION

Model : MI0240JT

Revision	
Engineering	
Date	
Our Reference	

DOCUMENT REVISION HISTORY

DOCUMENT REVISION FROM TO	DATE	DESCRIPTION	CHANGED BY	CHECKED BY
A	2007.08.07	First Release.		

CONTENTS

Specification
of
LCD Module Type
Model No.: MI0240JT

1. General Description

- QVGA, 2.4",240 x RGB x 320 dots, 262k colors, TFT, transmissive, dot matrix LCD module.
- Amorphous Silicon TFT active matrix.
- Viewing angle: 12 o'clock.
- Driving scheme: 1/320 duty.
- Driving IC: 'ILITEK' ILI9320 (COG) TFT controller / driver or equivalent.
- 16/18-bit Parallel bus interface with 8080-series MPU or RGB interface.
- Logic voltage: 2.8V(typ.).
- White LED backlight.
- FPC connection.
- "RoHS" compliance.

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

Parameter		Specifications	Unit
Outline dimensions		42.72(W) x 59.46(H) x 3.00(D) (Exclude bending area, component area, cable of backlight and FPC)	mm
TFT 240xRGBx320	Active area	36.72(W) x 48.96(H)	mm
	Display format	240 x RGB x 320	dots
	Color configuration	RGB stripe	-
	Dot pitch	0.153(RGB)(W) x 0.153(H) (or 0.051(W) x 0.153(H))	mm
Weight		TBD	gram

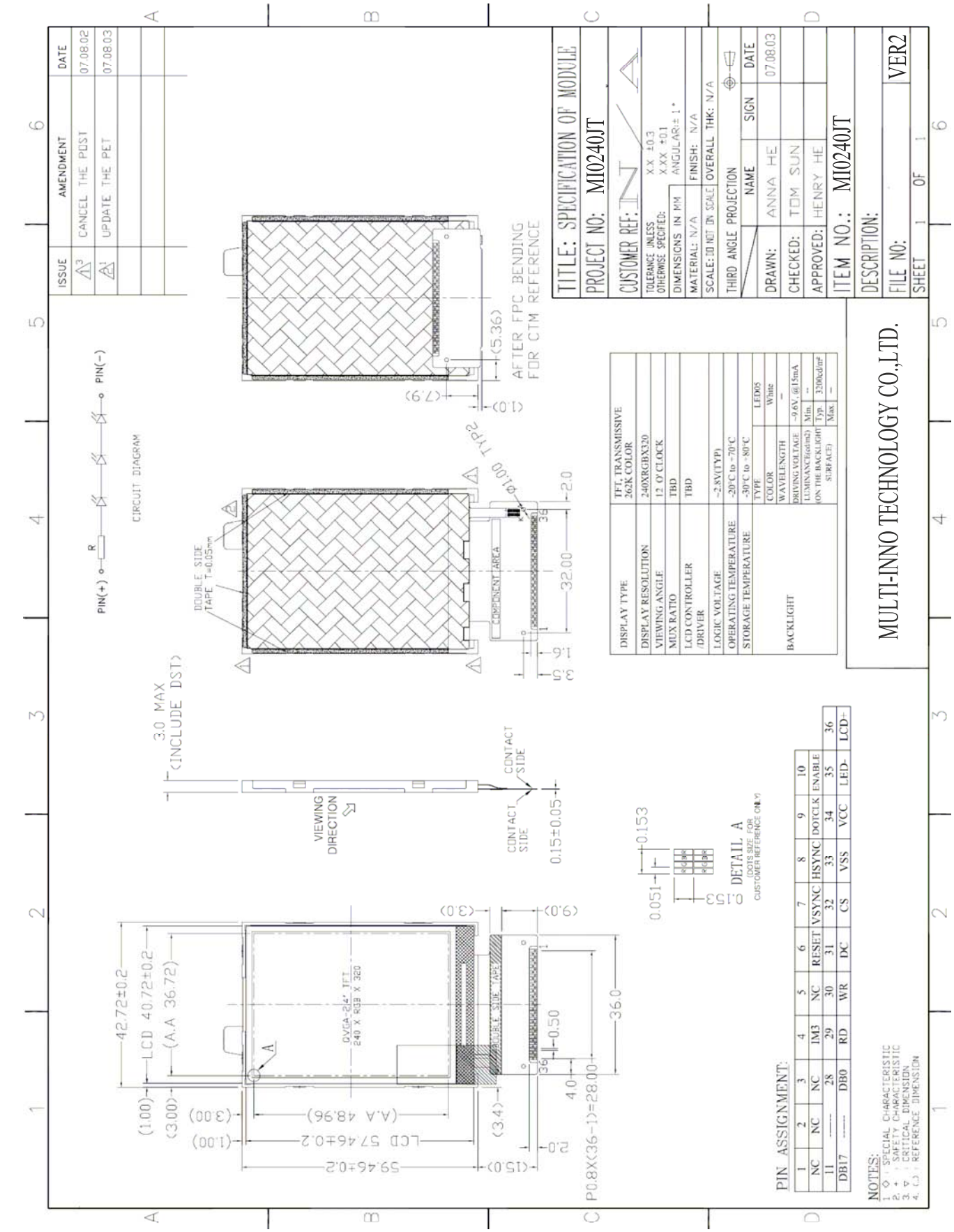


Figure 1: Module Specification

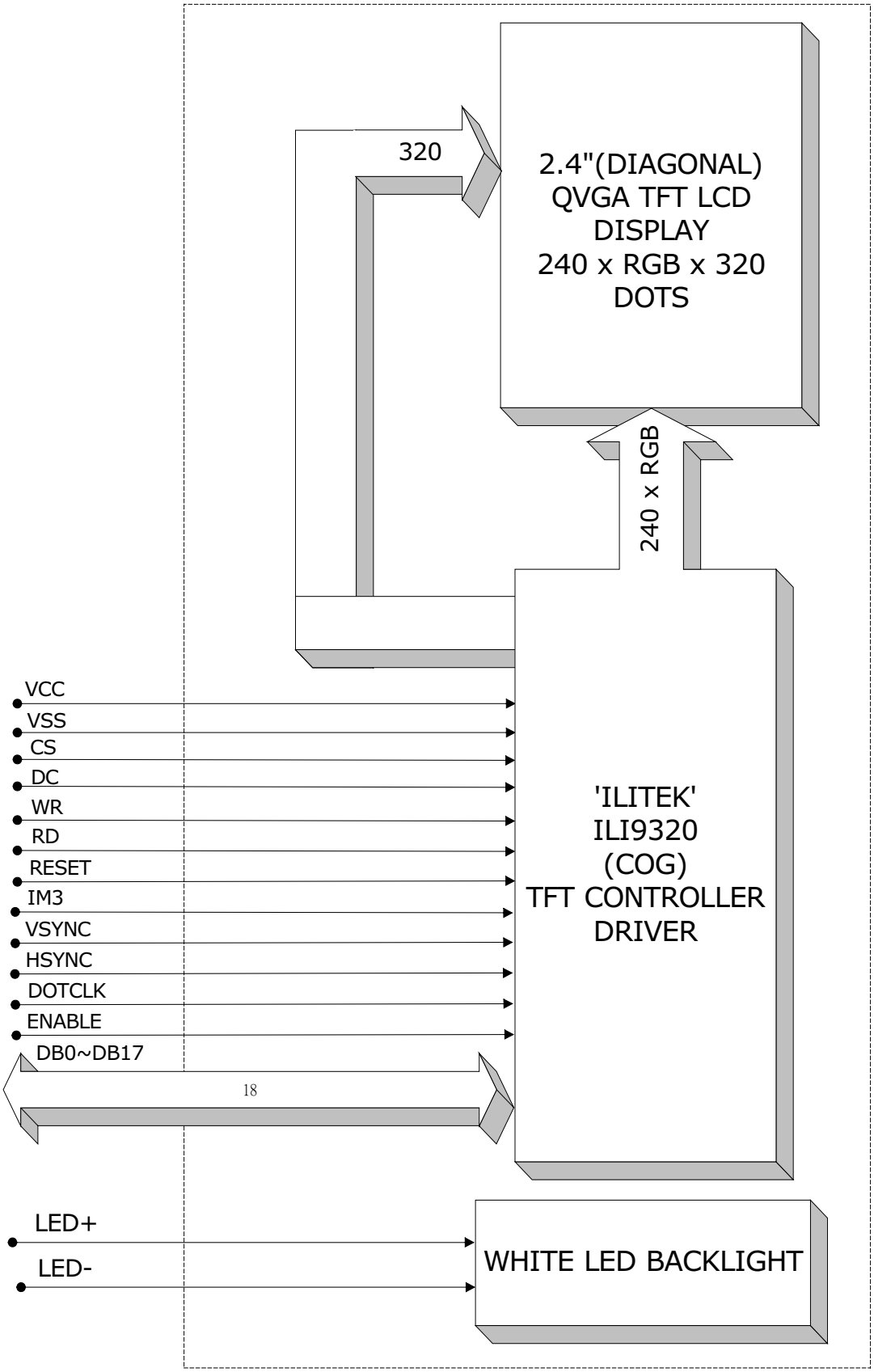


Figure 2: Block Diagram

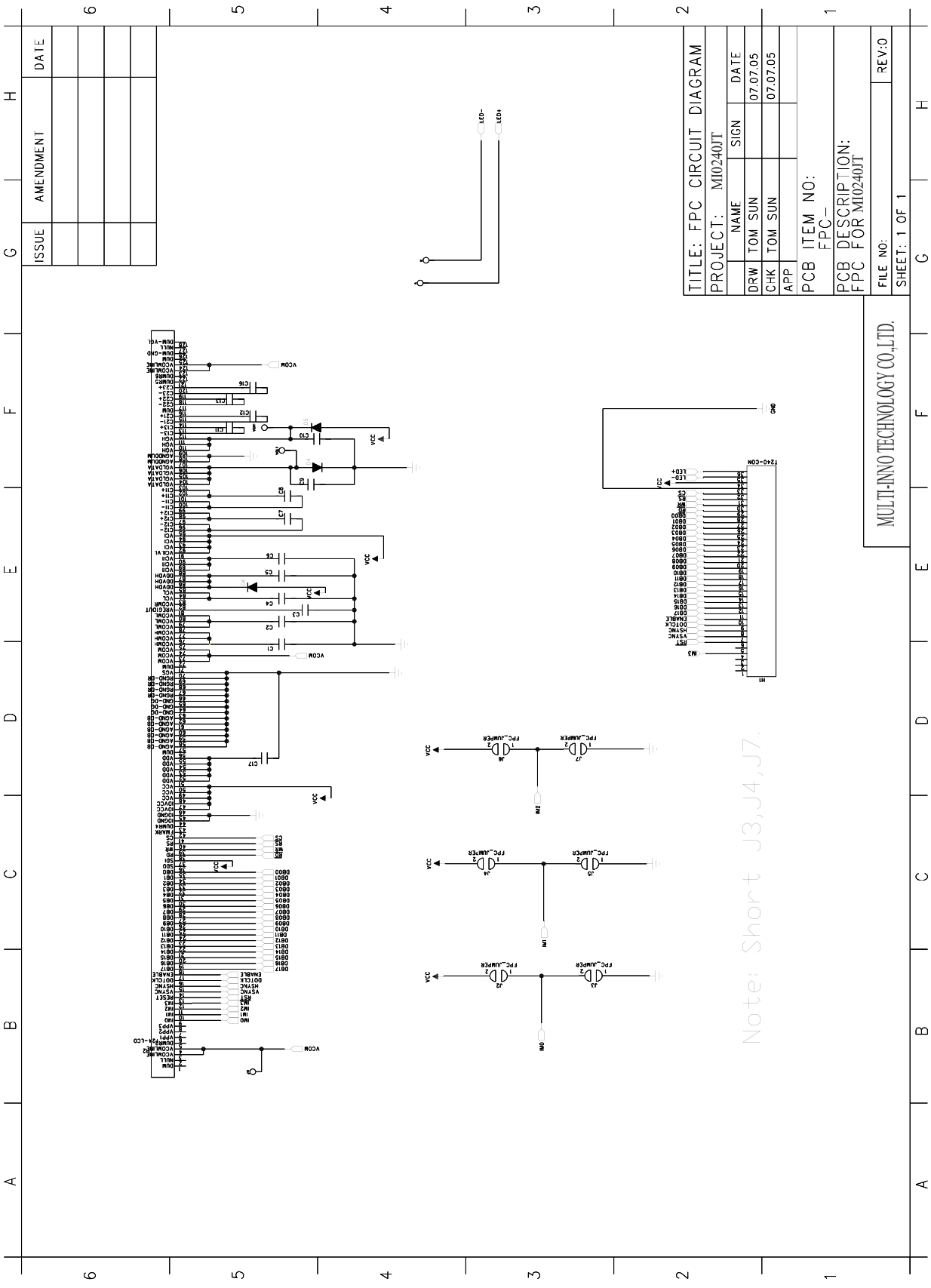


Figure 3: Reference circuit diagram

3. Interface signals

Table 2: Pin assignment

Pin No.	Symbol	Description
1~3	NC	No connection.
4	IM3	When IM3 select “0”, connect to i80-system 16-bit interface. When IM3 select “1”, connect to i80-system 18-bit interface.
5	NC	No connection.
6	RESET	A reset pin. Initializes the ILI9320 with a low input. Be sure to execute a power-on reset after supplying power.
7	VSYNC	Frame synchronizing signal for RGB interface operation. VSPL = “0”: Active low. VSPL = “1”: Active high.
8	HSYNC	Line synchronizing signal for RGB interface operation. HSPL = “0”: Active low. HSPL = “1”: Active high.
9	DOTCLK	Dot clock signal for RGB interface operation. DPL = “0”: Input data on the rising edge of DOTCLK DPL = “1”: Input data on the falling edge of DOTCLK
10	ENABLE	Data ENEABLE signal for RGB interface operation. Low: Select (access enabled) High: Not select (access inhibited) The EPL bit inverts the polarity of the ENABLE signal.
11~28	DB17~DB0	Data bus.
29	RD	A read strobe signal and enables an operation to read out data when the signal is low.
30	WR (NWR)	A write strobe signal and enables an operation to write data when the signal is low.
31	DC (RS)	A register select signal. Low: select an index or status register; High: select a control register
32	CS (NCS)	A chip select signal. Low: the ILI9320 is selected and accessible High: the ILI9320 is not selected and not accessible
33	VSS	Ground
34	VCC	Power supply.
35	LED-	Cathode of LED backlight.
36	LED+	Anode of LED backlight.

4. Absolute Maximum Ratings

4.1 Electrical Maximum Ratings – for IC Only

Table 3

Parameter	Symbol	Min.	Max.	Unit	Note
Power supply voltage (1)	VCC, IOVCC	-0.3	+4.6	V	1,2
Power supply voltage (1)	VCI - AGND	-0.3	+4.6	V	1,4
Power supply voltage (1)	DDVDH - AGND	-0.3	+6.0	V	1,4
Power supply voltage (1)	AGND - VCL	-0.3	+4.6	V	1
Power supply voltage (1)	DDVDH - VCL	-0.3	+9.0	V	1,5
Power supply voltage (1)	VGH - AGND	-0.3	+18.5	V	1,5
Power supply voltage (1)	AGND - VGL	-0.3	+18.5	V	1,6
Input voltage	Vt	-0.3	VCC+0.3	V	7

Notes:

1. VCC, DGND must be maintained
2. (High) (VCC = VCC) ≥ DGND (Low), (High) IOVCC ≥ DGND (Low).
3. Make sure (High) VCI ≥ DGND (Low).
4. Make sure (High) DDVDH ≥ ASSD (Low).
5. Make sure (High) DDVDH ≥ VCL (Low).
6. Make sure (High) VGH ≥ ASSD (Low).
7. Make sure (High) ASSD ≥ VGL (Low).
8. The modules may be destroyed if they are used beyond the absolute maximum ratings.

4.2 Environmental Condition

Table 4

Item	Operating temperature (Topr)		Storage temperature (Tstg) (Note 1)		Remark
	Min.	Max.	Min.	Max.	
Ambient temperature	-20°C	+70°C	-30°C	+80°C	Dry
Humidity (note 1)	90% max. RH for Ta ≤ 40°C < 50% RH for 40°C < Ta ≤ Maximum operating temperature				No condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Frequency: 10 ~ 55 Hz Amplitude: 0.75 mm Duration: 20 cycles in each direction.				3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Pulse duration: 11 ms Peak acceleration: 981 m/s^2 = 100g Number of shocks: 3 shocks in 3 mutually perpendicular axes.				3 directions

Note 1: Product cannot sustain at extreme storage conditions for long time.

5. Electrical Specifications

5.1 Typical Electrical Characteristics

At Ta = 25 °C, VCC=2.8V, VSS=0V.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (logic)	VCC-GND		2.5	2.8	3.0	V
Supply voltage	VCI		2.5	2.8	3.0	V
TFT gate ON voltage	VGH (Note 1)		12	-	18	V
TFT gate OFF voltage	VGL (Note 2)		-12	-	-7	V
TFT common electrode voltage	Vcom (Note 3)		-2	-	5	V
TFT kick-back voltage Max.	ΔVp max.		0.2	-	1.5	V
TFT kick-back voltage Min.	ΔVp min.		0.2	-	1.5	
Input signal voltage	V_{IH}	"H" level	0.8IOVCC	-	VCC	V
	V_{IL}	" L" level	-0.3	-	0.2IOVCC	V
Supply current (Logic & LCD)	ICC	VCC=2.8V	-	-	15.0	mA
Supply voltage of white LED backlight	VLED	Forward current =15 x 3 =45mA	9.1	9.6	10.1	V
Luminance (on the backlight surface)		Number of LED dies = 3	3200	-	-	cd/m^2

Note (1): VGH is TFT Gate operating voltage.

Note (2): VGL is TFT Gate operating voltage.

The low voltage level of VGL signal must be fluctuates with same phase as Vcom.

Note (3): Vcom must be adjusted to optimize display quality, as Crosstalk and Contrast ratio etc.

5.2 Timing Specification

5.2.1 i80-system Interface Timing Characteristics

Normal Write Mode

Table 6

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Bus cycle time	Write	t_{CYCW}	ns	100	-	-	-
	Read	t_{CYCR}	ns	300	-	-	-
Write low-level pulse width		PW_{LW}	ns	50	-	500	-
Write high-level pulse width		PW_{HW}	ns	50	-	-	-
Read low-level pulse width		PW_{LR}	ns	150	-	-	-
Read high-level pulse width		PW_{HR}	ns	150	-	-	
Write / Read rise / fall time		t_{WRr}/t_{WRf}	ns	-	-	25	
Setup time	Write (RS to nCS, E/nWR)	t_{AS}	ns	10	-	-	
	Read (RS to nCS, RW/nRD)			5	-	-	
Address hold time		t_{AH}	ns	5	-	-	
Write data set up time		t_{DSW}	ns	10	-	-	
Write data hold time		t_H	ns	15	-	-	
Read data delay time		t_{DDR}	ns	-	-	100	
Read data hold time		t_{DHR}	ns	5	-	-	

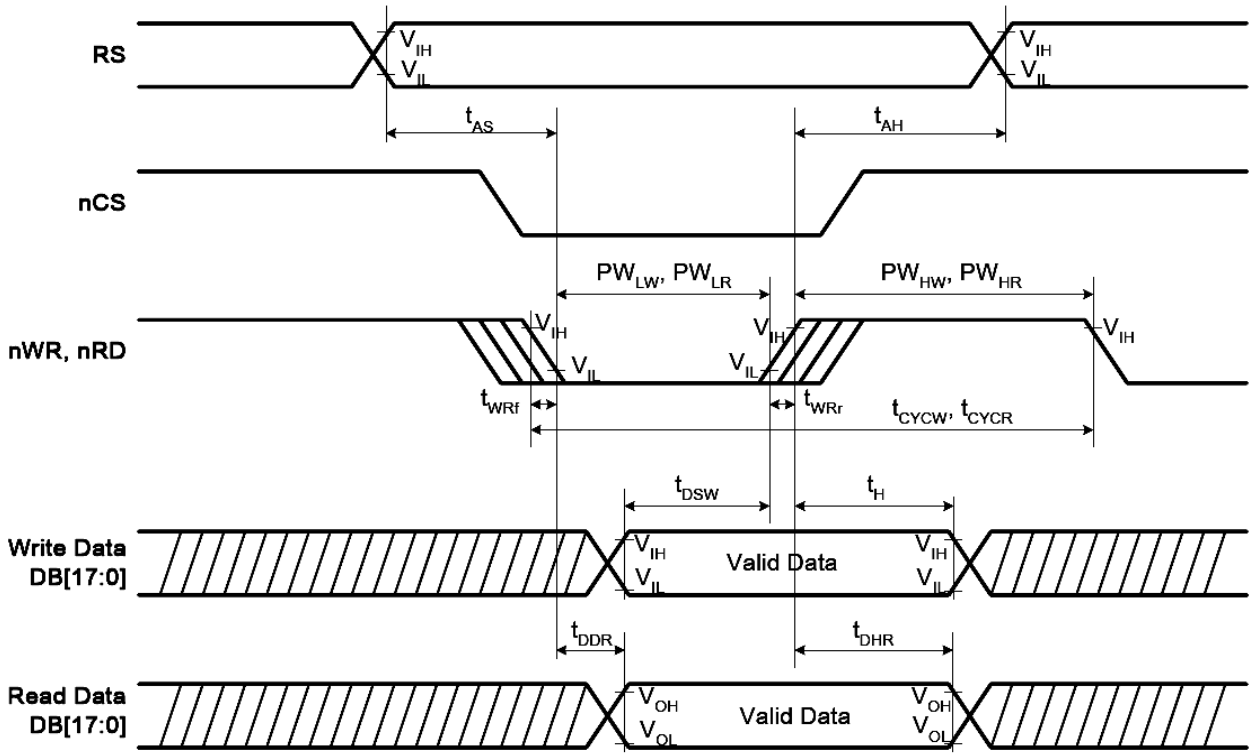


Figure 4: i80-system Interface Timing

5.2.2 Reset Timing Characteristics

Table 7

Item	Symbol	Unit	Min.	Typ.	Max.
Reset low-level width	t_{RES}	ms	1	-	-
Reset rise time	t_{rRES}	µs	-	-	10

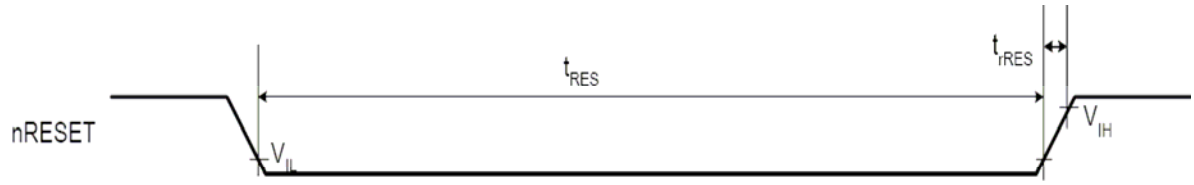


Figure 5: Reset Timing

5.2.3 RGB Interface Timing Characteristics

18/16-bit Bus RGB Interface Mode

Table 8

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
VSYNC/HSYNC setup time	t_{SYNCS}	ns	0	-	-	-
ENABLE setup time	t_{ENS}	ns	10	-	-	-
ENABLE hold time	t_{ENH}	ns	10	-	-	-
PD Data setup time	t_{PDS}	ns	10	-	-	-
PD Data hold time	t_{PDH}	ns	40	-	-	-
DOTCLK high-level pulse width	PWDH	ns	40	-	-	-
DOTCLK low-level pulse width	PWDL	ns	40	-	-	-
DOTCLK cycle time	t_{CYCD}	ns	100	-	-	-
DOTCLK, VSYNC, HSYNC, rise/fall time	t_{rghr}, t_{rghf}	ns	-	-	25	-

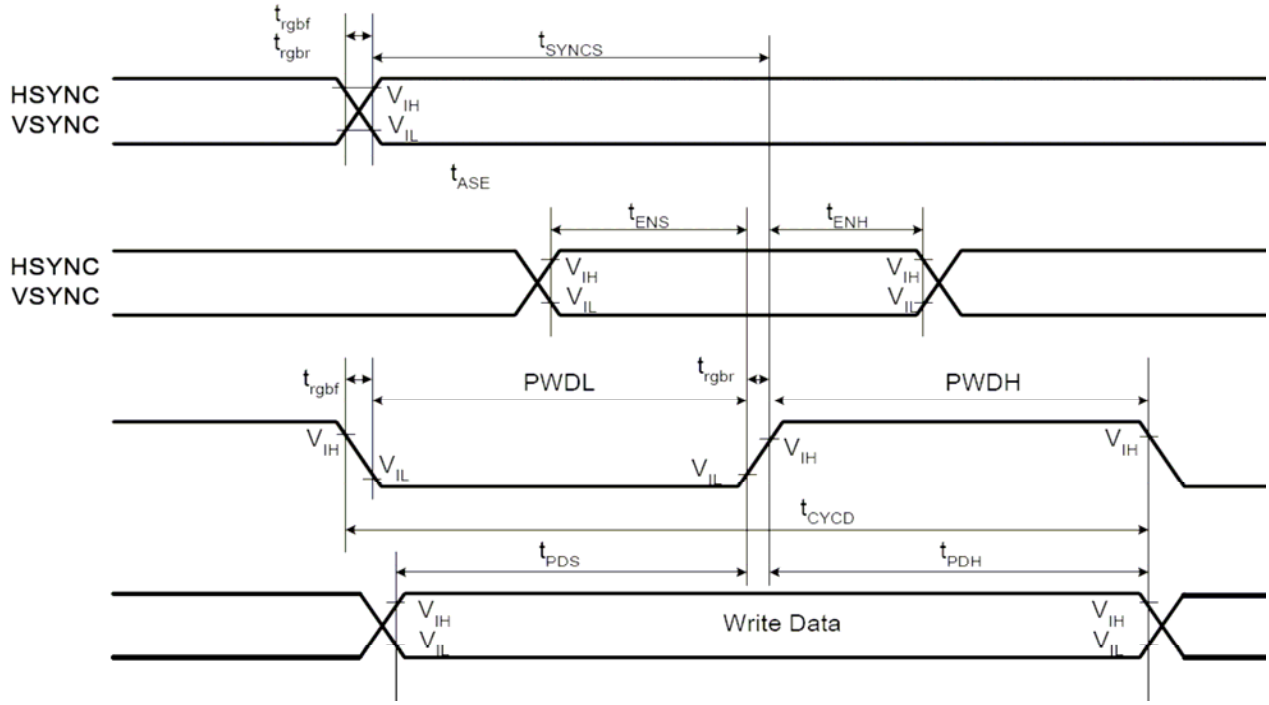


Figure 6: RGB Interface Timing

5.3 Display ON/OFF Sequence

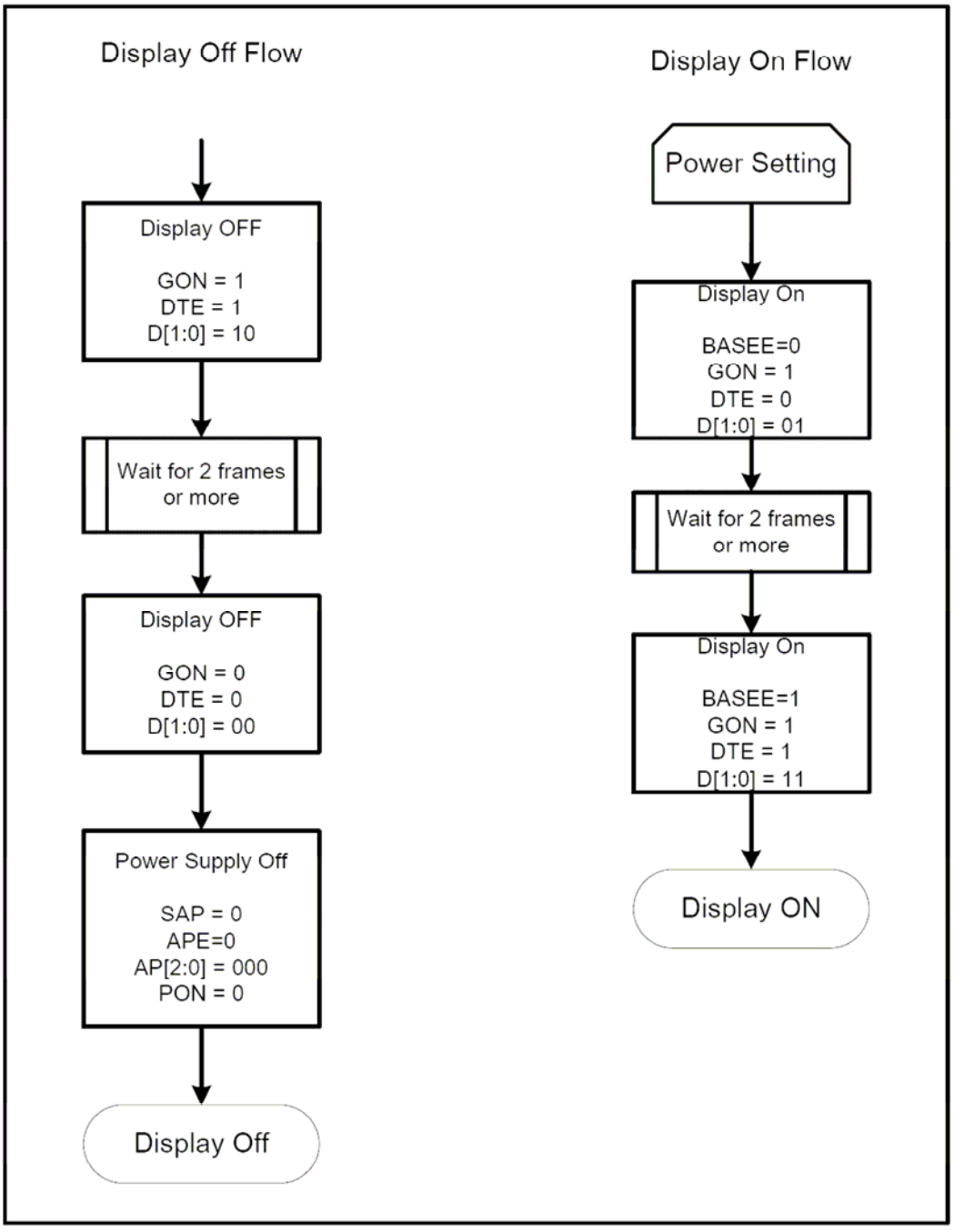


Figure 7: Display On/Off Register Setting Sequence

5.4 Deep Standby and Sleep Mode

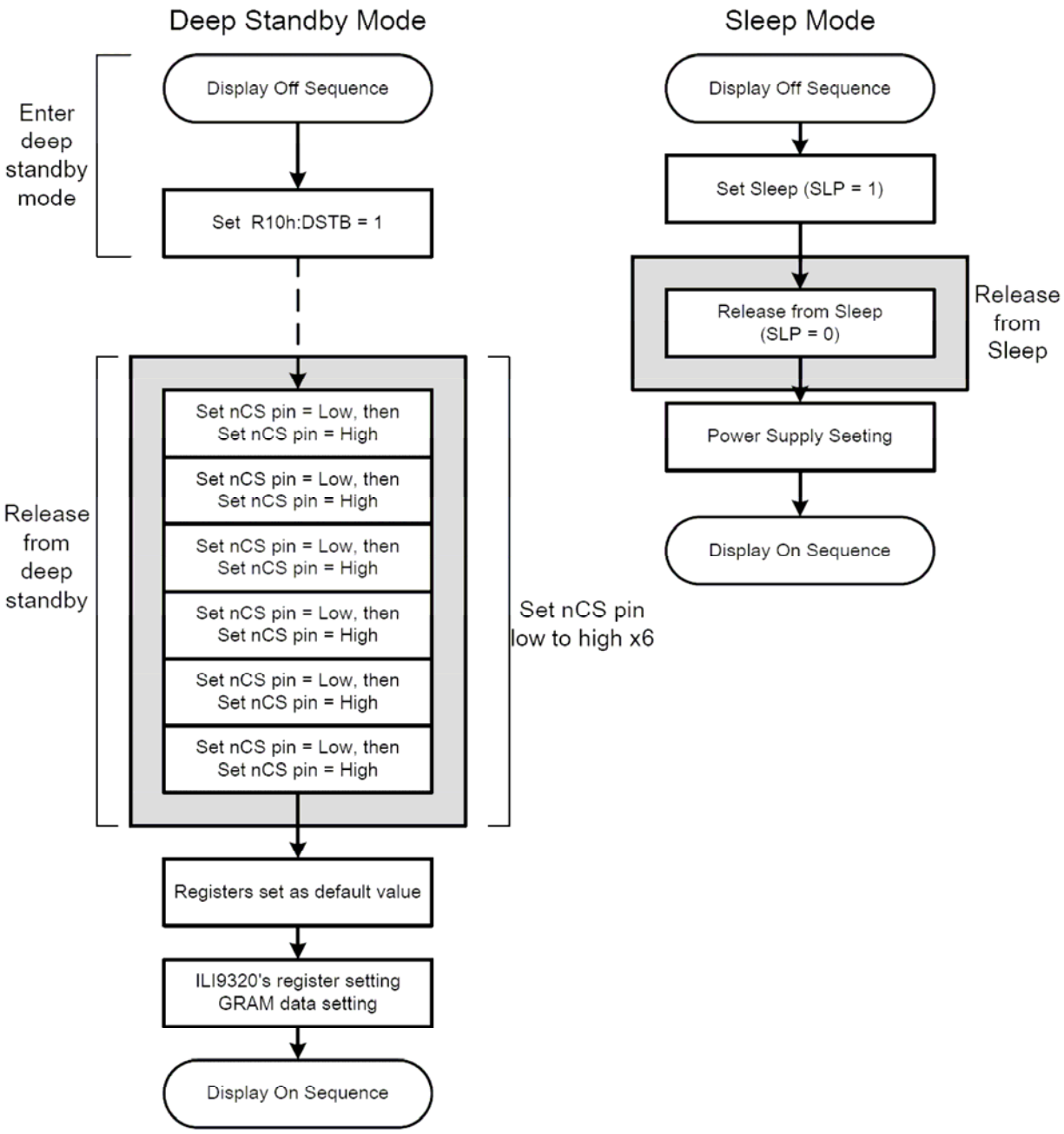


Figure 8: Deep Standby/Sleep Mode Register Setting Sequence

5.5 Power Supply Configuration

When supplying and cutting off power, follow the sequence below. The setting time for oscillators, step-up circuits and operational amplifiers depends on external resistance and capacitance.

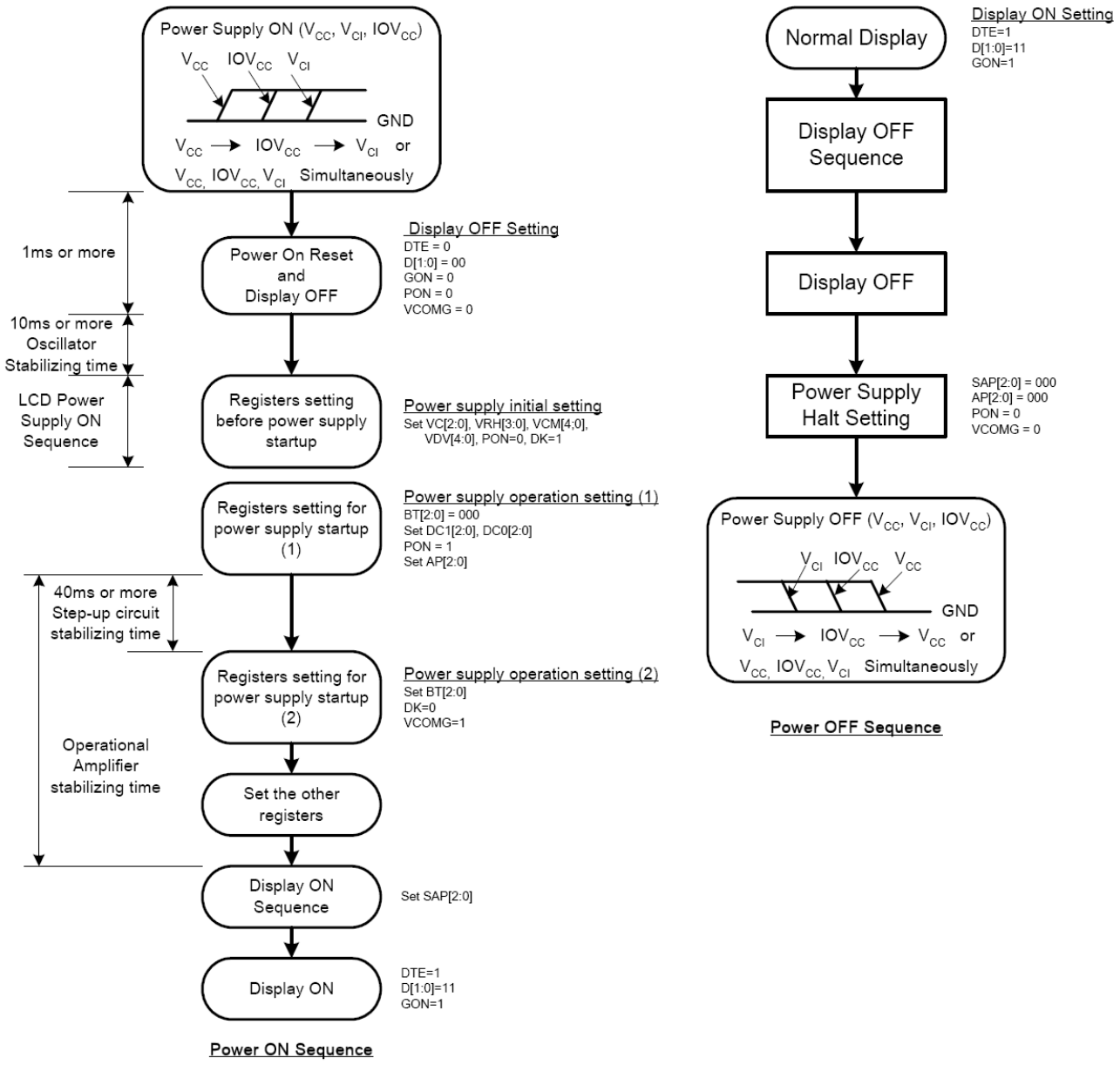


Figure 9: Power Supply ON/OFF Sequence

6. Optical Characteristics

Table 9

Items		Symbol	Condition	specifications			Unit	Remark
				Min.	Typ.	Max.		
Threshold voltage		Vsat		2.2	2.3	2.4	V	Fig. 10
		Vth		1.3	1.4	1.5	V	
Viewing angle range	Horizontal	ϕ1 (3 o'clock)	CR＞10	40	45	-	Deg.	Note 1
		ϕ2 (9 o'clock)		40	45	-	Deg.	
	Vertical	θ2 (12 o'clock)		45	50	-	Deg.	
		θ1 (6 o'clock)		15	20	-	Det.	
Contrast ratio		CR	θ = 0°	-	300	-	-	Note 2
Transmittance		T (%)	θ = 0°	-	5.8	-	-	Note 3
White chromaticity		Xw	θ = 0°	0.280	0.300	0.320	-	Note 4 Color filter glass
		Yw		0.314	0.334	0.354	-	
Reproduction of color	Red	X_R	θ = 0°	0.610	0.630	0.650	-	
		Y_R		0.311	0.331	0.351	-	
	Green	X_G		0.265	0.285	0.305	-	
		Y_G		0.541	0.561	0.581	-	
	Blue	X_B		0.115	0.135	0.155	-	
		Y_B		0.106	0.126	0.146	-	
Response time		Tr + Tf	θ = 0°	-	25	-	msec	Note 5

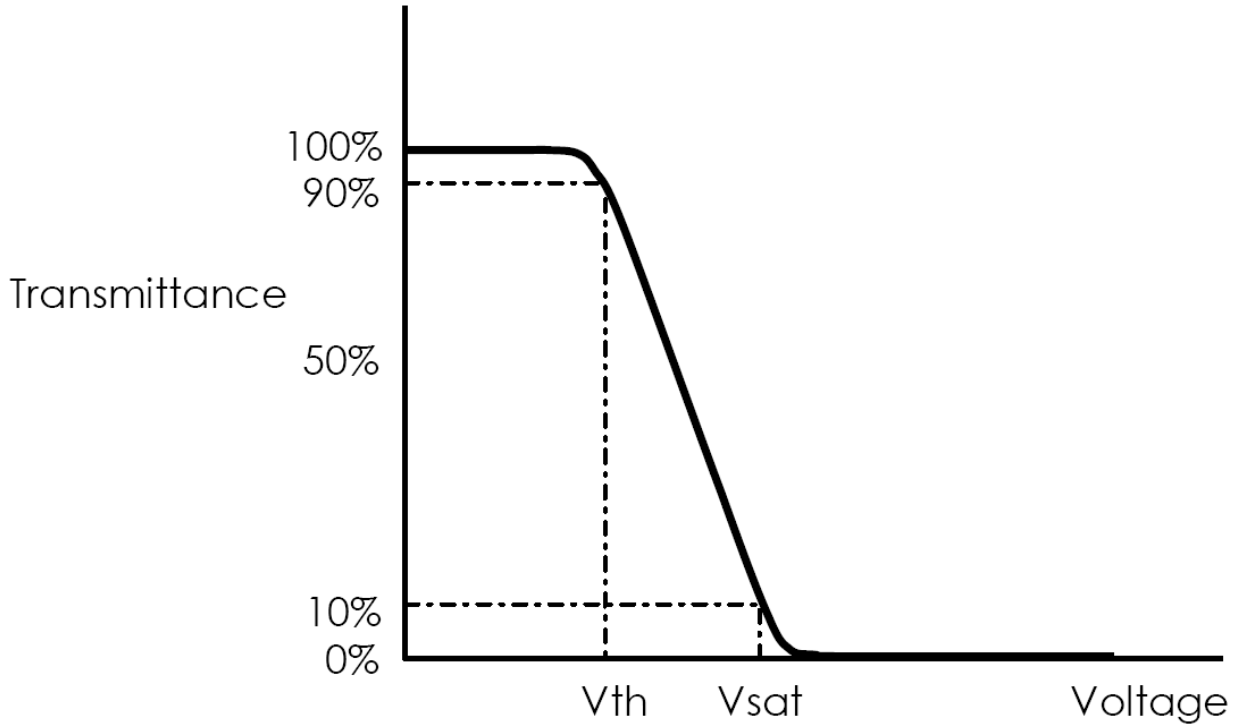


Figure 10: The definition of Vth & Vsat

Note 1: Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (See Figure 11).

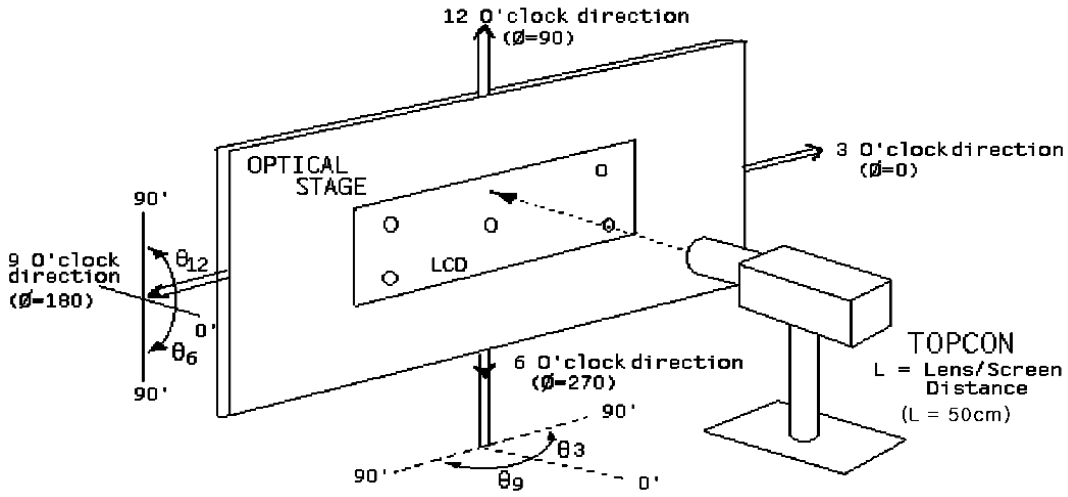


Figure 11: Measurement Set Up

Note 2: Contrast measurements shall be made at viewing angle of $\Theta = 0°$ and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (See Figure 11) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

Note3: Transmittance is the value with Polarizer The color chromaticity coordinates specified in Table 9 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the C/F. Measurement condition is C - light source & Halogen Lamp.

Note 4: The electro-optical response time measurements shall be made as Figure 12 shown in below by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is Tr, and 90% to 10% is Td.

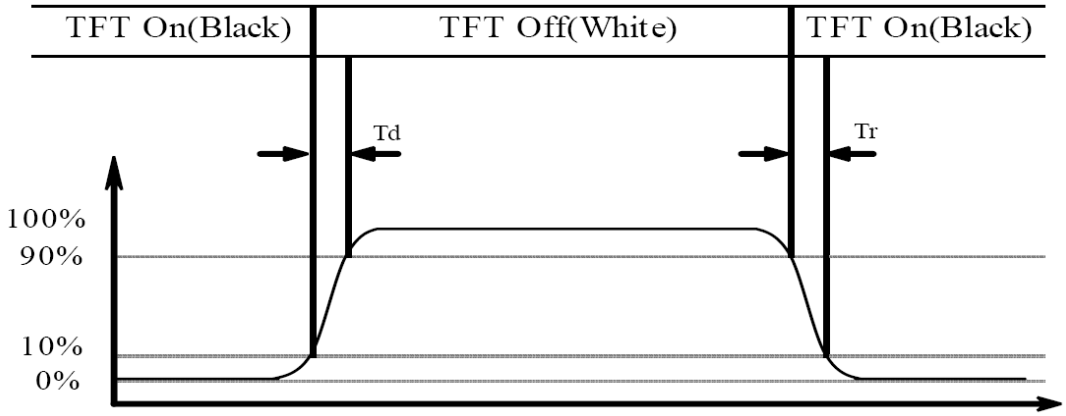
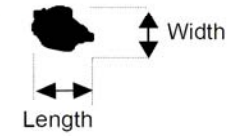
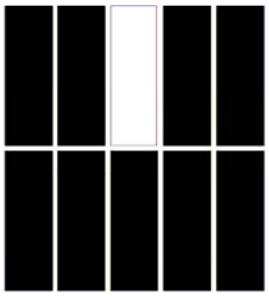
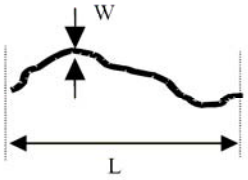
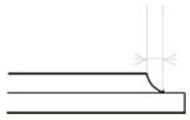
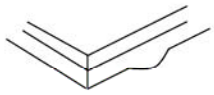
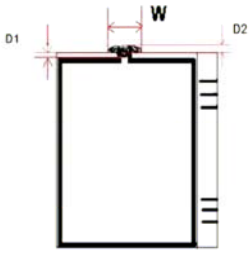
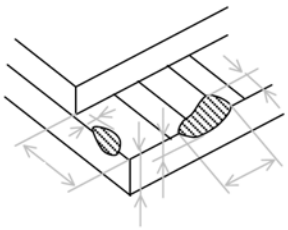
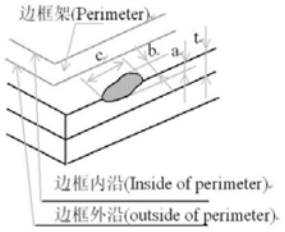
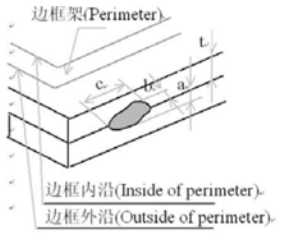
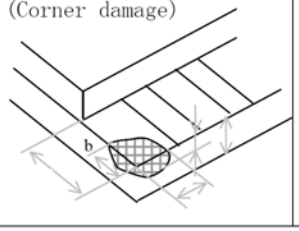


Figure 12: Response Time Testing

7. TFT inspection specification

壞品名稱 Failure mode	圖例說明 Illustration	分类 Category(Unit: mm)		可接受数量 Acceptable count	
				可视区 Viewing area	非可视区 non-Viewing area
黑點 Black spot 白點 White spot	 Φ= (Length+width)/2	A	Φ≦0.10	不计 Not count	不计 Not count
		B	0.10<Φ≦0.15	2, 两点间距离不小于 5mm The gap between the two spots should be 5 mm and above.	
		C	0.15<Φ≦0.20	1	
		D	0.20<Φ	0	
亮點(因爲濾光片損壞造成的紅點，綠點，藍點等) Bright spot (Red spot, green spot and blue spot caused by damaged colour filter)		A	缺陷面積小於或等於一個單基色面積 Area≦1 sub-pixel	1	N/A
黑线 Black line 白线 White line		A	W≦0.03	不计 Not count	不计 Not count
		B	0.03<W≦0.05, L≦3.0	2	
		C	0.05<W	按黑白点判定 Judged by spot spec	
以下为外观标准(Below are cosmetic inspection specifications)					
玻璃毛刺 Excess glass		b≦1.0 且不影响外形尺寸及装配(注意 COG 工序对 b 的要求，不同尺寸 LCD 的 b 都不同) b≦1.0, this defect shall not affect the outline dimension or assembly process.(Remarks: For COG process, the defect size is decided by the dimension of LCD panel.)			
		不影响外形尺寸及装配. This defect shall not affect the outline dimension or assembly process.			
进胶尺寸 The depth of UV glue entered in LCD cell		進膠深度大於等於 0.2mm 且不可進入視域范圍，膠水凸出玻璃邊高度小于等于 0.8mm,长度=（注入口宽度）+（2~6 mm） a. D1≥0.2，not enter into viewing area b. D2≦0.8, c. W=End mouth width + (2~6 mm)			

<table>
<tr><td rowspan="5">玻璃缺陷划伤、缺损

Glass defect
(scratch, damage)</td><td>① 台阶破损 (LCD ledge damage)
  </td><td colspan="2">分类 Category</td></tr>
<tr><td>A</td><td>非电极区，台阶破损不得影响装配及外形尺寸
The defect shall not affect the outline dimension or assembly process at non ITO zone.</td></tr>
<tr><td>B</td><td>电极区的破损，b 不得超过邦定电极长度（该长度应不小于 1.2mm）的 1/4, a、c 方向不限制
b≦1/4w, a & c not count (at ITO zone)</td></tr>
<tr><td>C</td><td>台阶两侧的缺损不得损伤对位标识或走线
Alignment mark on LCD ledge shall not be damaged.</td></tr>
<tr><td>②非封接面破损 (Outside of perimeter damage)
  </td><td colspan="2">b 方向破损不得到达边框内沿
b can’t reach inside of perimeter.</td></tr>
<tr><td>③ 封接面破损
(Joint glass damage)
  </td><td colspan="2">b 方向破损不得到达边框外沿或走线
b can’t reach outside of perimeter or ITO layout.</td></tr>
<tr><td rowspan="2">④角上破损
(Corner damage)
  </td><td>A</td><td>a ≦ t， b ≦ 3.0， c ≦ 3.0</td></tr>
<tr><td colspan="2">B. 玻璃破损不允许损伤电极图形和/或对位标识
Alignment mark on LCD ledge shall not be damaged.</td></tr>
<tr><td colspan="3">注：a:表示崩角厚度；b:表示崩角深度；c:表示崩角长度；t;表示单片玻璃厚度；单位：mm
Remark: a stands for thickness of damage, b for width, c for length and t for glass thickness. (Unit: mm)</td></tr>
</table>

8. Remark

HANDLING LCD AND LCD MODULES

1. Liquid Crystal Display (LCD)

LCD is made up of glass, organic sealant, organic fluid and polymer based polarizers. The following precautions should be taken when handling:

(1) Keep the temperature within range for use and storage. Excessive temperature and humidity could cause polarization degredation, polarizer peel-off or bubble generation. When storage for a long period over 40° C is required, the relative humidity should be kept below 60%.
(2) Do not contact the exposed polarizers with anything harder than an HB pencil lead. To clean dust off the display surface, wipe gently with cotton, chamois or other soft material soaked in petroleum benzin. Never scrub hard.
(3) Varitronix does not responsible for any polarizer defect after the protective film has been removed from the display
(4) Wipe off saliva or water drops immediately. Contact with water over a long period of time may cause polarizer deformation or color fading, while an active LCD with water condensation on its surface will cause corrosion of ITO electrodes.
(5) PETROLEUM BENZIN is recommended to remove adhesives used to attach front/rear polarizers and reflectors, while chemicals like acetone, toluene, ethanol and isopropyl alcohol will cause damage to the polarizer. Avoid oil and fats. Avoid lacquer and epoxies which might contain solvents and hardeners to cause electrode errosion. Some solvents will also soften the epoxy covering the DIL pins and thereby weakening the adhesion of the epoxy on glass. This will cause the exposed electrodes to erode electrochemically when operating in high humidity and condensing environment.
(6) Glass can be easily chipped or cracked from rough handling, especially at corners and edges.
(7) Do not drive LCD with DC voltage.
(8) When soldering DIL pins, avoid excessive heat and keep soldering temperature between 260°C to 300°C for no more than 5 seconds. Never use wave or reflow soldering.

2. Liquid Crystal Display Modules (MDL)

2.1 Mechanical Considerations

MDL's are assembled and adjusted with a high degree of precision. Avoid excessive shocks and do not make any alterations or modifications. The following should be noted.
(1) Do not tamper in any way with the tabs on the metal frame.
(2) Do not modify the PCB by drilling extra holes, changing its outline, moving its components or modifying its pattern.
(3) Do not touch the elastomer connector (conductive rubber), especially when inserting an EL panel.
(4) When mounting a MDL make sure that the PCB is not under any stress such as bending or twisting. Elastomer contacts are very delicate and missing pixels could result from slight dislocation of any of the elements.
(5) Avoid pressing on the metal bezel, otherwise the elastomer connector could be deformed and lose contact, resulting in missing pixels.
(6) If FPCA need to be bent, please refer the suggested bending area on the specification. The stiffener and component area on FPC/FFC/COF must not be bent during or after assembly (Note: for those models with FPC/FFC/COF+stiffener).
(7) Sharp bending should be avoided on FPC to prevent track cracking.

2.2 Static Electricity

MDL contains CMOS LSI's and the same precaution for such devices should apply, namely:

(1) The operator should be grounded whenever he comes into contact with the module. Never touch any of the conductive parts such as the LSI pads, the copper leads on the PCB and the interface terminals with any part of the human body.
(2) The modules should be kept in antistatic bags or other containers resistant to static for storage.
(3) Only properly grounded soldering irons should be used.
(4) If an electric screwdriver is used it should be well grounded and shielded from commutator sparks.
(5) The normal static prevention measures should be observed for work clothes and working benches; for the latter conductive (rubber) mat is recommended.
(6) Since dry air is inducive to statics, a relative humidity of 50 - 60% is recommended.

2.3 Soldering

(1) Solder only to the I/O terminals.
(2) Use only soldering irons with proper grounding and no leakage.
(3) Soldering temperature is 280°C ± 10°C .
(4) Soldering time: 3 to 4 seconds.
(5) Use eutectic solder with resin flux fill.
(6) If flux is used. the LCD surface should be covered to avoid flux spatters. Flux residue should be removed afterwards.
(7) Use proper de-soldering methods (e.g. suction type desoldering irons) to remove lead wires from the I/O terminals when necessary. Do not repeat the soldering/ desoldering process more than three times as the pads and plated through holes may be damaged.

2.4 Label

Identification labels will be stuck on the module without obstructing the viewing area of display.

3. Operation

(1) The viewing angle can be adjusted by varying the LCD driving voltage Vo.
(2) Driving voltage should be kept within specified range, excess voltage shortens display life.
(3) Response time increases with decrease in temperature.
(4) Display may turn black or dark Blue at temperatures above its operational range; this is however not destructive and the display will return to normal once the temperature falls back to range.
(5) Mechanical disturbance during operation (such as pressing on the viewing area) may cause the segments to appear "fractured". They will recover once the display is turned off.
(6) Condensation at terminals will cause malfunction and possible electrochemical reaction. Relative humidity of the environment should therefore be kept below 60%.
(7) Display performance may vary out of viewing area. If there is any special requirement on performance out of viewing area, please consult Varitronix.

4. Storage and Reliability

(1) LCD's should be kept in sealed polyethylene bags while MDL's should use antistatic ones. If properly sealed, there is no need for desiccant.
(2) Store in dark places and do not expose to sunlight or fluorescent light. Keep the temperature between 0°C and 35°C and the relative humidity low. Please consult MULTI-INNO for other storage requirements.
(3) Water condensation will affect reliability performance of the display and is not allowed.
(4) Semi-conductor device on the display is sensitive to light and should be protected properly.
(5) Power up/down sequence.
   a) Power Up: in general, LCD supply voltage, Vo must be supplied after logic voltage, VDD becomes steady. Please refer to related IC data sheet for details.
   b) Power Down: in general, LCD supply voltage, Vo must be removed before logic voltage, VDD turns off. Please refer to related IC data sheet for details.

5. Safety

If any fluid leaks out of a damaged glass cell, wash off any human part that comes into contact with soap and water. Never swallow the fluid. The toxicity is extremely low but caution should be exercised at all times.

LIMITED WARRANTY

MULTI-INNO LCDs and modules are not consumer products, but may be incorporated by MULTI-INNO 's customers into consumer products or components thereof. MULTI-INNO does not warrant that its LCDs and components are fit for any such particular purpose.

1. The liability of MULTI-INNO is limited to repair or replacement on the terms set forth below. MULTI-INNO will not be responsible for any subsequent or consequential events or injury or damage to any personnel or user including third party personnel and/or user.

   Unless otherwise agreed in writing between MULTI-INNO and the customer, MULTI-INNO will only replace or repair any of its LCD which is found defective electrically or visually when inspected in accordance with MULTI-INNO LCD Acceptance Standards (copies available on request), for a period of one year from the date of shipment. Confirmation of such date shall be based on freight documents.

2. No warranty can be granted if any of the precautions stated in HANDLING LCD and LCD Modules above have been disregarded. Broken glass, scratches on polarizers, mechanical damages as well as defects that are caused by accelerated environmental tests are excluded from warranty.
3. In returning the LCD and Modules, they must be properly packaged and there should be detailed description of the failures or defects.

IMPORTANT NOTICE

The information presented in this document has been carefully checked and is believed to be accurate, however, no responsibility is assumed for inaccuracies. MULTI-INNO reserves the right to make changes to any specifications without further notice for performance, reliability, production technique and other considerations, MULTI-INNO does not assume any liability arising out of the application or use of products herein. Please see Limited Warranty in the previous section.

- END -