MULTI-INNO TECHNOLOGY CO., LTD.

LCD MODULE SPECIFICATION

Model : MI9664FK

Revision	
Engineering	
Date	
Our Reference	

DOCUMENT REVISION HISTORY

DOCUMENT REVISION FROM TO	DATE	DESCRIPTION	CHANGED BY	CHECKED BY
A	2007.11.16	First Release.	ZHANG YAN FANG	LUO CHENG

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Preliminary Specification
of
LCD Module Type
Model No.: MI9664FK

1. General Description

- 0.95", 96 x RGB x 64 dots 56K CSTN Negative transmissive dot matrix LCD module.
- Viewing angle: 6 o'clock.
- Driving scheme: 1/64 duty, 1/9 bias.
- Driving IC:'ULTRACHIP' UC1681SGBB (COG) LCD controller / driver or equivalent.
- Data interface: 8080 system, 8-bit parallel bus.
- Logic voltage: 2.8V.
- Analog voltage: 2.8V.
- White LED backlight.
- Low power.
- FPC connection.
- "RoHS" compliance.

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

Parameter		Specifications	Unit
Outline dimensions		26.76(W) x 27.08(H) x 3.05(D) (Exclude FPC and terminals of backlight)	mm
CSTN 96xRGBx64	Viewing area	22.15(W) x 15.43(H)	mm
	Active area	20.15(W) x 13.43(H)	mm
	Display format	96 x RGB x 64	dots
	Color configuration	R.G.B. stripe	-
	Dot size	0.20 (RGB)(W) x 0.20 (H)	mm
	Dot spacing	0.01 (W) x 0.01 (H)	mm
	Dot pitch	0.21(RGB)(W) x 0.21(H)	mm
Weight		TBD	gram

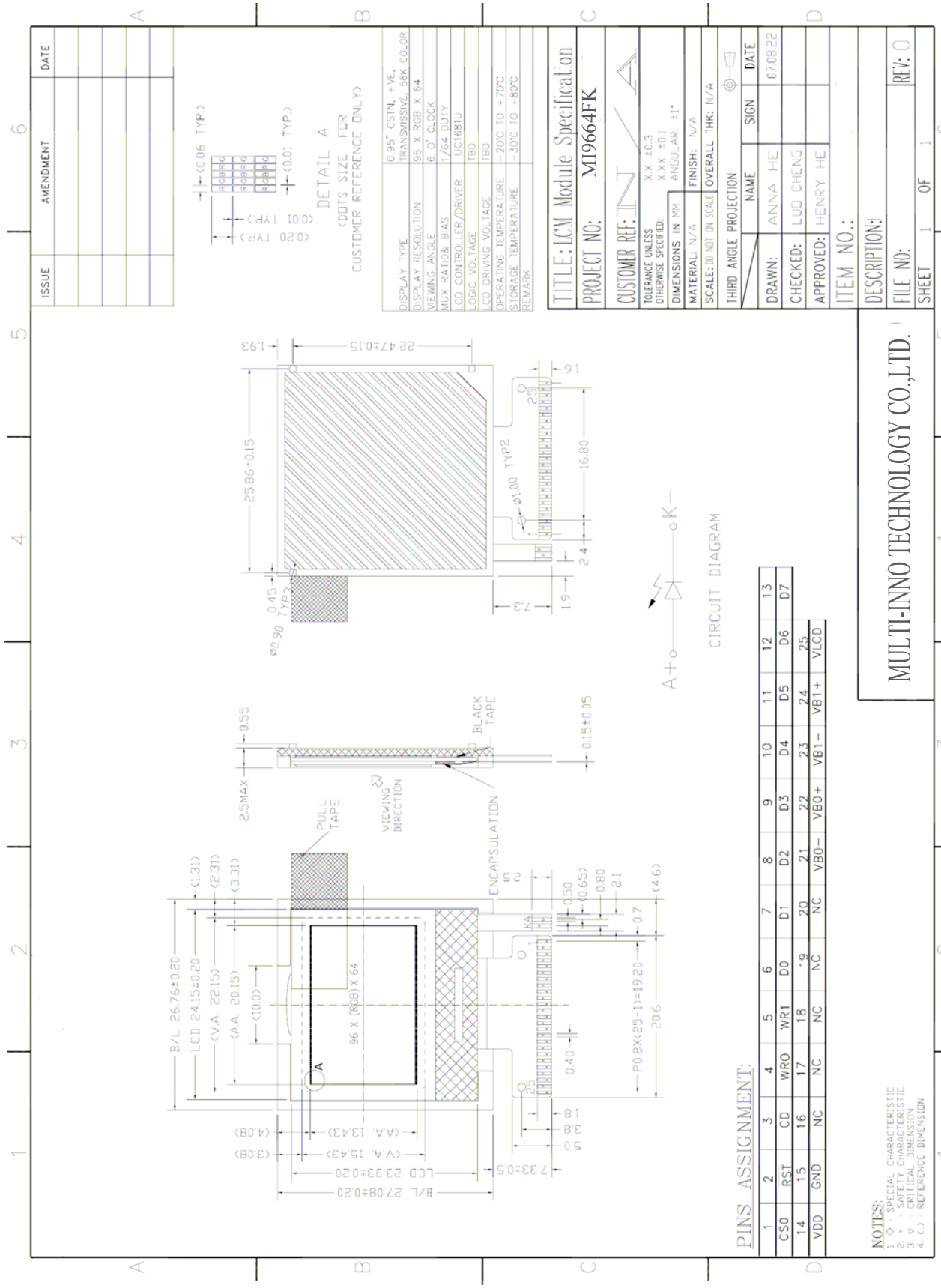

Figure 1: Module Specification

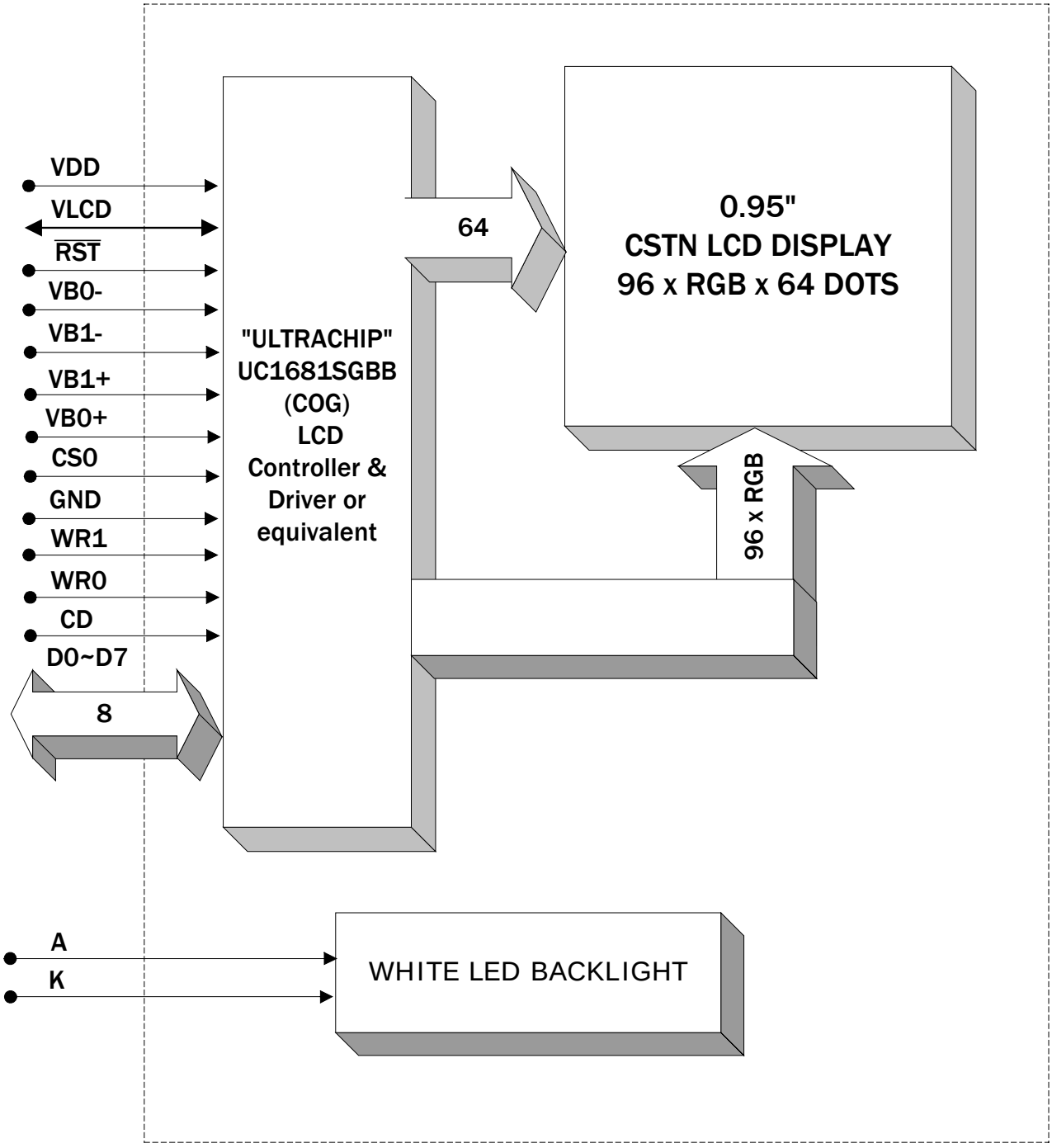

Figure 2: Block Diagram

3. Interface signals

Table 2

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Description</th></tr>
<tr><td>1</td><td>CS0</td><td>Chip Select. Chip is selected when CS0 = “L”.
When the chip is not selected, D[7:0] will be high impedance.</td></tr>
<tr><td>2</td><td>RST</td><td>When RST= “L”, all control registers are re-initialized by their default states.</td></tr>
<tr><td>3</td><td>CD</td><td>Select Control data or Display data for read/write operation.
In S9 mode, CD pin is not used. Connect CD to VSS when not used.
“L”: Control data “H”: Display data</td></tr>
<tr><td>4</td><td>WR0</td><td rowspan="2">WR[1:0] controls the read/write operation of the host interface.
In parallel mode, the meaning of WR[1:0] depends on whether the interface is in 6800 mode or 8080 mode.
In serial interface modes, these two pins are not used, connect them to VSS.</td></tr>
<tr><td>5</td><td>WR1</td></tr>
<tr><td>6</td><td>D0</td><td rowspan="8">Bi-directional bus for both serial and parallel host interfaces. In serial modes, connect D[0] to SCK, D[3] to SDA,
<table>
<tr><th></th><th>BM=1x
(Parallel)</th><th>BM=0x
(Parallel)</th><th>BM=01
(S9)</th><th>BM=00
(S8/S8uc)</th></tr>
<tr><td>D0</td><td>D0</td><td>D0/D4</td><td>SCK</td><td>SCK</td></tr>
<tr><td>D1</td><td>D1</td><td>D1/D5</td><td>–</td><td>–</td></tr>
<tr><td>D2</td><td>D2</td><td>D2/D6</td><td>–</td><td>–</td></tr>
<tr><td>D3</td><td>D3</td><td>D3/D7</td><td>SDA</td><td>SDA</td></tr>
<tr><td>D4</td><td>D4</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>D5</td><td>D5</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>D6</td><td>D6</td><td>–</td><td>0</td><td>S8/S8uc</td></tr>
<tr><td>D7</td><td>D7</td><td>0</td><td>1</td><td>1</td></tr>
</table>
Connect unused pins to VDD or VSS.</td></tr>
<tr><td>7</td><td>D1</td></tr>
<tr><td>8</td><td>D2</td></tr>
<tr><td>9</td><td>D3</td></tr>
<tr><td>10</td><td>D4</td></tr>
<tr><td>11</td><td>D5</td></tr>
<tr><td>12</td><td>D6</td></tr>
<tr><td>13</td><td>D7</td></tr>
<tr><td>14</td><td>VDD</td><td>Power supply.</td></tr>
<tr><td>15</td><td>GND</td><td>Ground (0V).</td></tr>
<tr><td>16~20</td><td>NC</td><td>No connection.</td></tr>
<tr><td>21</td><td>VB0-</td><td rowspan="4">LCD Bias Voltages.
These are the voltage sources to provide SEG driving currents.
These voltages are generated internally. Connect capacitors of CBX value between VBX+ and VBX–.
The resistance of these traces directly affects the driving strength of SEG electrodes and impacts the image of the LCD module. Minimize the trace resistance is critical in achieving high quality image.</td></tr>
<tr><td>22</td><td>VB-+</td></tr>
<tr><td>23</td><td>VB1-</td></tr>
<tr><td>24</td><td>VB1+</td></tr>
<tr><td>25</td><td>VLCD</td><td>LCD power supply.</td></tr>
<tr><td>-</td><td>A</td><td>Anode of LED backlight.</td></tr>
<tr><td>-</td><td>K</td><td>Cathode of LED backlight.</td></tr>
</table>

4. Absolute Maximum Ratings

4.1 Electrical Maximum Ratings – for IC Only

Table 3

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage (1)	VDD,VDD2	-0.3	+4.0	V
Supply Voltage (2)	VDD2-VDD	-	+1.6	V
LCD driving voltage	VLCD	-0.3	+11.8	V
Input voltage range	Vin	-0.4	VDD+0.5	V

Note:

The module may be destroyed if they are used beyond the absolute maximum ratings.

All voltage values are referenced to VSS= 0V.

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4.2 Environmental Condition

Table 4

Item	Operating temperature (Topr)		Storage temperature (Tstg) (note 1)		Remark
	Min.	Max.	Min.	Max.	
Ambient temperature (Ta)	-20°C	+70°C	-30°C	+80°C	Dry
Humidity (note 1)	90% max. RH for Ta ≤ 40°C < 50% RH for 40°C < Ta ≤ Maximum operating temperature				No condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Frequency: 10 ~ 55 Hz Amplitude: 0.75 mm Duration: 20 cycles in each direction.				3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Pulse duration: 11 ms Peak acceleration: 981 m/s^2 = 100g Number of shocks: 3 shocks in 3 mutually perpendicular axes.				3 directions

Note 1: Product cannot sustain at extreme storage conditions for long time.

5. Electrical Specifications

5.1 Typical Electrical Characteristics

At Ta = 25 °C, VDD =2.8V, GND=0V.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (logic)	VDD		2.4	2.8	3.3	V
Supply voltage (LCD) (Build-in)	VLCD	Ta=-20°C, Character mode, VDD=2.8V, Note 1.	-	TBD	-	V
		Ta=+25°C, VDD=2.8V, Note 1.	-	TBD	-	V
		Ta=+70°C, Character mode, VDD=2.8V, Note 1.	-	TBD	-	V
Low level input voltage	V_{IL}		VSS		0.2VDD	V
High level input voltage	V_{IH}		0.8VDD		VDD	V
Supply Current	IDD	All mode, VDD=2.8V	-	TBD	-	mA
Supply voltage of white LED backlight	VLED	Forward current =15mA Number of LED dies=1	3.0	3.2	3.4	V
Luminance of backlight (on the backlight surface)			2500	-	-	cd/m^2

Note (1): There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

5.2 Timing Specifications

5.2.1 Parallel Bus Timing Characteristics (for 8080 MCU)

At Ta =-20 °C To +70 °C, VDD= 2.8V, GND=0V.

Table 6

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		0 15	–	nS
t_{CY80}		System cycle time 8 bits bus (read) (write) 4 bits bus (read) (write)		 140 80 140 80	–	nS
t_{PWR80}	WR1	Pulse width 8 bits (read) 4 bits		70 70	–	nS
t_{PWW80}	WR0	Pulse width 8 bits (write) 4 bits		40 40	–	nS
t_{HPW80}	WR0, WR1	High pulse width 8 bits bus (read) (write) 4 bits bus (read) (write)		 70 40 70 40	–	nS
t_{DS80} t_{DH80}	D0~D7	Data setup time Data hold time		30 15	–	nS
t_{ACC80} t_{OD80}		Read access time Output disable time	C_L = 100pF	– 25	50 50	nS
t_{CSSA80} t_{CSH80}	CS1/CS0	Chip select setup time		5 5		nS

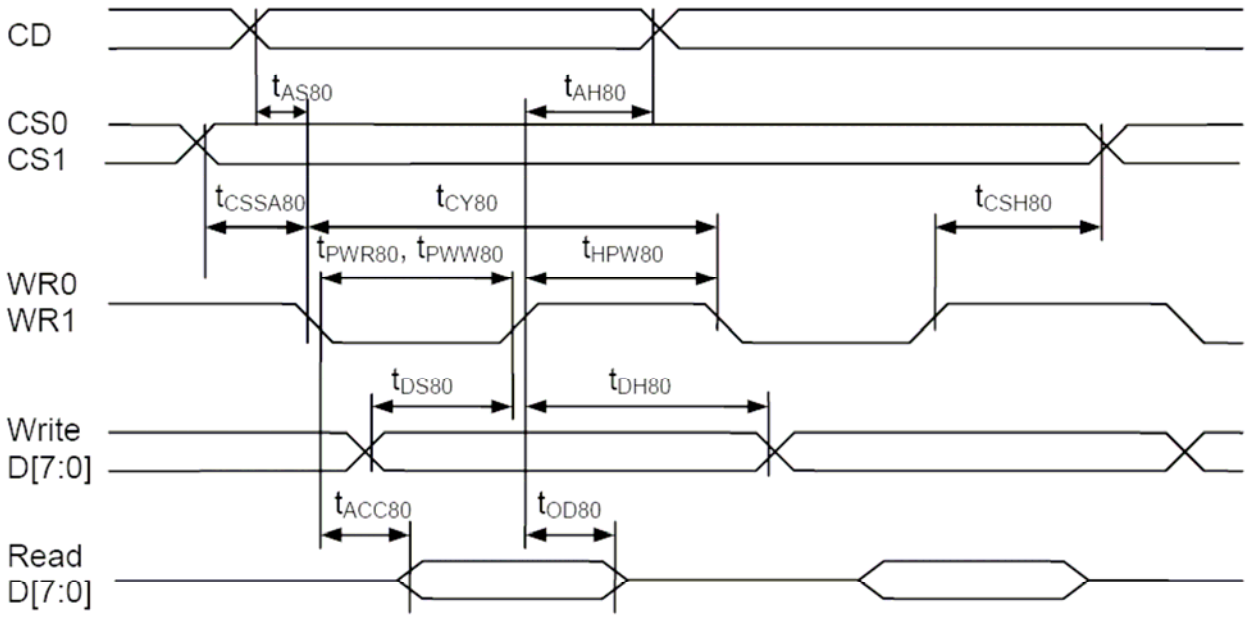


Figure 3: Parallel Bus Timing Characteristics (for 8080 MCU)

5.2.2 Parallel Bus Timing Characteristics (for 6800 MCU)

At Ta =-20 °C To +70 °C, VDD= 2.8V, GND=0V.

Table 7

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		0 20	–	nS
t_{CY68}		System cycle time 8 bits bus (read) (write) 4 bits bus (read) (write)		 140 80 140 80	–	nS
t_{PWR68}	WR1	Pulse width 8 bits (read) 4 bits		70 70	–	nS
t_{PWW68}		Pulse width 8 bits (write) 4 bits		40 40	–	nS
t_{LPW68}		Low pulse width 8 bits bus (read) (write) 4 bits bus (read) (write)		 70 40 70 40	–	nS
t_{DS68} t_{DH68}	D0~D7	Data setup time Data hold time		30 15	–	nS
t_{ACC68} t_{OD68}		Read access time Output disable time	C_L = 100pF	– 25	50 50	nS
t_{CSSA68} t_{CSH68}	CS1/CS0	Chip select setup time		5 5		nS

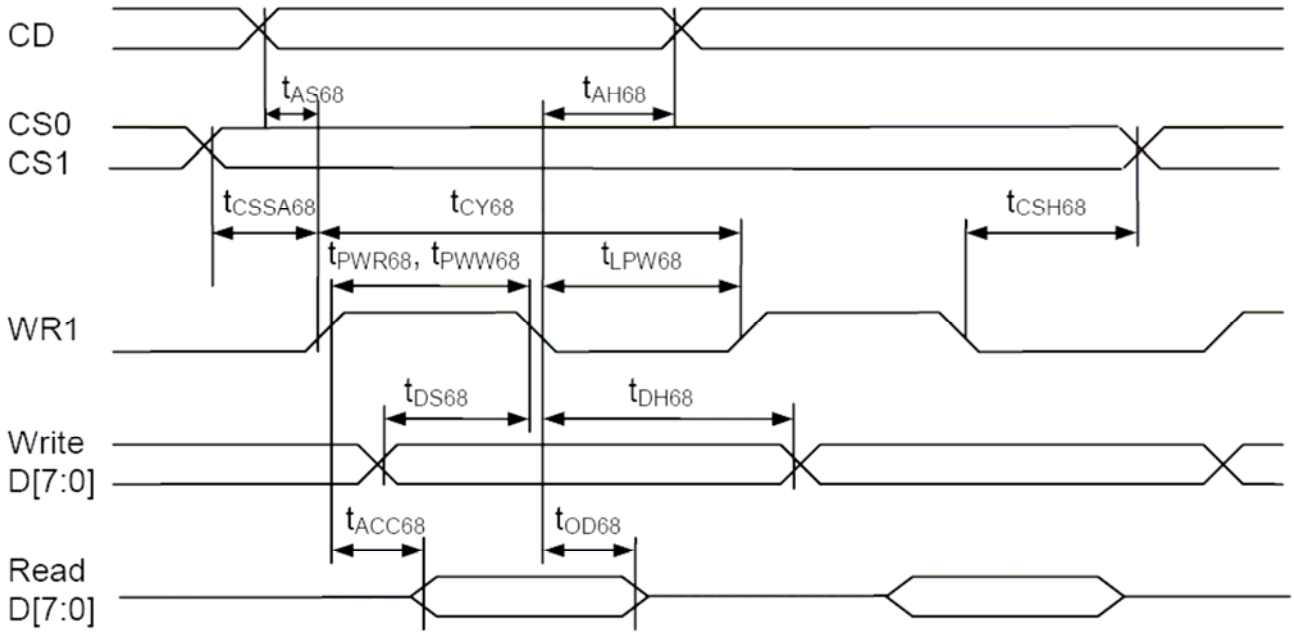


Figure 4: Parallel Bus Timing Characteristics (for 6800 MCU)

5.2.3 Serial Bus Timing Characteristics (for S8)

At Ta =-20 °C To +70 °C, VDD= 2.8V, GND=0V.

Table 8

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS8}	CD	Address setup time		0	–	nS
t_{AHS8}		Address hold time		15	–	nS
t_{CYS8}	SCK	System cycle time		80	–	nS
t_{LPWS8}		Low pulse width		35	–	nS
t_{HPWS8}		High pulse width		35	–	nS
t_{DSS8} t_{DHS8}	SDA	Data setup time Data hold time		30 20	–	nS
t_{CSSAS8} t_{CSHS8}	CS1/CS0	Chip select setup time		5 5		nS

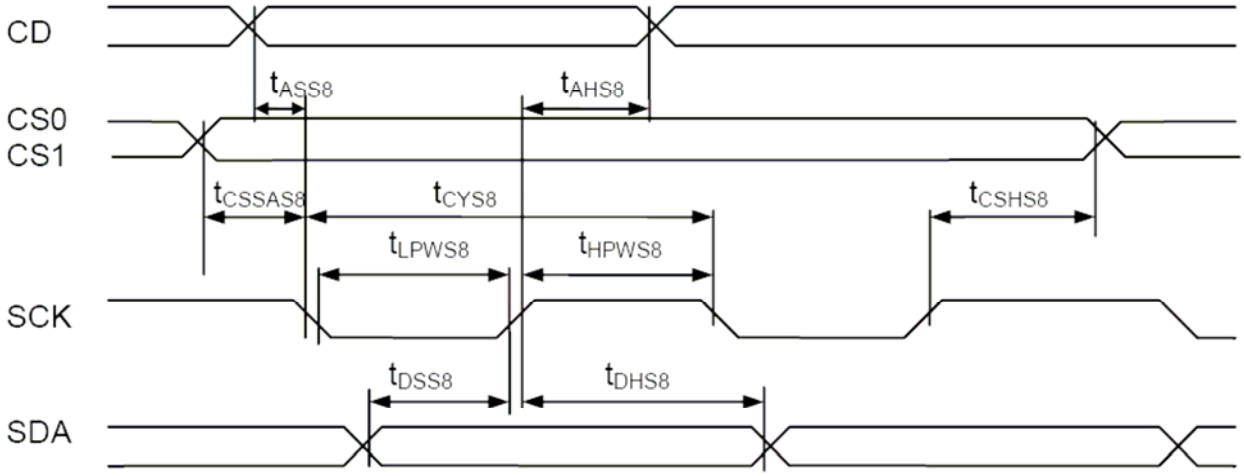


Figure 5: Serial Bus Timing Characteristics (for S8)

5.2.4 Serial Bus Timing Characteristics (for S9)

At Ta =-20 °C To +70 °C, VDD= 2.8V, GND=0V.

Table 9

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{CYS9}	SCK	System cycle time		80	–	nS
t_{LPWS9}		Low pulse width		35	–	nS
t_{HPWS9}		High pulse width		35	–	nS
t_{DSS9} t_{DHS9}	SDA	Data setup time Data hold time		30 20	–	nS
t_{CSSAS9} t_{CSHS9}	CS1/CS0	Chip select setup time		5 5		nS

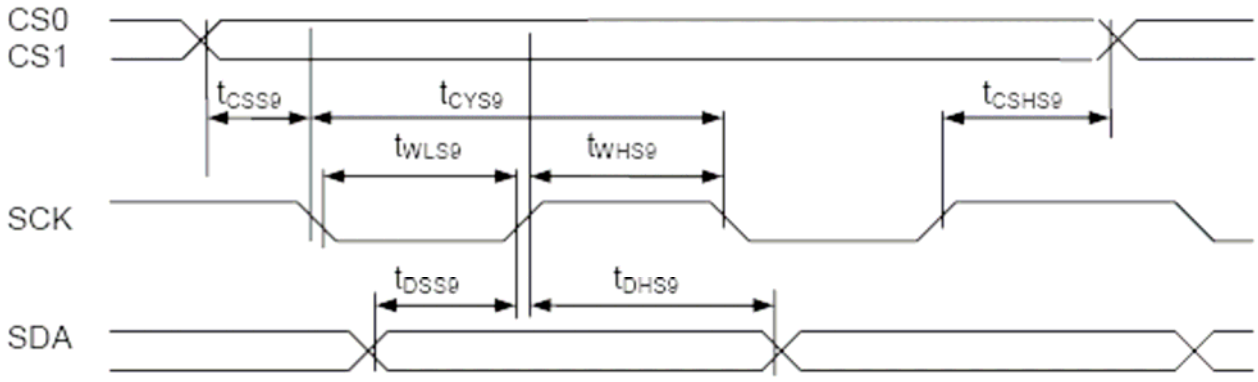


Figure 6: Serial Bus Timing Characteristics (for S9)

5.2.5 Reset Input Timing

At Ta =-20 °C To +70 °C, VDD=2.8V, GND=0V.

Table 10

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{RW}	RST	Reset low pulse width		3	–	μS
t_{RD}	RST, WR	Reset to WR pulse delay		10		mS

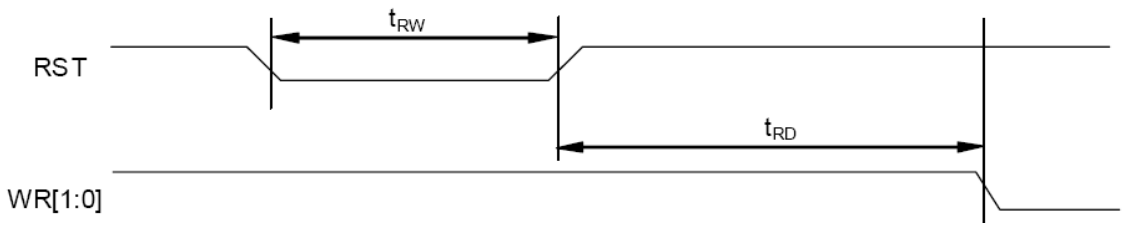
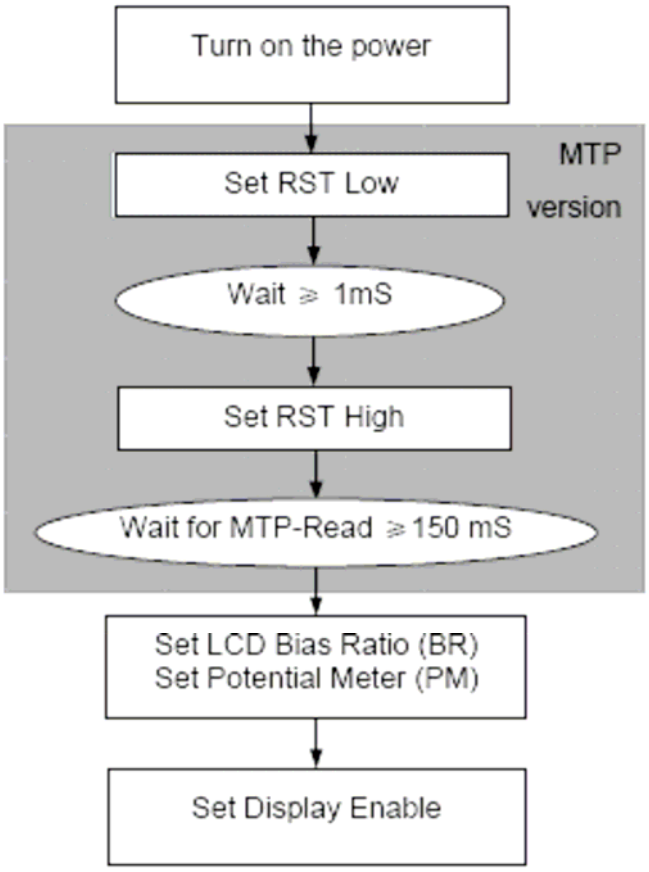


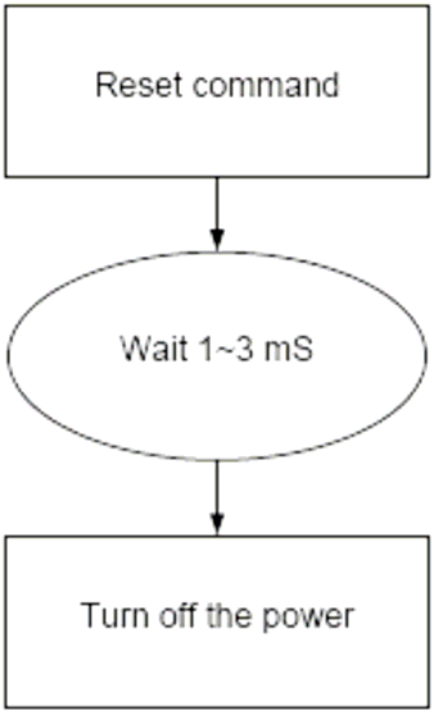
Figure 7: Reset Input Timing

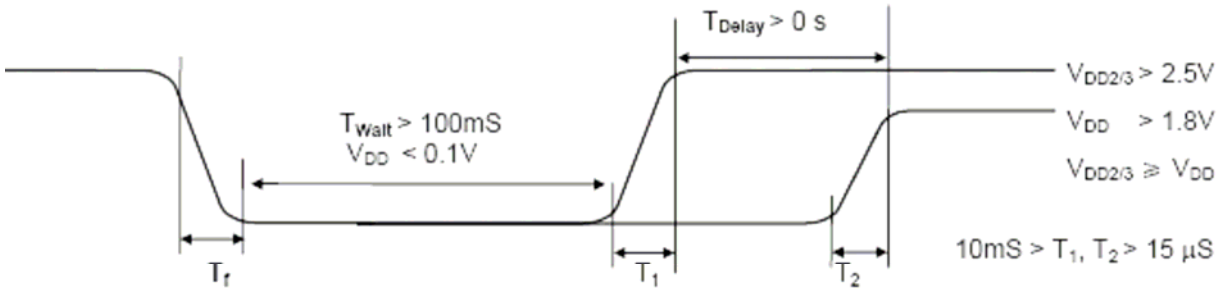
5.3 Power-up/ down sequence

Power-up sequence



Power-down sequence



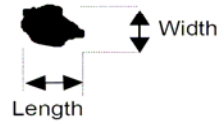
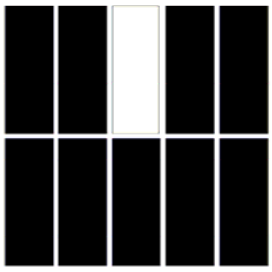
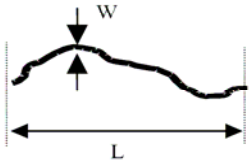
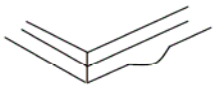
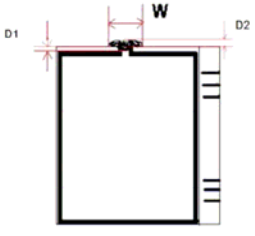


Delay allowance and Power Off-On Sequence

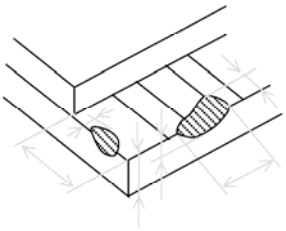
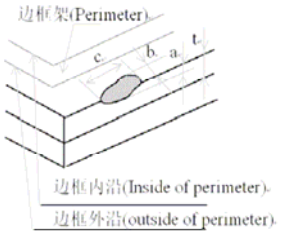
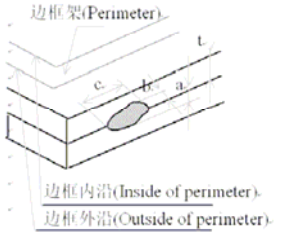
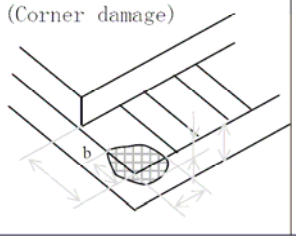
6. Electrical & Optical Characteristics

(TBD)

7. CSTN Panel Inspection Specifications

壞品名稱 Failure mode	圖例說明 Illustration	分类 Category(Unit: mm)		可接受数量 Acceptable count	
				可视区 Viewing area	非可视区 non-Viewing area
黑點 Black spot 白點 White spot	 Φ= (Length+width)/2	A	Φ≦0.10	不计 Not count	不计 Not count
		B	0.10<Φ≦0.15	2, 两点间距离不小于 5mm The gap between the two spots should be 5 mm and above.	
		C	0.15<Φ≦0.20	1	
		D	0.20<Φ	0	
亮點(因爲濾光片損壞造成的紅點，綠點，藍點等) Bright spot (Red spot, green spot and blue spot caused by damaged colour filter)		A	缺陷面積小於或等於一個單基色面積 Area≦1 sub-pixel	1	N/A
黑线 Black line 白线 White line		A	W≦0.03	不计 Not count	不计 Not count
		B	0.03<W≦0.05, L≦3.0	2	
		C	0.05<W	按黑白点判定 Judged by spot spec	
以下为外观标准(Below are cosmetic inspection specifications)					
玻璃毛刺 Excess glass		b≦1.0 且不影响外形尺寸及装配(注意COG工序对b的要求，不同尺寸LCD的b都不同) b≦1.0, this defect shall not affect the outline dimension or assembly process.(Remarks: For COG process, the defect size is decided by the dimension of LCD panel.)			
		不影响外形尺寸及装配. This defect shall not affect the outline dimension or assembly process.			
进胶尺寸 The depth of UV glue entered in LCD cell		進膠深度大於等於 0.2mm 且不可進入視域范圍，膠水凸出玻璃邊高度小于等于 0.8mm,长度=（注入口宽度）+（2~6 mm） a. D1≥0.2，not enter into viewing area b. D2≦0.8, c. W=End mouth width + (2~6 mm)			

<table>
<tr><td rowspan="5">玻璃缺陷划伤、缺损

Glass defect
(scratch, damage)</td><td>①台阶破损(LCD ledge damage)
  </td><td colspan="2">分类 Category</td></tr>
<tr><td>A</td><td>非电极区，台阶破损不得影响装配及外形尺寸
The defect shall not affect the outline dimension or assembly process at non ITO zone.</td></tr>
<tr><td>B</td><td>电极区的破损，b 不得超过邦定电极长度（该长度应不小于 1.2mm）的 1/4, a、c 方向不限制
b≦1/4w, a & c not count (at ITO zone)</td></tr>
<tr><td>C</td><td>台阶两侧的缺损不得损伤对位标识或走线
Alignment mark on LCD ledge shall not be damaged.</td></tr>
<tr><td>②非封接面破损 (Outside of perimeter damage)
 
</td><td colspan="2">b 方向破损不得到达边框内沿
b can't reach inside of perimeter.</td></tr>
<tr><td>③ 封接面破损
(Joint glass damage)
 
</td><td colspan="2">b 方向破损不得到达边框外沿或走线
b can't reach outside of perimeter or ITO layout.</td></tr>
<tr><td rowspan="2">④角上破损
(Corner damage)
 
</td><td>A</td><td>a ≦ t， b ≦ 3.0， c ≦ 3.0</td></tr>
<tr><td colspan="2">B. 玻璃破损不允许损伤电极图形和/或对位标识
Alignment mark on LCD ledge shall not be damaged.</td></tr>
<tr><td colspan="3">注：a:表示崩角厚度；b:表示崩角深度；c:表示崩角长度；t:表示单片玻璃厚度；单位：mm
Remark: a stands for thickness of damage, b for width, c for length and t for glass thickness. (Unit: mm)</td></tr>
</table>

8. Remark

HANDLING LCD AND LCD MODULES

1. Liquid Crystal Display (LCD)

LCD is made up of glass, organic sealant, organic fluid and polymer based polarizers. The following precautions should be taken when handling:

(1) Keep the temperature within range for use and storage. Excessive temperature and humidity could cause polarization degredation, polarizer peel-off or bubble generation. When storage for a long period over 40° C is required, the relative humidity should be kept below 60%.
(2) Do not contact the exposed polarizers with anything harder than an HB pencil lead. To clean dust off the display surface, wipe gently with cotton, chamois or other soft material soaked in petroleum benzin. Never scrub hard.
(3) Varitronix does not responsible for any polarizer defect after the protective film has been removed from the display
(4) Wipe off saliva or water drops immediately. Contact with water over a long period of time may cause polarizer deformation or color fading, while an active LCD with water condensation on its surface will cause corrosion of ITO electrodes.
(5) PETROLEUM BENZIN is recommended to remove adhesives used to attach front/rear polarizers and reflectors, while chemicals like acetone, toluene, ethanol and isopropyl alcohol will cause damage to the polarizer. Avoid oil and fats. Avoid lacquer and epoxies which might contain solvents and hardeners to cause electrode errosion. Some solvents will also soften the epoxy covering the DIL pins and thereby weakening the adhesion of the epoxy on glass. This will cause the exposed electrodes to erode electrochemically when operating in high humidity and condensing environment.
(6) Glass can be easily chipped or cracked from rough handling, especially at corners and edges.
(7) Do not drive LCD with DC voltage.
(8) When soldering DIL pins, avoid excessive heat and keep soldering temperature between 260°C to 300°C for no more than 5 seconds. Never use wave or reflow soldering.

2. Liquid Crystal Display Modules (MDL)

2.1 Mechanical Considerations

MDL's are assembled and adjusted with a high degree of precision. Avoid excessive shocks and do not make any alterations or modifications. The following should be noted.
(1) Do not tamper in any way with the tabs on the metal frame.
(2) Do not modify the PCB by drilling extra holes, changing its outline, moving its components or modifying its pattern.
(3) Do not touch the elastomer connector (conductive rubber), especially when inserting an EL panel.
(4) When mounting a MDL make sure that the PCB is not under any stress such as bending or twisting. Elastomer contacts are very delicate and missing pixels could result from slight dislocation of any of the elements.
(5) Avoid pressing on the metal bezel, otherwise the elastomer connector could be deformed and lose contact, resulting in missing pixels.
(6) If FPCA need to be bent, please refer the suggested bending area on the specification. The stiffener and component area on FPC/FFC/COF must not be bent during or after assembly (Note: for those models with FPC/FFC/COF +stiffener).
(7) Sharp bending should be avoided on FPC to prevent track cracking.

2.2 Static Electricity

MDL contains CMOS LSI's and the same precaution for such devices should apply, namely:

(1) The operator should be grounded whenever he comes into contact with the module. Never touch any of the conductive parts such as the LSI pads, the copper leads on the PCB and the interface terminals with any part of the human body.
(2) The modules should be kept in antistatic bags or other containers resistant to static for storage.
(3) Only properly grounded soldering irons should be used.
(4) If an electric screwdriver is used it should be well grounded and shielded from commutator sparks.
(5) The normal static prevention measures should be observed for work clothes and working benches; for the latter conductive (rubber) mat is recommended.
(6) Since dry air is inducive to statics, a relative humidity of 50 - 60% is recommended.

2.3 Soldering

(1) Solder only to the I/O terminals.
(2) Use only soldering irons with proper grounding and no leakage.
(3) Soldering temperature is 280°C ± 10°C .
(4) Soldering time: 3 to 4 seconds.
(5) Use eutectic solder with resin flux fill.
(6) If flux is used. the LCD surface should be covered to avoid flux spatters. Flux residue should be removed afterwards.
(7) Use proper de-soldering methods (e.g. suction type desoldering irons) to remove lead wires from the I/O terminals when necessary. Do not repeat the soldering/ desoldering process more than three times as the pads and plated through holes may be damaged.

2.4 Label

Identification labels will be stuck on the module without obstructing the viewing area of display.

3. Operation

(1) The viewing angle can be adjusted by varying the LCD driving voltage Vo.
(2) Driving voltage should be kept within specified range, excess voltage shortens display life.
(3) Response time increases with decrease in temperature.
(4) Display may turn black or dark Blue at temperatures above its operational range; this is however not destructive and the display will return to normal once the temperature falls back to range.
(5) Mechanical disturbance during operation (such as pressing on the viewing area) may cause the segments to appear "fractured". They will recover once the display is turned off.
(6) Condensation at terminals will cause malfunction and possible electrochemical reaction. Relative humidity of the environment should therefore be kept below 60%.
(7) Display performance may vary out of viewing area. If there is any special requirement on performance out of viewing area, please consult Varitronix.

4. Storage and Reliability

(1) LCD's should be kept in sealed polyethylene bags while MDL's should use antistatic ones. If properly sealed, there is no need for desiccant.
(2) Store in dark places and do not expose to sunlight or fluorescent light. Keep the temperature between 0°C and 35°C and the relative humidity low. Please consult MULTI-INNO for other storage requirements.
(3) Water condensation will affect reliability performance of the display and is not allowed.
(4) Semi-conductor device on the display is sensitive to light and should be protected properly.
(5) Power up/down sequence.
   a) Power Up: in general, LCD supply voltage, Vo must be supplied after logic voltage, VDD becomes steady. Please refer to related IC data sheet for details.
   b) Power Down: in general, LCD supply voltage, Vo must be removed before logic voltage, VDD turns off. Please refer to related IC data sheet for details.

5. Safety

If any fluid leaks out of a damaged glass cell, wash off any human part that comes into contact with soap and water. Never swallow the fluid. The toxicity is extremely low but caution should be exercised at all times.

LIMITED WARRANTY

MULTI-INNO LCDs and modules are not consumer products, but may be incorporated by MULTI-INNO 's customers into consumer products or components thereof. MULTI-INNO does not warrant that its LCDs and components are fit for any such particular purpose.

1. The liability of MULTI-INNO is limited to repair or replacement on the terms set forth below. MULTI-INNO will not be responsible for any subsequent or consequential events or injury or damage to any personnel or user including third party personnel and/or user.

   Unless otherwise agreed in writing between MULTI-INNO and the customer, MULTI-INNO will only replace or repair any of its LCD which is found defective electrically or visually when inspected in accordance with MULTI-INNO LCD Acceptance Standards (copies available on request), for a period of one year from the date of shipment. Confirmation of such date shall be based on freight documents.

2. No warranty can be granted if any of the precautions stated in HANDLING LCD and LCD Modules above have been disregarded. Broken glass, scratches on polarizers, mechanical damages as well as defects that are caused by accelerated environmental tests are excluded from warranty.
3. In returning the LCD and Modules, they must be properly packaged and there should be detailed description of the failures or defects.

IMPORTANT NOTICE

The information presented in this document has been carefully checked and is believed to be accurate, however, no responsibility is assumed for inaccuracies. MULTI-INNO reserves the right to make changes to any specifications without further notice for performance, reliability, production technique and other considerations, MULTI-INNO does not assume any liability arising out of the application or use of products herein. Please see Limited Warranty in the previous section.