MIC22705

1 MHz, 7A Integrated Switch, High Efficiency Synchronous Buck Regulator

Features

- Input Voltage Range: 2.9V to 5.5V
- Output Voltage Adjustable Down to 0.7V
- Output Load Current Up to 7A
- Safe Start-Up into a Pre-Biased Output Load
- Full Sequencing and Tracking Ability
- Power Good Output
- Efficiency >95% Across a Broad Load Range
- Ultra-Fast Transient Response
- Easy RC Compensation
- 100% Maximum Duty Cycle
- Fully Integrated MOSFET Switches
- Thermal Shutdown and Current-Limit Protection
- 24-Pin 4 mm x 4 mm QFN
- –40°C to +125°C Junction Temperature Range

Applications

- High Power Density Point-of-Load Conversion
- Servers, Routers, and Base Stations
- Blu-Ray/DVD Players and Recorders
- Computing Peripherals
- FPGAs, DSP, and Low Voltage ASIC Power

General Description

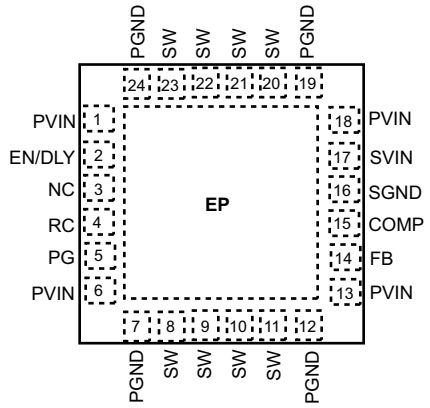
The MIC22705 is a highly efficient, 7A, integrated switch, synchronous buck (step-down) regulator. The MIC22705 is optimized for highest efficiency, achieving more than 95% efficiency while still switching at 1 MHz over a broad range. The ultra-high speed control loop keeps the output voltage within regulation even under extreme transient load swings commonly found in FPGAs and low-voltage ASICs. The output voltage is pre-bias safe and can be adjusted down to 0.7V to address all low-voltage power needs.

The MIC22705 offers a full range of sequencing and tracking options. The Enable/Delay (EN/DLY) pin, combined with the Power Good (PG) pin, allows multiple outputs to be sequenced in any way during turn-on and turn-off. The Ramp Control (RC) pin allows the device to be connected to another product in the MIC22xxx and/or MIC68xxx family, to keep the output voltages within a certain ΔV on start-up.

The MIC22705 is available in a 24-pin 4mm x 4mm QFN with a junction operating range from –40°C to +125°C.

Package Type

MIC22705
24-Lead 4 mm x 4 mm QFN (ML)
(Top View)



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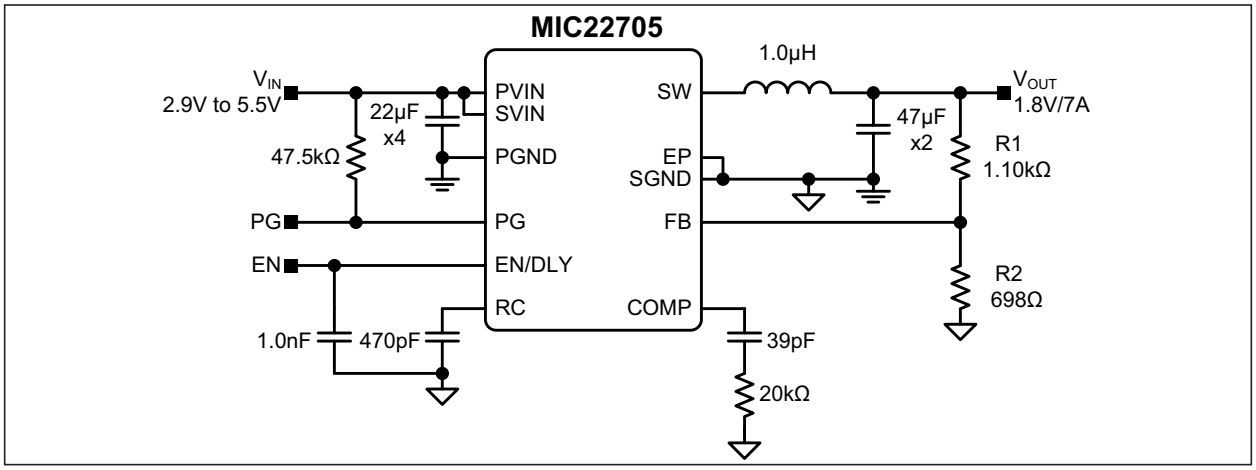
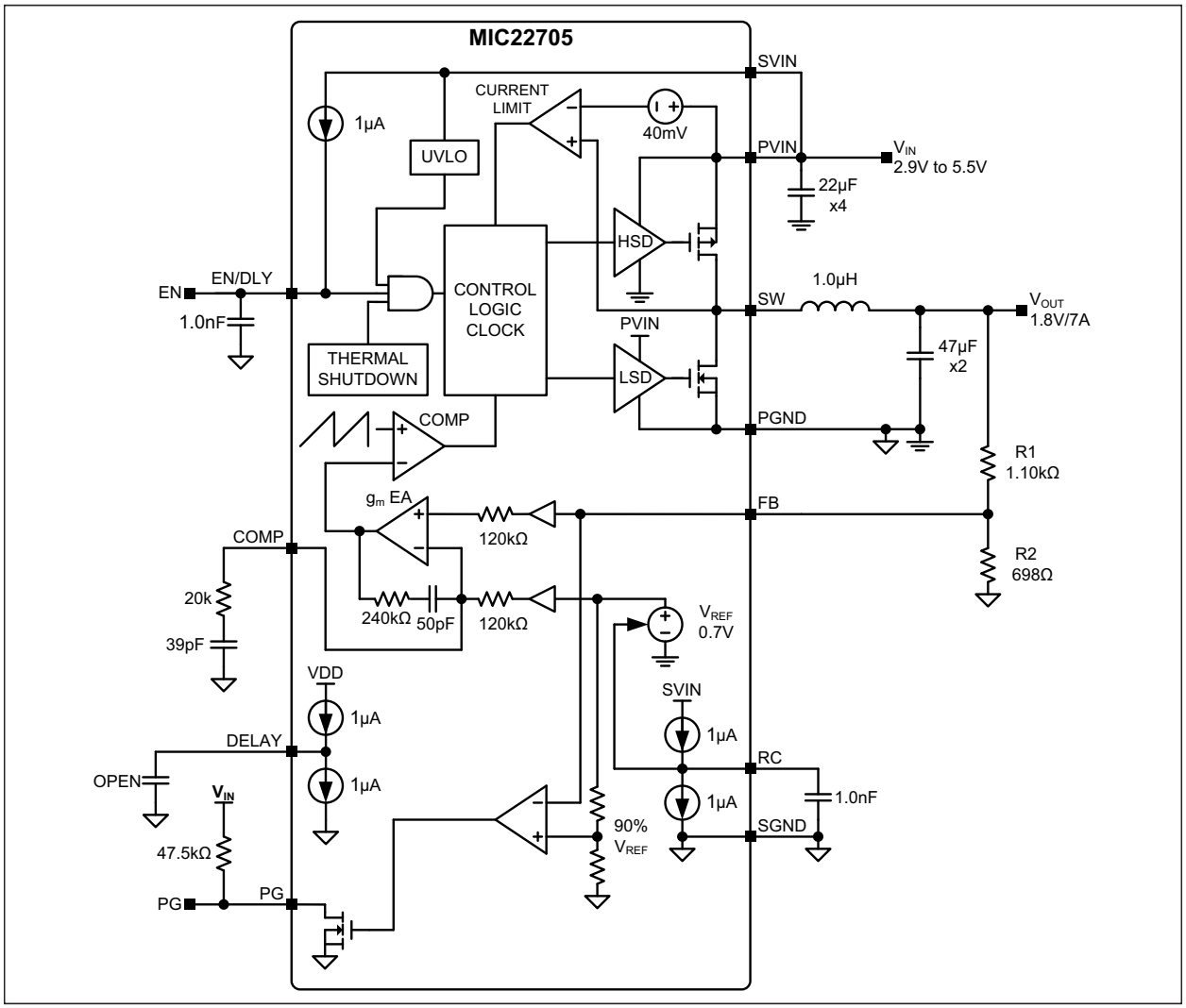
Typical Application Circuit



Functional Block Diagram



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

PV_{IN} to PGND ..... –0.3V to +6V
SV_{IN} to PGND ..... –0.3V to PV_{IN}
V_{SW} to PGND ..... –0.3V to PV_{IN}
$V_{EN/DLY}$ to PGND ..... –0.3V to PV_{IN}
V_{PG} to PGND ..... –0.3V to PV_{IN}
PGND to SGND ..... –0.3V to +0.3V
ESD Rating ..... Note 1

Operating Ratings ††

Supply Voltage ..... +2.9V to +5.5V
Power Good Voltage (V_{PG}) ..... 0V to PV_{IN}
Enable Input ($V_{EN/DLY}$) ..... 0V to PV_{IN}

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† Notice: The device is not guaranteed to function outside its operating ratings.

Note 1: Devices are ESD sensitive. Handling precautions recommended.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: $SV_{IN} = PV_{IN} = V_{EN/DLY} = 3.3V$, $V_{OUT} = 1.8V$, $T_A = +25°C$, unless noted. **Bold** values indicate $–40°C \leq T_J \leq +125°C$. Note 1

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Power Input Supply						
Supply Voltage Range	PV_{IN}	**2.9**	—	**5.5**	V	—
UVLO Trip Level	—	**2.55**	2.75	**2.9**	V	PV_{IN} rising
UVLO Hysteresis	—	—	420	—	mV	—
Quiescent Supply Current	—	—	0.85	**1.3**	mA	$V_{FB} = 0.9V$ (not switching)
Shutdown Current	I_{SHDN}	—	5	**10**	µA	$V_{EN/DLY} = 0V$
Reference						
Feedback Voltage	V_{FB}	**0.686**	0.7	**0.714**	V	—
FB Bias Current	—	—	10	—	nA	$V_{FB} = 0.5V$
Load Regulation	—	—	0.2	—	%	I_{OUT} = 100 mA to 7A
Line Regulation	—	—	0.2	—	%	V_{IN} = 2.9V to 5.5V; I_{OUT} = 100 mA
Enable Control						
EN/DLY Threshold Voltage	—	**1.14**	1.24	**1.34**	V	—
EN Hysteresis	—	—	10	—	mV	—
EN/DLY Bias Current	—	**0.6**	1.0	**1.8**	µA	$V_{EN/DLY} = 0.5V$; V_{IN} = 2.9V and V_{IN} = 5.5V
RC Ramp Control						
RC Pin Source Current	I_{RAMP}	0.5	1	1.7	µA	$V_{RC} = 0.35V$

Note 1: Specification for packaged product only.

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ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: SV_{IN} = PV_{IN} = $V_{EN/DLY}$ = 3.3V, V_{OUT} = 1.8V, T_A = +25°C, unless noted. **Bold** values indicate –40°C≤ T_J ≤ +125°C. Note 1

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Oscillator						
Switching Frequency	f_{SW}	0.8	1.0	1.2	MHz	—
Maximum Duty Cycle	—	100	—	—	%	V_{FB} ≤ 0.5V
Short-Circuit Protection						
Current Limit	I_{LIM}	**7**	11	**21**	A	V_{FB} = 0.5V
Internal FETs						
Top MOSFET $R_{DS(ON)}$	—	—	30	—	mΩ	V_{FB} = 0.5V, I_{SW} = 1A
Bottom MOSFET $R_{DS(ON)}$	—	—	25	—	mΩ	V_{FB} = 0.9V, I_{SW} = –1A
SW Leakage Current	—	—	—	**60**	µA	PV_{IN} = 5.5V, V_{SW} = 5.5V, V_{EN} = 0V
V_{IN} Leakage Current	—	—	—	**25**	µA	PV_{IN} = 5.5V, V_{SW} = 0V, V_{EN} = 0V
Power Good (PG)						
PG Threshold	—	–7.5	–10	–12.5	%	Threshold % of V_{FB} from V_{REF}
Hysteresis	—	—	2.0	—	%	—
PG Output Low Voltage	—	—	144	—	mV	I_{PG} = 5 mA (sinking), $V_{EN/DLY}$ = 0V
PG Leakage Current	—	—	1.0	**2.0**	µA	V_{PG} = 5.5V; V_{FB} = 0.9V
Thermal Protection						
Overtemperature Shutdown	—	—	160	—	°C	T_J rising
Overtemperature Shutdown Hysteresis	—	—	20	—	°C	—

Note 1: Specification for packaged product only.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Junction Temperature Range	T_J	–40	—	+125	°C	—
Maximum Junction Temperature	$T_{J(MAX)}$	—	—	+150	°C	—
Storage Temperature Range	T_S	–65	—	+150	°C	—
Lead Temperature	—	—	+260	—	°C	Soldering, 10 sec.
Package Thermal Resistance						
Thermal Resistance, QFN 24-Ld	θ_{JC}	—	14	—	°C/W	—
	θ_{JA}	—	40	—	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

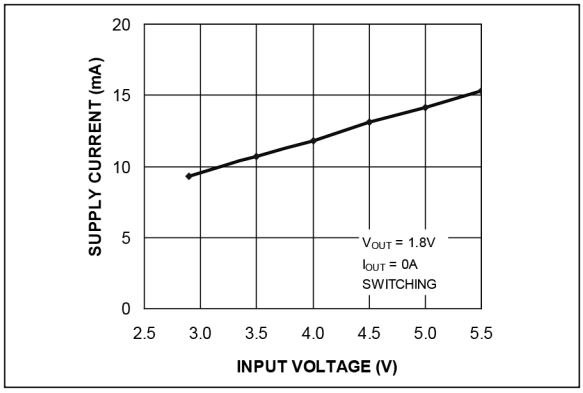

FIGURE 2-1: *V_{IN} Operating Supply Current vs. Input Voltage.*

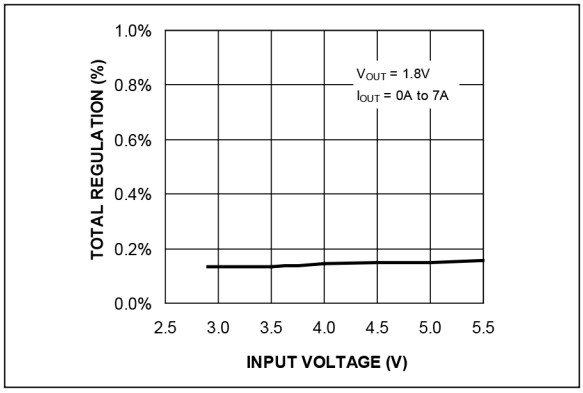

FIGURE 2-4: *Load Regulation vs. Input Voltage.*

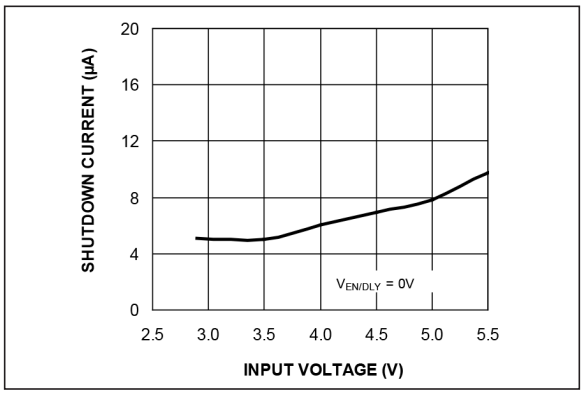

FIGURE 2-2: *V_{IN} Shutdown Current vs. Input Voltage.*

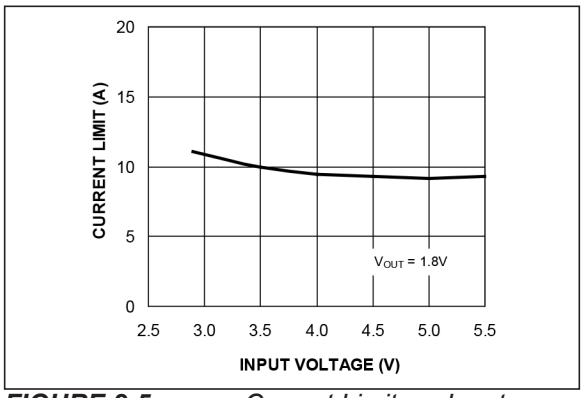

FIGURE 2-5: *Current Limit vs. Input Voltage.*

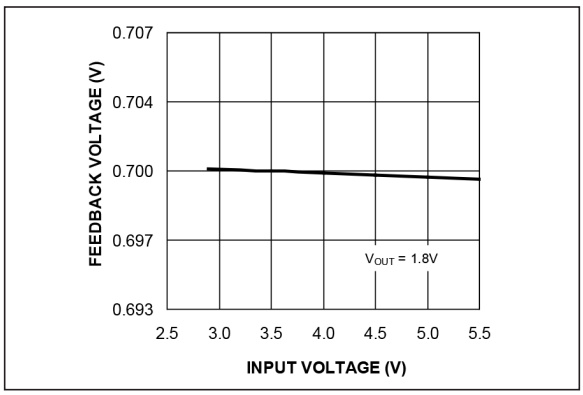

FIGURE 2-3: *Feedback Voltage vs. Input Voltage.*

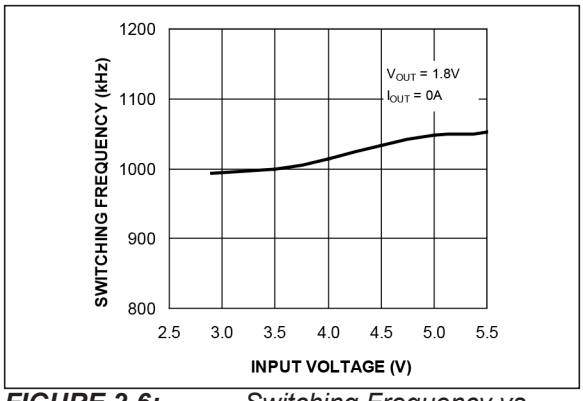

FIGURE 2-6: *Switching Frequency vs. Input Voltage.*

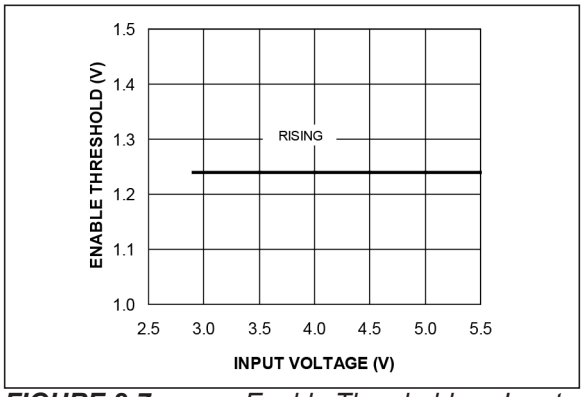

FIGURE 2-7: *Enable Threshold vs. Input Voltage.*

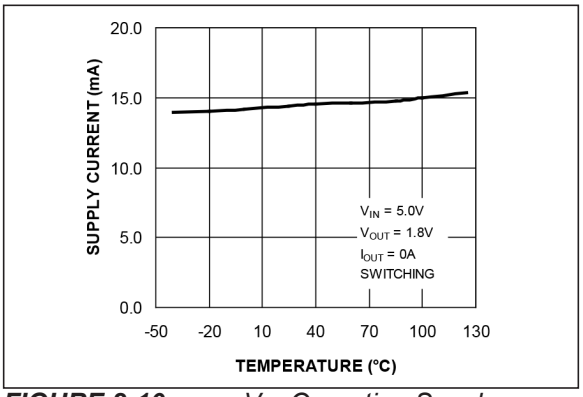

FIGURE 2-10: *V_{IN} Operating Supply Current vs. Temperature.*

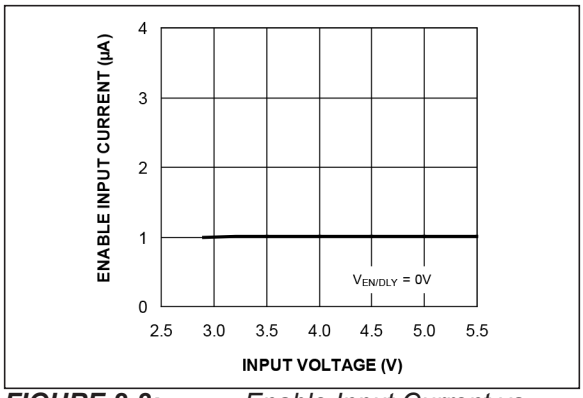

FIGURE 2-8: *Enable Input Current vs. Input Voltage.*

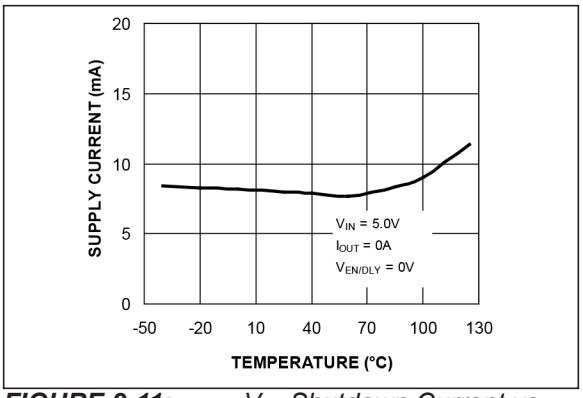

FIGURE 2-11: *V_{IN} Shutdown Current vs. Temperature.*

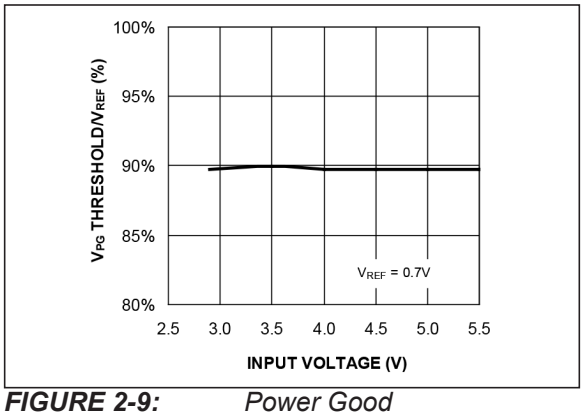

FIGURE 2-9: *Power Good Threshold/V_{REF} Ratio vs. Input Voltage.*

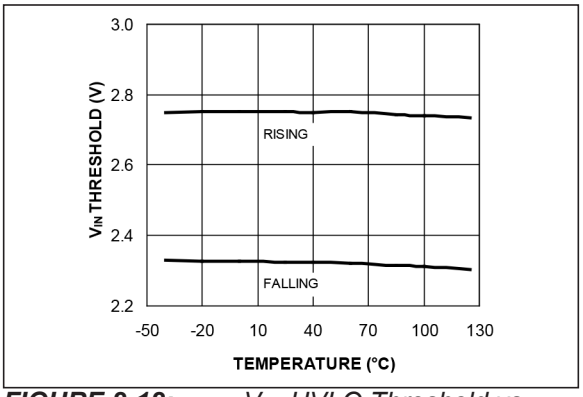

FIGURE 2-12: *V_{IN} UVLO Threshold vs. Temperature.*

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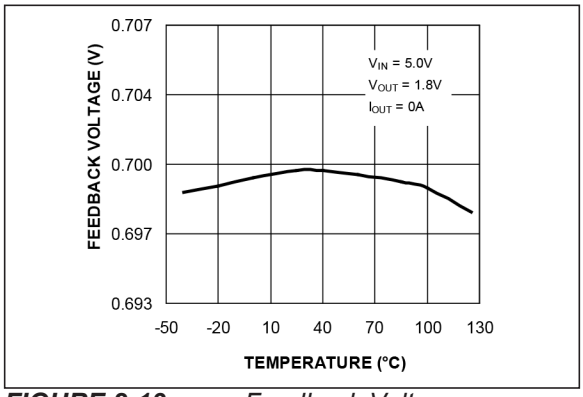

FIGURE 2-13: *Feedback Voltage vs. Temperature.*

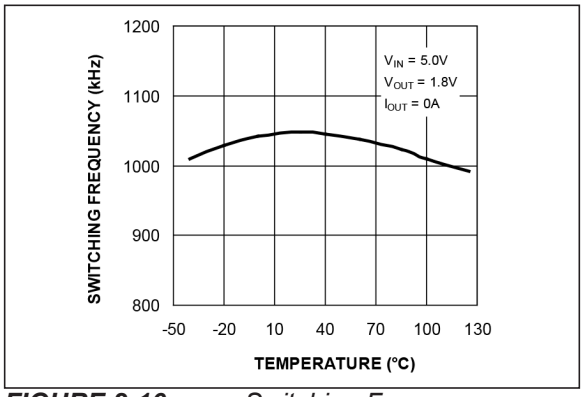

FIGURE 2-16: *Switching Frequency vs. Temperature.*

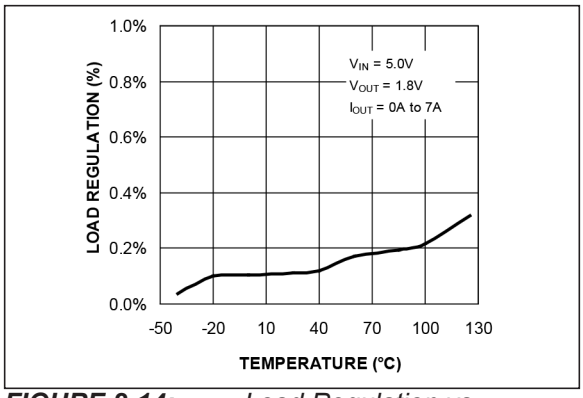

FIGURE 2-14: *Load Regulation vs. Temperature.*

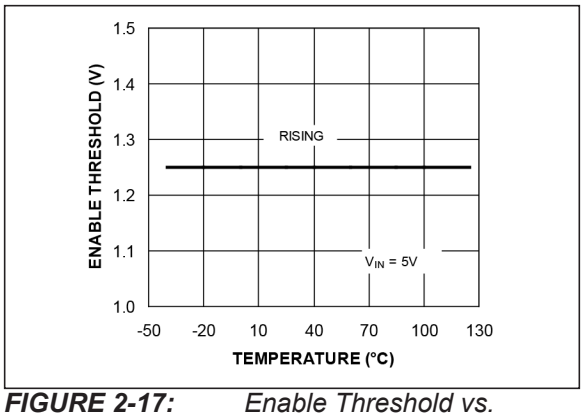

FIGURE 2-17: *Enable Threshold vs. Temperature.*

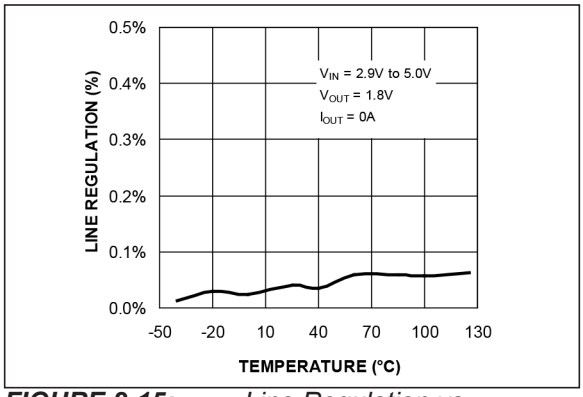

FIGURE 2-15: *Line Regulation vs. Temperature.*

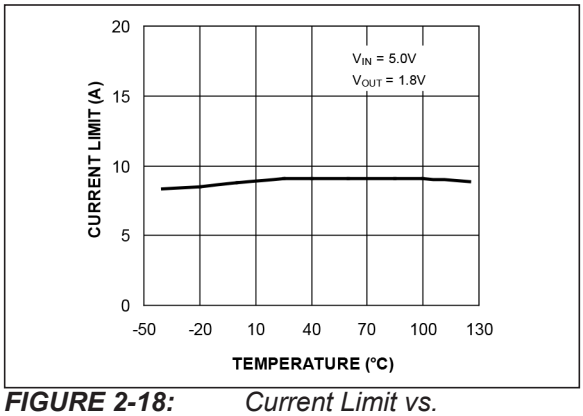

FIGURE 2-18: *Current Limit vs. Temperature.*

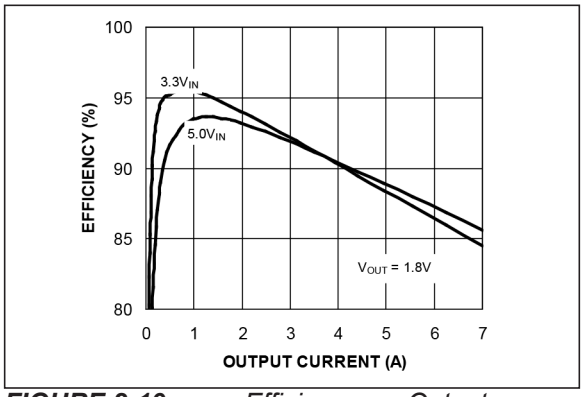

FIGURE 2-19: *Efficiency vs. Output Current.*

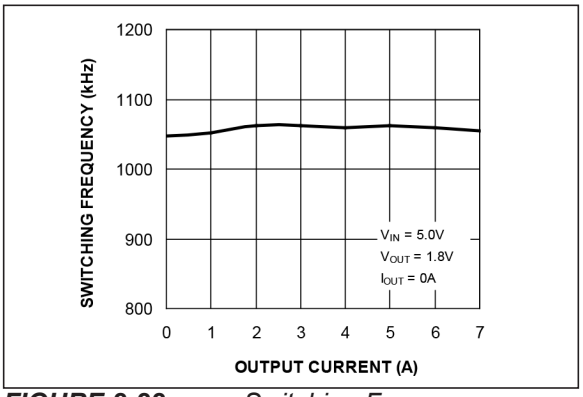

FIGURE 2-22: *Switching Frequency vs. Output Current.*

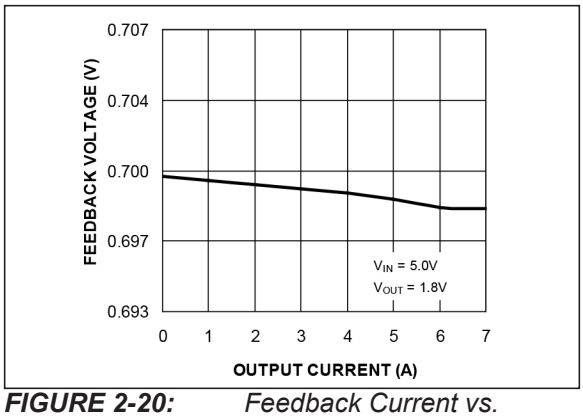

FIGURE 2-20: *Feedback Current vs. Output Current.*

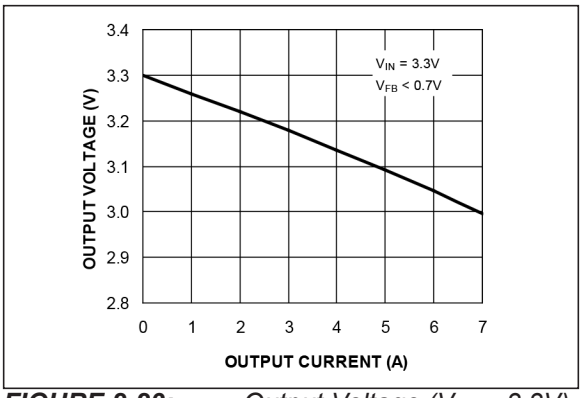

FIGURE 2-23: *Output Voltage (V_{IN} = 3.3V) vs. Output Current.*

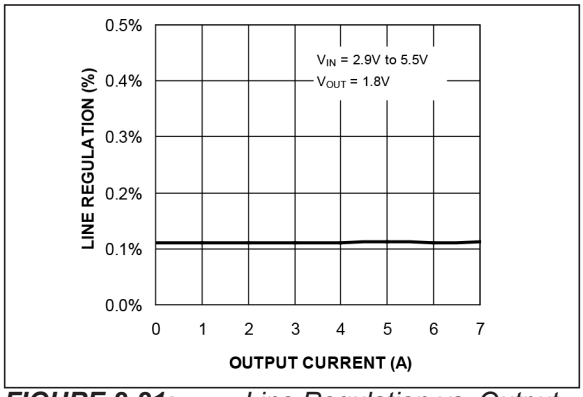

FIGURE 2-21: *Line Regulation vs. Output Current.*

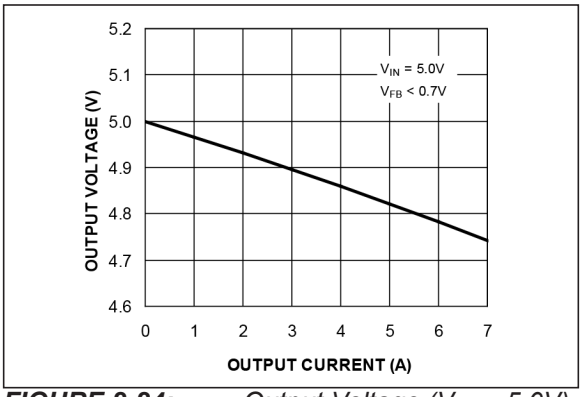

FIGURE 2-24: *Output Voltage (V_{IN} = 5.0V) vs. Output Current.*

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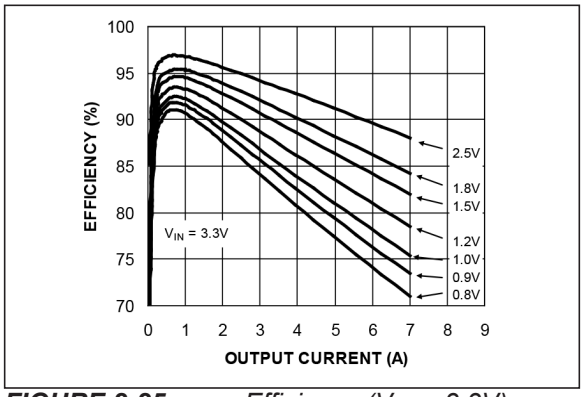

FIGURE 2-25: *Efficiency (V_{IN} = 3.3V) vs. Output Current.*

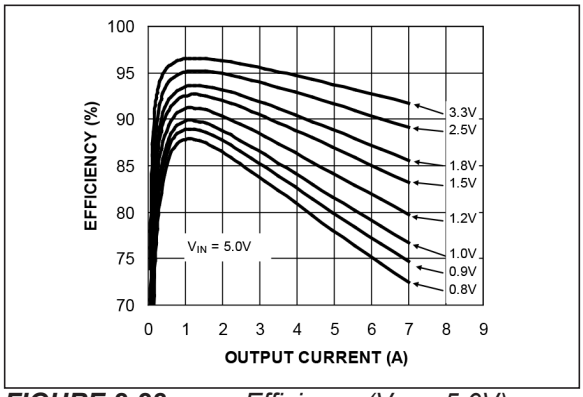

FIGURE 2-28: *Efficiency (V_{IN} = 5.0V) vs. Output Current.*

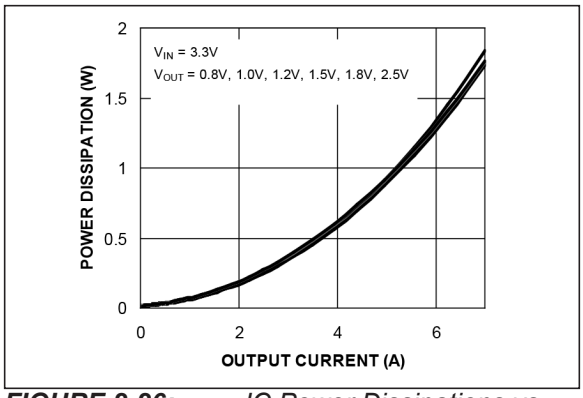

FIGURE 2-26: *IC Power Dissipations vs. Output Current (V_{IN} = 3.3V).*

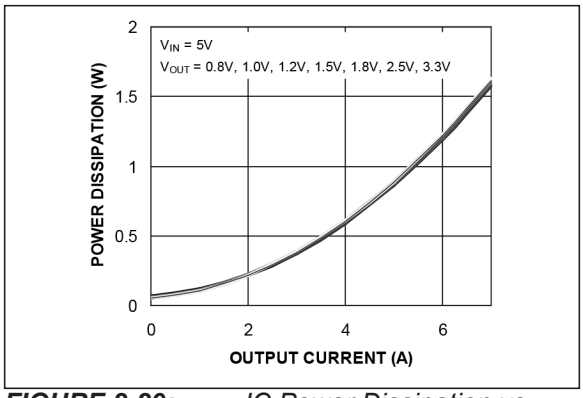

FIGURE 2-29: *IC Power Dissipation vs. Output Current (V_{IN} = 5.0V).*

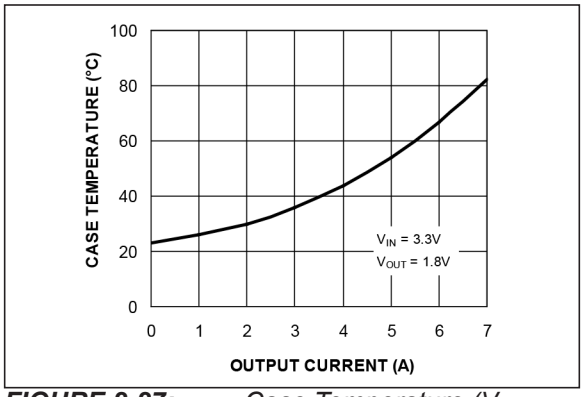

FIGURE 2-27: *Case Temperature (V_{IN} = 3.3V) vs. Output Current.*

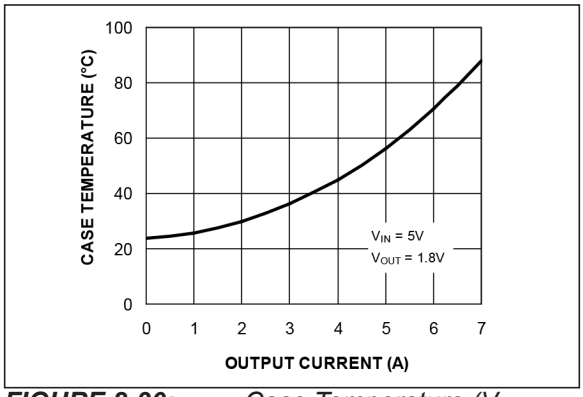

FIGURE 2-30: *Case Temperature (V_{IN} = 5.0V) vs. Output Current.*

For Figure 2-27 and Figure 2-30, the temperature measurement was taken at the hottest point on the MIC22705 case and mounted on a five-square inch PCB (see Thermal Measurements section). Actual results will depend upon the size of the PCB, ambient temperature, and proximity to other heat-emitting components.

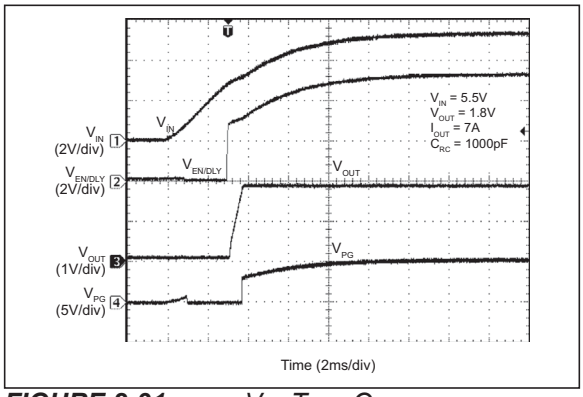

FIGURE 2-31: *V_{IN} Turn-On.*

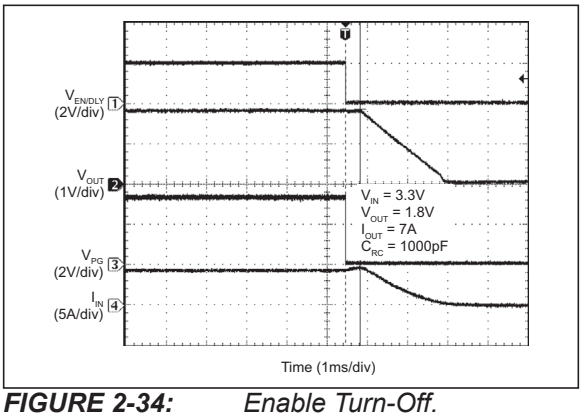

FIGURE 2-34: *Enable Turn-Off.*

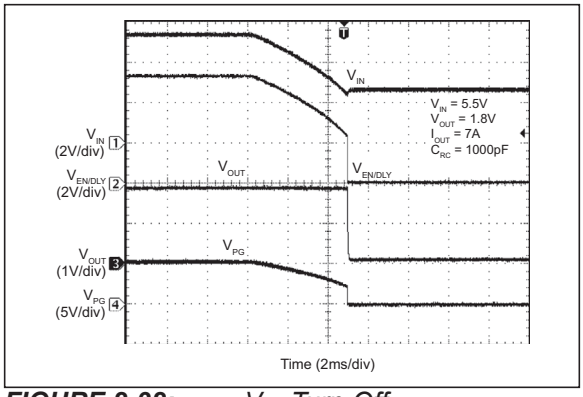

FIGURE 2-32: *V_{IN} Turn-Off.*

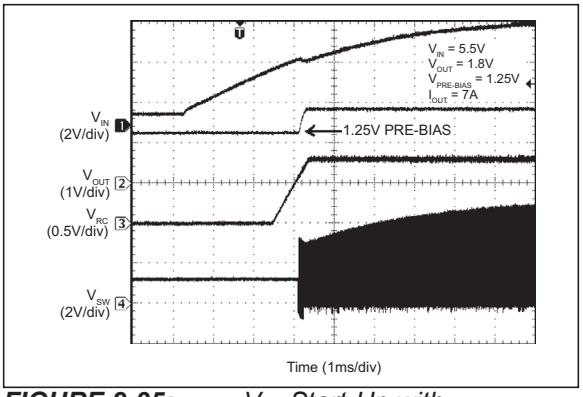

FIGURE 2-35: *V_{IN} Start-Up with Pre-Biased Output.*

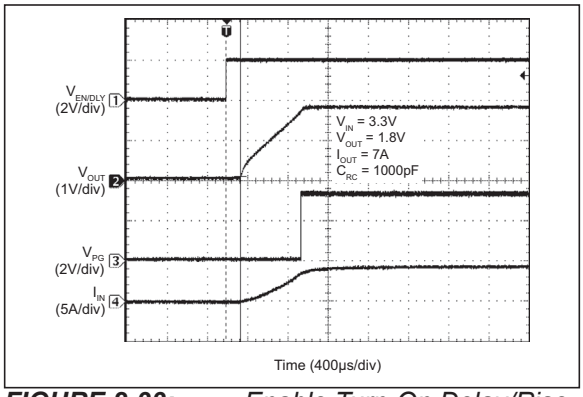

FIGURE 2-33: *Enable Turn-On Delay/Rise Time.*

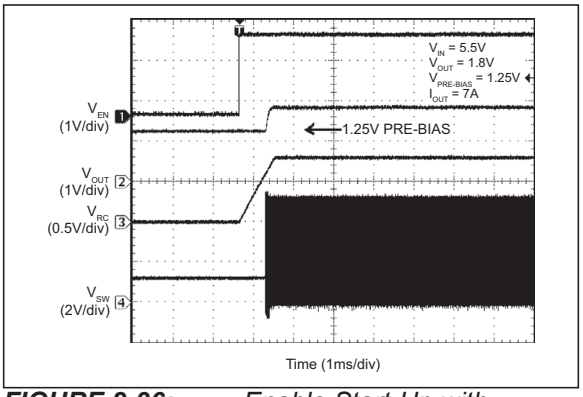

FIGURE 2-36: *Enable Start-Up with Pre-Biased Output.*

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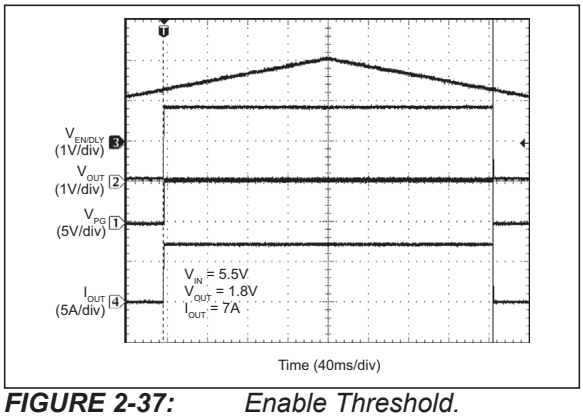

FIGURE 2-37: *Enable Threshold.*

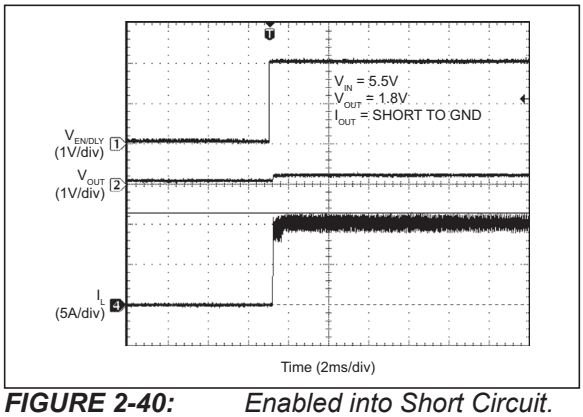

FIGURE 2-40: *Enabled into Short Circuit.*

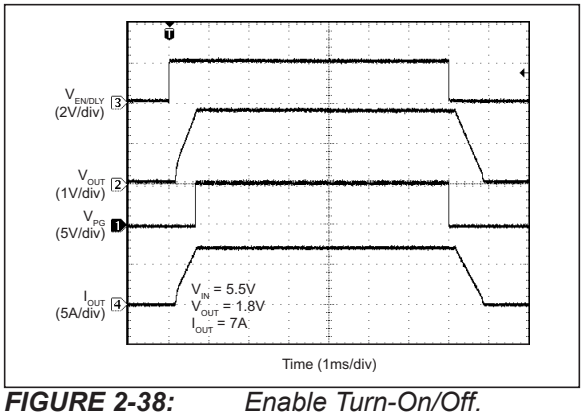

FIGURE 2-38: *Enable Turn-On/Off.*

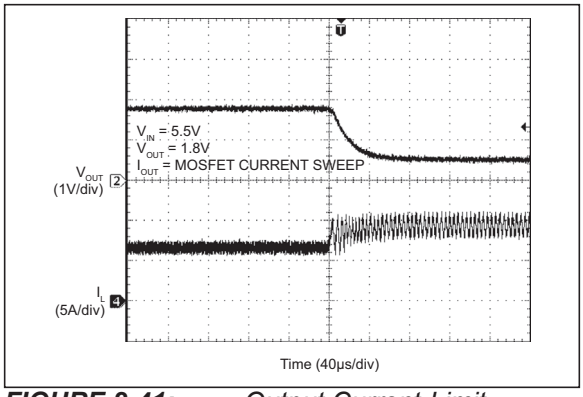

FIGURE 2-41: *Output Current-Limit Threshold.*

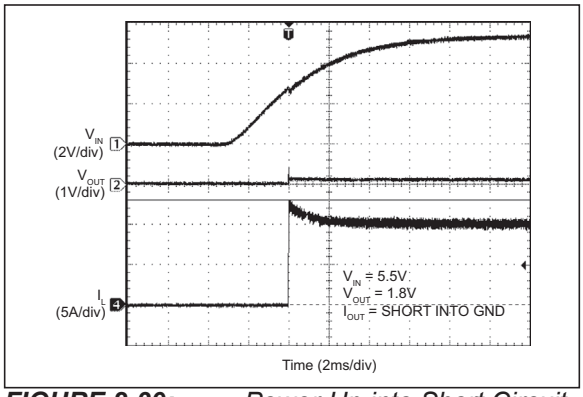

FIGURE 2-39: *Power-Up into Short Circuit.*

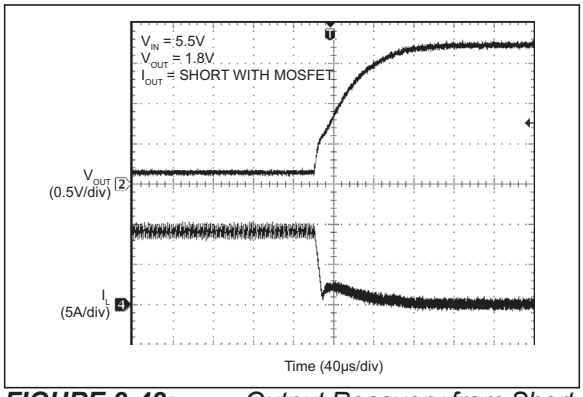

FIGURE 2-42: *Output Recovery from Short Circuit.*

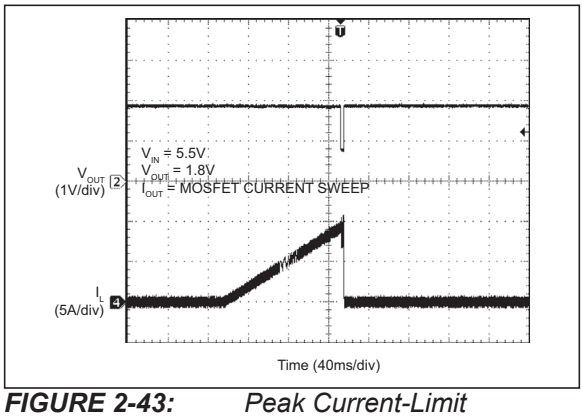

FIGURE 2-43: *Peak Current-Limit Threshold.*

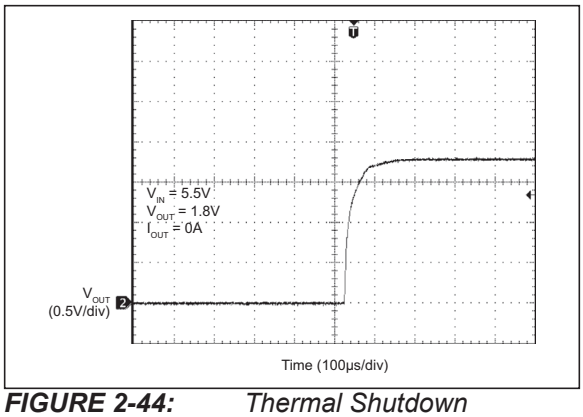

FIGURE 2-44: *Thermal Shutdown Recovery.*

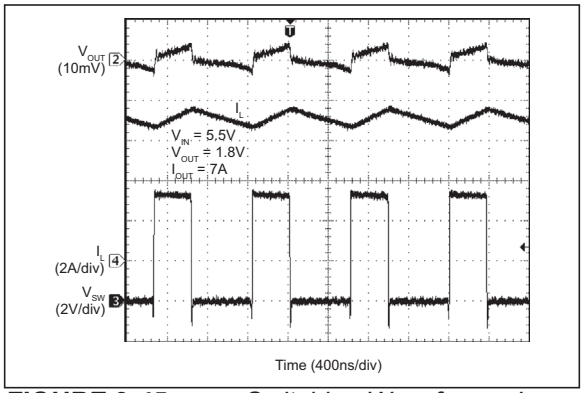

FIGURE 2-45: *Switching Waveforms, I_{OUT} = 7A.*

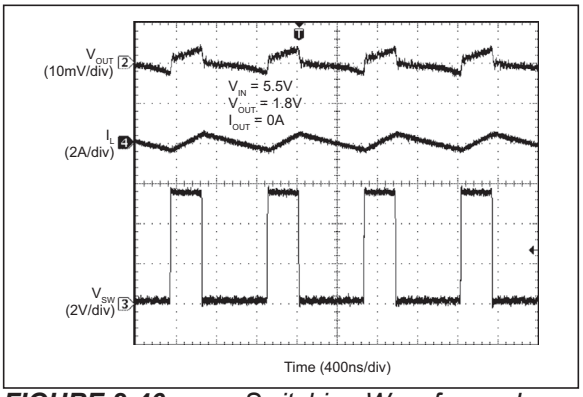

FIGURE 2-46: *Switching Waveforms, I_{OUT} = 0A.*

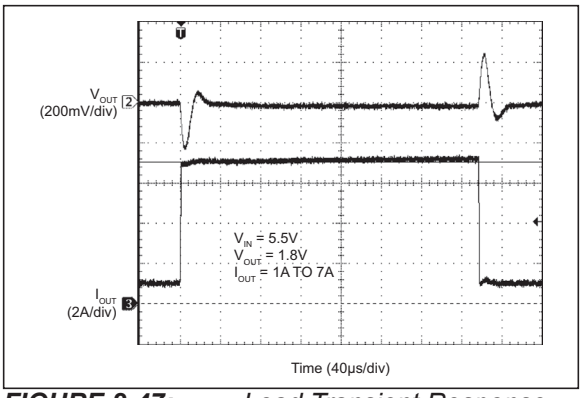

FIGURE 2-47: *Load Transient Response.*

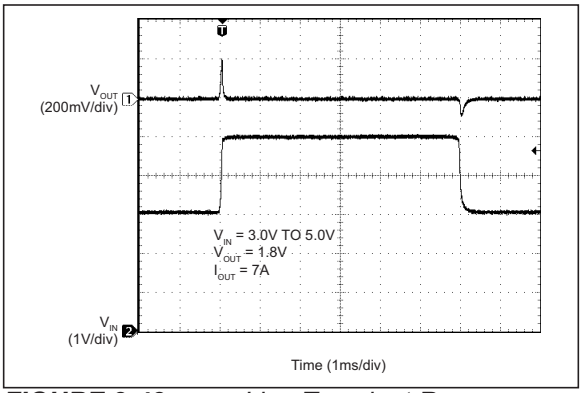

FIGURE 2-48: *Line Transient Response.*

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3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1, 6, 13, 18	PVIN	Power Supply Voltage (Input): The PVIN pins are the input supply to the internal P-Channel Power MOSFET. A 22 µF ceramic is recommended for bypassing at each PVIN pin. The SVIN pin must be connected to a PVIN pin.
2	EN/DLY	Enable/Delay (Input): This pin is internally fed with a 1 µA current source from SVIN. A delayed turn-on is implemented by adding a capacitor to this pin. The delay is proportional to the capacitor value. The internal circuits are held off until EN/DLY reaches the enable threshold of 1.24V. This pin is pulled low when the input voltage is lower than the UVLO threshold.
3	NC	No Connect: Leave this pin open. Do not connect to ground or route other signals through this pin.
4	RC	Ramp Control: A capacitor from the RC pin-to-ground determines slew rate of output voltage during start-up. The RC pin is internally fed with a 1 µA current source. The output voltage tracks the RC pin voltage. The slew rate is proportional by the internal 1 µA source and RC pin capacitor. This feature can be used for tracking capability as well as soft start.
5	PG	PG (Output): This is an open-drain output that indicates when the output voltage is below 90% of its nominal voltage. The PG flag is asserted without delay when the enable is set low or when the output goes below the 90% threshold.
14	FB	Feedback: Input to the error amplifier. The FB pin is regulated to 0.7V. A resistor divider connecting the feedback to the output is used to adjust the desired output voltage.
15	COMP	Compensation Pin (Input): The MIC22705 uses an internal compensation network containing a fixed-frequency zero (phase lead response) and pole (phase lag response) that allows the external compensation network to be much simplified for stability. The addition of a single capacitor and resistor to the COMP pin will add the necessary pole and zero for voltage mode loop stability using low-value, low-ESR ceramic capacitors.
16	SGND	Signal Ground: Internal signal ground for all low power circuits.
17	SVIN	Signal Power Supply Voltage (Input): This pin is connected externally to the PVIN pin. A 2.2 µF ceramic capacitor from the SVIN pin to SGND must be placed next to the IC.
7, 12, 19, 24	PGND	Power Ground: Internal ground connection to the source of the internal N-Channel MOSFETs.
8, 9, 10, 11, 20, 21, 22, 23	SW	Switch (Output): This is the connection to the drain of the internal P-Channel MOSFET and drain of the N-Channel MOSFET. This is a high-frequency, high-power connection; therefore traces should be kept as short and as wide as practical.
EP	GND	Exposed Pad (Power): Must make a full connection to a GND plane for full output power to be realized.

4.0 APPLICATION INFORMATION

The MIC22705 is a 7A synchronous step-down regulator IC with a fixed 1 MHz, voltage-mode PWM control scheme. The other features include tracking and sequencing control for controlling multiple output power systems, and power-on-reset (POR).

The MIC22705 is a voltage mode, pulse-width modulation (PWM) regulator. By controlling the ratio of the on-to-off time, or duty cycle, a regulated DC output voltage is achieved. As load or supply voltage changes, so does the duty cycle to maintain a constant output voltage. In cases where the input supply runs into a dropout condition, the MIC22705 will run at 100% duty cycle.

The MIC22705 provides constant switching at 1 MHz with synchronous internal MOSFETs. The internal MOSFETs include a high-side P-Channel MOSFET from the input supply to the switch pin and an N-Channel MOSFET from the switch pin-to-ground. Since the low-side N-Channel MOSFET provides the current during the off cycle, very-low amount of power is dissipated during the off period.

The PWM control provides fixed-frequency operation. By maintaining a constant switching frequency, predictable fundamental and harmonic frequencies are achieved. Other methods of regulation, such as burst and skip modes, have frequency spectrums that change with load that can interfere with sensitive communication equipment.

4.1 Input Capacitor

A 22 µF X5R or X7R dielectrics ceramic capacitor is recommended on each of the PVIN pins for bypassing. A Y5V dielectrics capacitor should not be used. Aside from losing most of their capacitance over temperature, they also become resistive at high frequencies. This reduces their ability to filter out high-frequency noise.

4.2 Output Capacitor

The MIC22705 was designed specifically for the use of ceramic output capacitors. The 100 µF output capacitor can be increased to improve transient performance. Since the MIC22705 is in voltage mode, the control loop relies on the inductor and output capacitor for compensation. For this reason, do not use excessively large output capacitors. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from the undesirable effect of their wide variation in capacitance over temperature, become resistive at high frequencies. Using Y5V or Z5U capacitors can cause instability in the MIC22705.

4.3 Inductor Selection

Inductor selection will be determined by the following (not necessarily in the order of importance):

- Inductance
- Rated current value
- Size requirements
- DC resistance (DCR)

The MIC22705 is designed to use a 0.47 µH to 4.7 µH inductor.

Maximum current ratings of the inductor are generally given in two methods: permissible DC current and saturation current. Permissible DC current can be rated either for a 40°C temperature rise or a 10% loss in inductance. Ensure the inductor selected can handle the maximum operating current. When saturation current is specified, make sure that there is enough margin that the peak current will not saturate the inductor. The ripple current can add as much as 1.2A to the output current level. The RMS rating should be chosen to be equal or greater than the current limit of the MIC22705 to prevent overheating in a fault condition. For best electrical performance, the inductor should be placed very close to the SW nodes of the IC. For this reason, the heat of the inductor is somewhat coupled to the IC (in such cases, the case temperature is not the real dissipation in the regulator), so it offers some level of protection if the inductor gets too hot. It is important to test all operating limits before settling on the final inductor choice.

The size requirements refer to the area and height requirements that are necessary to fit a particular design. Please refer to the inductor dimensions on their data sheet.

DC resistance is also important. While DCR is inversely proportional to size, DCR can represent a significant efficiency loss. Refer to the Efficiency Considerations section for a more detailed description.

4.4 Efficiency Considerations

Efficiency is defined as the amount of useful output power, divided by the amount of power consumed.

EQUATION 4-1:

$$Efficiency\ \% = \left(\frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}}\right) \times 100$$

Maintaining high efficiency serves two purposes. It decreases power dissipation in the power supply, reducing the need for heat sinks and thermal design considerations and it decreases consumption of

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current for battery powered applications. Reduced current draw from a battery increases the devices operating time, critical in hand-held devices.

There are mainly two loss terms in switching converters: static losses and switching losses. Static losses are simply the power losses due to VI or I^2R. For example, power is dissipated in the high side switch during the on cycle. Power loss is equal to the high side MOSFET $R_{DS(ON)}$ multiplied by the RMS Switch Current squared (I_{SW}^2). During the off cycle, the low side N-Channel MOSFET conducts, also dissipating power. Similarly, the inductor's DCR and capacitor's ESR also contribute to the I^2R losses. Device operating current also reduces efficiency by the product of the quiescent (operating) current and the supply voltage. The current required to drive the gates on and off at a constant 1 MHz frequency and the switching transitions make up the switching losses.

Figure 4-1 shows an efficiency curve. In the portion from 0A to 0.4A, efficiency losses are dominated by quiescent current losses, gate drive, and transition losses. In this case, lower supply voltages yield greater efficiency in that they require less current to drive the MOSFETs and have reduced input power consumption.

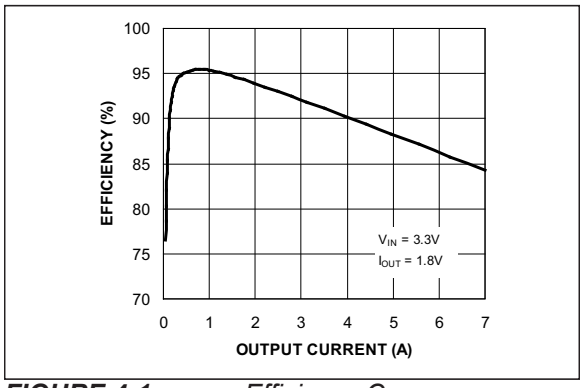

FIGURE 4-1: *Efficiency Curve.*

In the region from 1A to 7A, efficiency loss is dominated by MOSFET $R_{DS(ON)}$ and inductor DC losses. Higher input supply voltages will increase the Gate-to-Source voltage on the internal MOSFETs, reducing the internal $R_{DS(ON)}$. This improves efficiency by decreasing DC losses in the device. All but the inductor losses are inherent to the device. In which case, inductor selection becomes increasingly critical in efficiency calculations. As the inductors are reduced in size, the DC resistance (DCR) can become quite significant.

The DCR losses can be calculated as follows:

EQUATION 4-2:

$$L_{PD} = I_{OUT}^{2} \times DCR$$

From that, the loss in efficiency due to inductor resistance can be calculated as in Equation 4-3.

EQUATION 4-3:

$$EL = \left[1 - \left(\frac{V_{OUT} \times I_{OUT}}{(V_{OUT} \times I_{OUT}) + L_{PD}}\right)\right] \times 100$$

Where:
EL = Efficiency loss value in percent.

Efficiency loss due to DCR is minimal at light loads and gains significance as the load is increased. Inductor selection becomes a trade-off between efficiency and size in this case.

Alternatively, under lighter loads, the ripple current due to the inductance becomes a significant factor. When light load efficiencies become more critical, a larger inductor value maybe desired. Larger inductances reduce the peak-to-peak inductor ripple current, which minimizes losses.

4.5 Compensation

The MIC22705 has a combination of internal and external stability compensation to simplify the circuit for small, high-efficiency designs. In such designs, voltage mode conversion is often the optimum solution. Voltage mode is achieved by creating an internal 1 MHz ramp signal and using the output of the error amplifier to modulate the pulse width of the switch node, thereby maintaining output voltage regulation. With a typical gain bandwidth of 100 kHz to 200 kHz, the MIC22705 is capable of extremely fast transient responses.

The MIC22705 is designed to be stable with a typical application using a 1 µH inductor and a 100 µF ceramic (X5R) output capacitor. These values can be varied dependent upon the trade-off between size, cost and efficiency, keeping the LC natural frequency ideally less than 26 kHz to stability can be achieved. The minimum recommended inductor value is 0.47 µH and minimum recommended output capacitor value is 22 µF. The trade-off between changing these values is that with a larger inductor, there is a reduced peak-to-peak current that yields a greater efficiency at

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lighter loads. A larger output capacitor will improve transient response by providing a larger hold up reservoir of energy to the output.

The integration of one pole-zero pair within the control loop greatly simplifies compensation. The optimum values for C_{COMP} (in series with a 20 kΩ resistor) are shown in Table 4-1.

TABLE 4-1: COMPENSATION CAPACITOR SELECTION

L	C		
	22 µF - 47 µF	**47 µF - 100 µF**	**100 µF - 470 µF**
0.47 µH	0 pF - 10 pF (Note 1)	22 pF	33 pF
1 µH	0 pF - 15 pF (Note 2)	15 pF - 22 pF	33 pF
2.2 µH	15 pF - 33 pF	33 pF - 47 pF	100 pF - 220 pF

Note 1: V_{OUT} > 1.2V
2: V_{OUT} > 1V

4.6 Feedback

The MIC22705 provides a feedback pin to adjust the output voltage to the desired level. This pin connects internally to an error amplifier. The error amplifier then compares the voltage at the feedback to the internal 0.7V reference voltage and adjusts the output voltage to maintain regulation. The resistor divider network for a desired V_{OUT} is given by:

EQUATION 4-4:

$$R2 = \frac{R1}{\left(\frac{V_{OUT}}{V_{REF}} - 1\right)}$$

Where:
V_{REF} = 0.7V
V_{OUT} = The desired output voltage.

A 10 kΩ or lower resistor value from the output to the feedback (R1) is recommended since large feedback resistor values increase the impedance at the feedback pin, making the feedback node more susceptible to noise pick-up. A small capacitor (50 pF to 100 pF) across the lower resistor can reduce noise pick-up by providing a low impedance path to ground.

4.7 Enable/Delay (EN/DLY) Pin

Enable/Delay (EN/DLY) sources 1 µA out of the IC to allow a startup delay to be implemented. The delay time is simply the time it takes 1 µA to charge $C_{EN/DLY}$ to 1.24V. Therefore:

EQUATION 4-5:

$$t_{EN/\mathrm{DLY}} = \frac{1.24 \times C_{EN/\mathrm{DLY}}}{1 \times 10^{-6}}$$

4.8 RC Pin (Soft-Start)

The RC pin provides a trimmed 1 µA current source/sink similar to the DELAY pin for accurate ramp-up (soft-start) and ramp-down control. This allows the MIC22705 to be used in systems that require voltage tracking or ratio-metric voltage tracking at startup.

There are two ways of using the RC pin:

- Externally driven from a voltage source
- Externally attached capacitor sets output ramp up/down rate

In the first case, driving RC with a voltage from 0V to V_{REF} programs the output voltage between 0% and 100% of the nominal set voltage.

In the second case, the external capacitor sets the ramp up and ramp down time of the output voltage. The time is given by:

EQUATION 4-6:

$$t_{RAMP} = \frac{0.7 \times C_{RC}}{1.10^{-6}}$$

Where:
t_{RAMP} = The time from 0% to 100% nominal output voltage.

4.8.1 PRE-BIAS START-UP

The MIC22705 is designed to start up into a pre-biased output. This prevents large negative inductor currents and excessive output voltage oscillations. The MIC22705 starts with the low-side MOSFET turned off, preventing reverse inductor current flow. The synchronous MOSFET stays off until the end of the start-up sequence.

If the load current demand is zero or very small at the time the synchronous MOSFET is enabled, the inductor current could be discontinuous. In this case, when the synchronous MOSFET is enabled, the regulator will transition abruptly from DCM to CCM. This may cause some small reverse current. If load is applied to keep the inductor current in CCM, then the transition will be seamless. A pre-bias condition can occur if the input is turned off then immediately turned back on before the output capacitor is discharged to ground. It is also possible that the output of the MIC22705 could be pulled up or pre-biased through

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parasitic conduction paths from one supply rail to another in multiple voltage (V_{OUT}) level ICs such as a FPGA.

Figure 4-2 shows a normal start-up waveform. A 1 µA current source charges the soft-start capacitor C_{RC}. The C_{RC} capacitor forces the V_{RC} voltage to come up slowly (V_{RC} trace), thereby providing a soft-start ramp. This ramp is used to control the internal reference (V_{REF}). The error amplifier forces the output voltage to follow the V_{REF} ramp from zero to the final value.

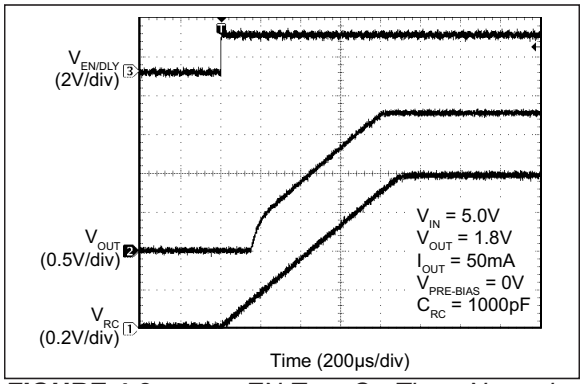

FIGURE 4-2: *EN Turn-On Time: Normal Start Up.*

If the output is pre-biased to a voltage above the expected value, as shown in Figure 4-3, then neither MOSFET will turn on until the ramp control voltage (V_{RC}) is above the reference voltage (V_{REF}). Then, the high-side MOSFET starts switching, forcing the output to follow the VRC ramp. Once the soft-start has completed, the low-side MOSFET will begin switching.

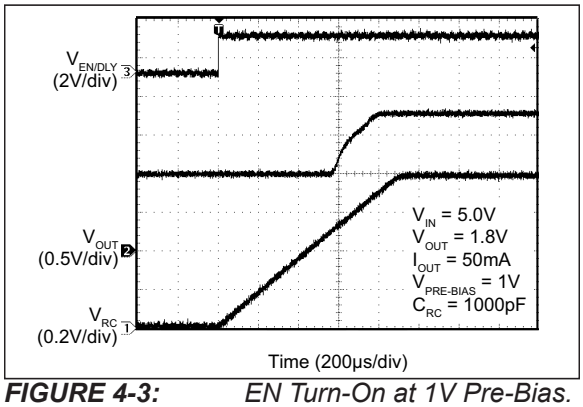

FIGURE 4-3: *EN Turn-On at 1V Pre-Bias.*

When the MIC22705 is turned off, the low-side MOSFET will be disabled and the output voltage will decay to zero. During this time, the ramp control voltage (V_{RC}) will still control the output voltage fall-time with the high-side MOSFET if the output voltage falls faster than the V_{RC} voltage. Figure 4-4 shows this operating condition. Here a 7A load pulls the output down fast enough to force the high-side MOSFET on (V_{SW} trace).

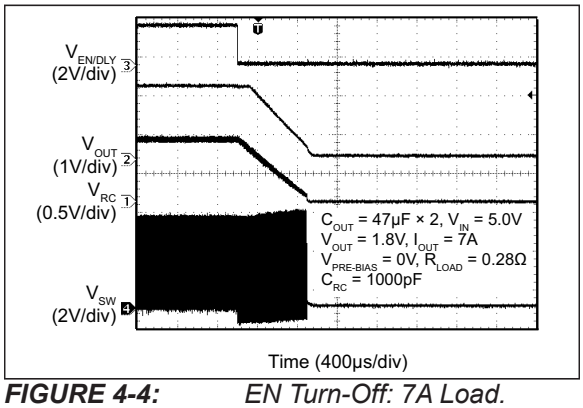

FIGURE 4-4: *EN Turn-Off: 7A Load.*

If the output voltage falls slower than the V_{RC} voltage, then the both MOSFETs will be off and the output will decay to zero as shown in the V_{OUT} trace in Figure 4-5. With both MOSFETs off, any resistive load connected to the output will help pull down the output voltage. This will occur at a rate determined by the resistance of the load and the output capacitance.

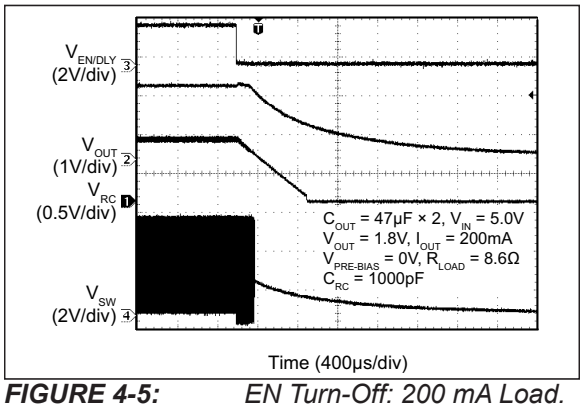

FIGURE 4-5: *EN Turn-Off: 200 mA Load.*

4.9 Current Limit

The MIC22705 is protected against overload in two stages. The first is to limit the current in the P-channel switch; the second is overtemperature shutdown.

Current is limited by measuring the current through the high-side MOSFET during its power stroke and immediately switching off the driver when the preset limit is exceeded.

The circuit in Figure 4-6 describes the operation of the current limit circuit. Because the actual $R_{DS(ON)}$ of the P-channel MOSFET varies part-to-part, over temperature and with input voltage, simple IR voltage detection is not employed. Instead, a smaller copy of the Power MOSFET (Reference FET) is fed with a constant current that is directly proportional to the factory set current limit. This sets the current limit as a current ratio and thus, is not dependent upon the $R_{DS(ON)}$ value. Current limit is set to nominal value.

Variations in the scale factor K between the power PFET and the reference PFET used to generate the limit threshold account for a relatively small inaccuracy.

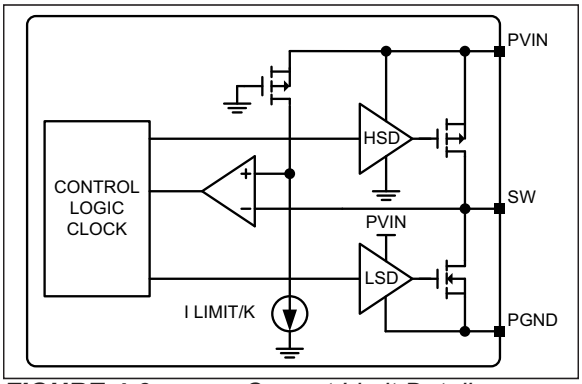

FIGURE 4-6: *Current Limit Detail.*

4.10 Thermal Considerations

The MIC22705 is packaged in a 4 mm x 4 mm QFN. It's a package that has excellent thermal-performance, equaling that of the larger TSSOP packages. This maximizes heat transfer from the junction to the exposed pad (ePAD) that connects to the ground plane. The size of the ground plane attached to the exposed pad determines the overall thermal resistance from the junction to the ambient air surrounding the printed circuit board. The junction temperature for a given ambient temperature can be calculated using:

EQUATION 4-7:

$$T_J = T_A + P_{DISS} \times R\theta_{JA}$$

Where:

PDISS = The power dissipated within the QFN package and is at 7A load.

$R\theta_{JA}$ = A combination of junction-to-case thermal resistance ($R\theta_{JC}$) and Case-to-Ambient thermal resistance ($R\theta_{CA}$), since thermal resistance of the solder connection from the ePAD to the PCB is negligible; $R\theta_{CA}$ is the thermal resistance of the ground plane-to-ambient, so $R\theta_{JA} = R\theta_{JC} + R\theta_{CA}$.

T_A = The operating ambient temperature.

Example:

The evaluation board has two copper planes contributing to an $R\theta_{JA}$ of approximately 25°C/W. The worst case $R\theta_{JC}$ of the QFN 4 mm x 4 mm is 14°C/W.

EQUATION 4-8:

$$R\theta_{JA} = 14 + 25 = 39°C/\text{W}$$

To calculate the junction temperature for a 50°C ambient:

EQUATION 4-9:

$$T_J = T_A + P_{DISS} \times R\theta_{JA}$$

$$T_J = 50 + (1.8 \times 39)$$

$$T_J = 120°C$$

4.11 Thermal Measurements

Measuring the IC's case temperature is recommended to ensure it is within its operating limits. Although this might seem like a very elementary task, it is easy to get erroneous results. The most common mistake is to use the standard thermal couple that comes with a thermal meter. This thermal couple wire gauge is large, typically 22 gauge, and behaves like a heatsink, resulting in a lower case measurement.

Two methods of temperature measurement are using a smaller thermal couple wire or an infrared thermometer. If a thermal couple wire is used, it must be constructed of 36 gauge wire or higher then (smaller wire size) to minimize the wire heat-sinking effect. In addition, the thermal couple tip must be covered in either thermal grease or thermal glue to make sure that the thermal couple junction is making good contact with the case of the IC. Omega brand thermal couple (5SC-TT-K-36-36) is adequate for most applications.

Whenever possible, an infrared thermometer is recommended. The measurement spot size of most infrared thermometers is too large for an accurate reading on a small form factor ICs. However, a IR thermometer from Optris has a 1 mm spot size, which makes it a good choice for measuring the hottest point on the case. An optional stand makes it easy to hold the beam on the IC for long periods of time.

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4.12 Sequencing and Tracking Examples

There are four distinct variations that are easily implemented using the MIC22705. The two sequencing variations are Delayed and Windowed. The two tracking variants are Normal and Ratio Metric. The following diagrams illustrate methods for connecting two MIC22705's to achieve these requirements.

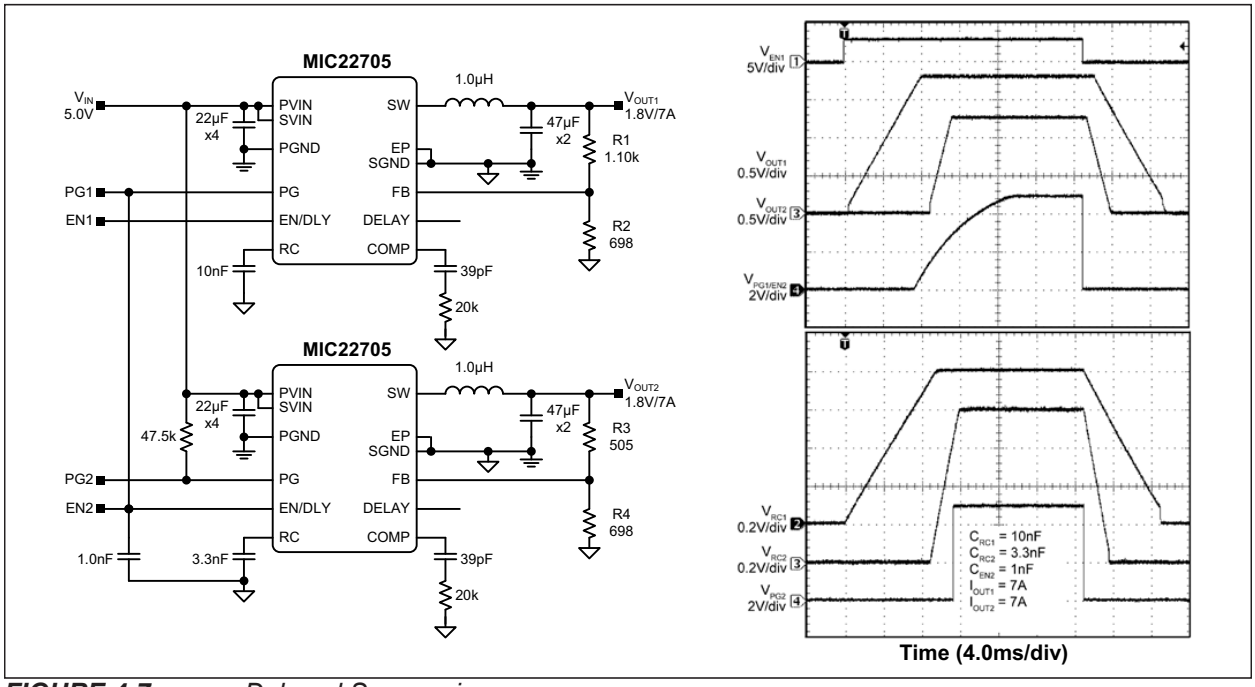

FIGURE 4-7: *Delayed Sequencing.*

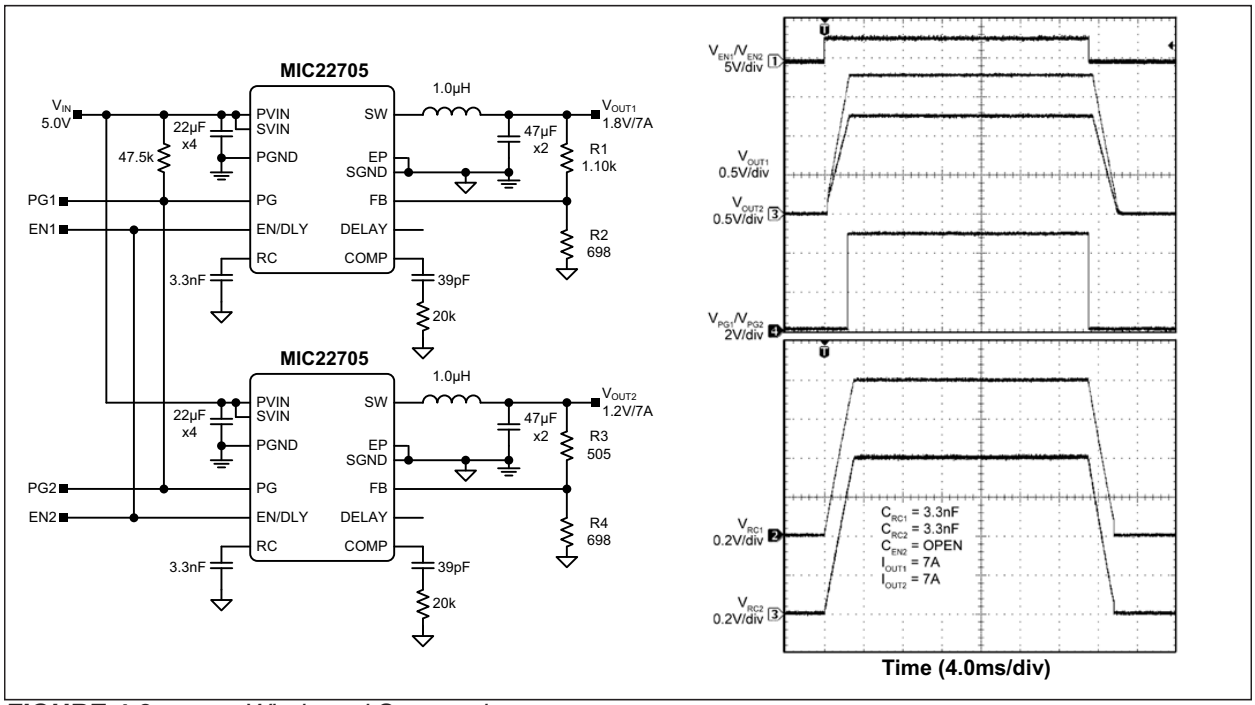

FIGURE 4-8: *Windowed Sequencing.*

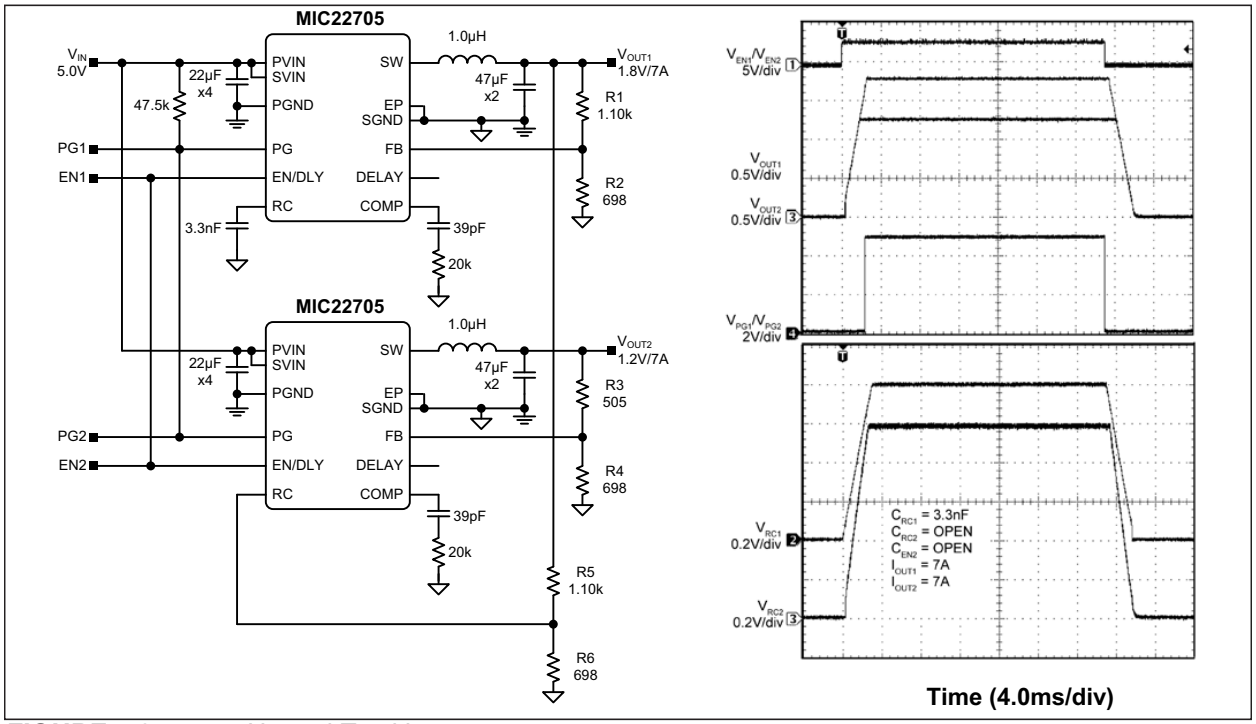

FIGURE 4-9: *Normal Tracking.*

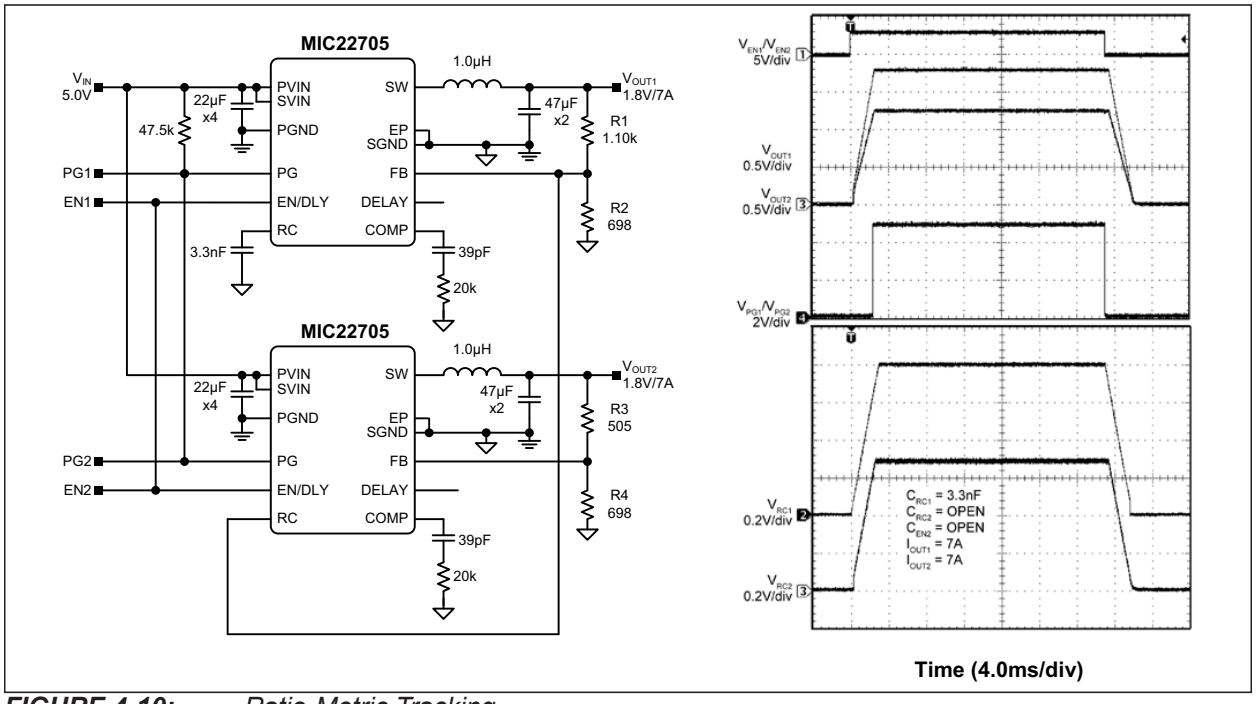

FIGURE 4-10: *Ratio-Metric Tracking.*

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5.0 PCB LAYOUT GUIDELINES

PCB layout is critical to achieve reliable, stable and efficient performance. A ground plane is required to control EMI and minimize the inductance in power, signal and return paths.

The following guidelines should be followed to ensure proper operation of the MIC22705 converter.

5.1 IC

- The 2.2 µF ceramic capacitor, which is connected to the SVIN pin, must be located right at the IC. The SVIN pin is very noise sensitive and placement of the capacitor is very critical. Use wide traces to connect to the SVIN and SGND pins.
- The signal ground pin (SGND) must be connected directly to the ground planes. Do not route the SGND pin to the PGND Pad on the top layer.
- Place the IC close to the point of load (POL).
- Use fat traces to route the input and output power lines.
- Signal and power grounds should be kept separate and connected at only one location.

5.2 Input Capacitor

- A 22 µF X5R or X7R dielectrics ceramic capacitor is recommended on each of the PVIN pins for bypassing.
- Place the input capacitors on the same side of the board and as close to the IC as possible.
- Keep both the PVIN pin and PGND connections short.
- Place several vias to the ground plane close to the input capacitor ground terminal.
- Use either X7R or X5R dielectric input capacitors. Do not use Y5V or Z5U type capacitors.
- Do not replace the ceramic input capacitor with any other type of capacitor. Any type of capacitor can be placed in parallel with the input capacitor.
- If a Tantalum input capacitor is placed in parallel with the input capacitor, it must be recommended for switching regulator applications and the operating voltage must be derated by 50%.
- In “Hot-Plug” applications, a Tantalum or Electrolytic bypass capacitor must be used to limit the overvoltage spike seen on the input supply with power is suddenly applied.

5.3 Inductor

- Keep the inductor connection to the switch node (SW) short.
- Do not route any digital lines underneath or close to the inductor.
- Keep the switch node (SW) away from the feedback (FB) pin.
- To minimize noise, place a ground plane underneath the inductor.
- The inductor can be placed on the opposite side of the PCB with respect to the IC. It does not matter whether the IC or inductor is on the top or bottom as long as there is enough air flow to keep the power components within their temperature limits. The input and output capacitors must be placed on the same side of the board as the IC.

5.4 Output Capacitor

- Use a wide trace to connect the output capacitor ground terminal to the input capacitor ground terminal.
- Phase margin will change as the output capacitor value and ESR changes. Contact the factory if the output capacitor is different from what is shown in the BOM.
- The feedback divider network must be place close to the IC with the bottom of R2 connected to SGND.
- The feedback trace should be separate from the power trace and connected as close as possible to the output capacitor. Sensing a long high-current load trace can degrade the DC load regulation.

5.5 RC Snubber

- Place the RC snubber on either side of the board and as close to the SW pin as possible.

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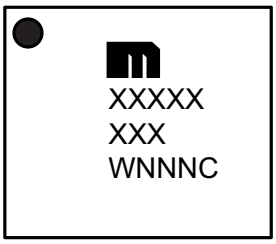
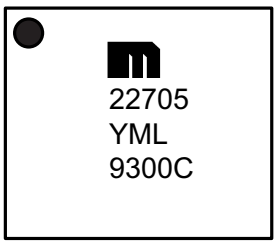
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

24-Lead QFN*



Example



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

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24-Lead QFN 4 mm x 4 mm Package Outline and Recommended Land Pattern

TITLE
24 LEAD QFN 4x4mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

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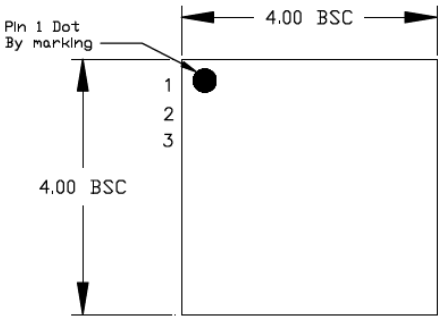
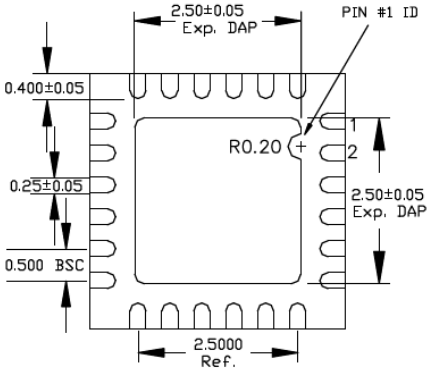
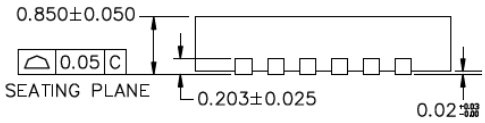


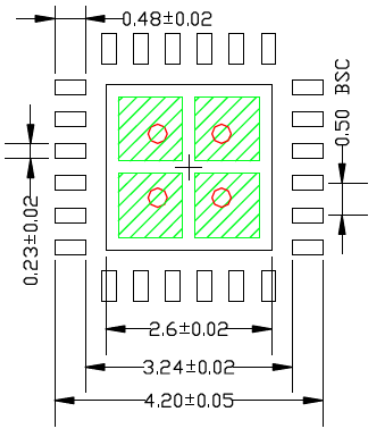
TOP VIEW
NOTE: 1, 2, 3



BOTTOM VIEW
NOTE: 1, 2, 3



SIDE VIEW
NOTE: 1, 2, 3



RECOMMENDED LAND PATTERN
NOTE: 4, 5

NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA. SIZE SHOULD BE 0.30-0.35M IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE
5. GREEN RECTANGLES (SHADED AREA) Indicate SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 1.00x1.00 MM IN SIZE, 1.20 MM PITCH.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

NOTES:

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APPENDIX A: REVISION HISTORY

Revision A (February 2020)

- Converted Micrel document MIC22705 to Microchip data sheet template DS20006307A.
- Minor grammatical text changes throughout.
- Evaluation Board Schematic, BOM, and PCB Layout sections from original data sheet moved to the part's Evaluation Board User's Guide.

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Device	X	XX	-XX
Part No.	Junction Temp. Range	Package	Media Type

Device:	MIC22705:	1 MHz, 7A Integrated Switch High Efficiency Synchronous Buck Regulator	
Junction Temperature Range:	Y	=	–40°C to +125°C, RoHS-Compliant
Package:	ML	=	24-Lead 4 mm x 4 mm QFN
Media Type:	TR	=	5,000/Reel

Examples:

a) MIC22705YML-TR: MIC22705, Adj. Output Voltage, –40°C to +125°C Temperature Range, 24-Lead QFN, 5,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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