

## General Description

The MIC4103 and MIC4104 are high frequency, 100V Half Bridge MOSFET drivers with faster turn-off characteristics than the MIC4100 and MIC4101 drivers. They feature fast 24ns propagation delay times and 6ns driver fall times. The low-side and high-side gate drivers are independently controlled and matched to within 3ns typical. The MIC4103 has CMOS input thresholds and the MIC4104 has TTL input thresholds. The MIC4103/4 include a high voltage internal diode that charges the high-side gate drive bootstrap capacitor.

A robust, high-speed, and low power level shifter provides clean level transitions to the high side output. The robust operation of the MIC4103/4 ensures the outputs are not affected by supply glitches, HS ringing below ground, or HS slewing with high speed voltage transitions. Under-voltage protection is provided on both the low-side and high-side drivers.

The MIC4103 and MIC4104 are available in an 8-pin SOIC and 8-pin 3mm × 3mm MLF<sup>®</sup> package with a operating junction temperature range of -40°C to +125°C.

Data sheets and support documentation can be found on Micrel's web site at: [www.micrel.com](http://www.micrel.com).

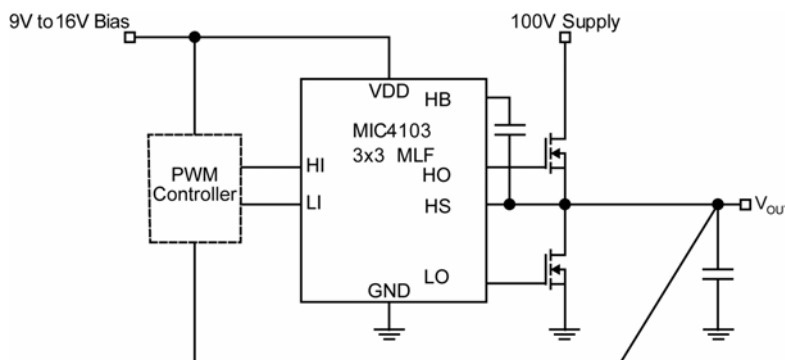
## Features

- Asymmetrical, low impedance outputs drive 1000pF load with 10ns rise times and 6ns fall times
- Bootstrap supply max voltage to 118V DC
- Supply voltage up to 16V
- Drives high- and low-side N-Channel MOSFETs with independent inputs
- CMOS input thresholds (MIC4103)
- TTL input thresholds (MIC4104)
- On-chip bootstrap diode
- Fast 24ns propagation times
- Low power consumption
- Supply under-voltage protection
- Typical 2.5Ω pull up and 1.25Ω pull down output driver resistance
- -40°C to +125°C junction temperature range

## Applications

- High voltage buck converters
- Full- and half-bridge power topologies
- Active clamp forward converter
- Two switch forward topologies
- Interface to digital controllers

## Typical Application

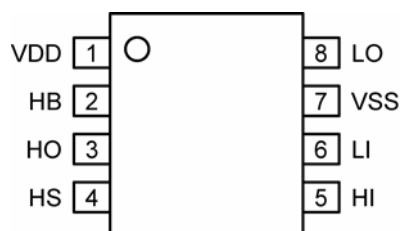


**100V Buck Regulator Solution**

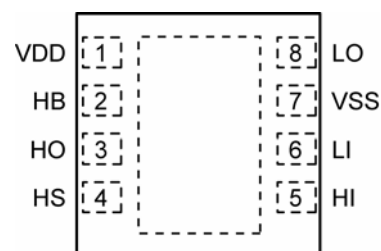
## Ordering Information

Part Number	Input	Junction Temp. Range	Package
MIC4103YM	CMOS	-40° to +125°C	8-Pin SOIC
MIC4104YM	TTL	-40° to +125°C	8-Pin SOIC
MIC4103YML (coming soon)	CMOS	-40° to +125°C	8-Pin 3x3 MLF <sup>®</sup>
MIC4104YML (coming soon)	TTL	-40° to +125°C	8-Pin 3x3 MLF <sup>®</sup>

## Pin Configuration



8-Pin SOIC (M)



8-Pin 3mm x 3mm MLF<sup>®</sup> (ML)

## Pin Description

Pin Number	Pin Name	Pin Function
1	VDD	Positive Supply to lower gate drivers. Decouple this pin to VSS (Pin 7). Bootstrap diode connected to HB (pin 2).
2	HB	High-Side Bootstrap supply. External bootstrap capacitor is required. Connect positive side of bootstrap capacitor to this pin. Bootstrap diode is on-chip.
3	HO	High-Side Output. Connect to gate of High-Side power MOSFET.
4	HS	High-Side Source connection. Connect to source of High-Side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
5	HI	High-Side input.
6	LI	Low-Side input.
7	VSS	Chip negative supply, generally will be ground.
8	LO	Low-Side Output. Connect to gate of Low-Side power MOSFET.

### Absolute Maximum Ratings<sup>(1)</sup>

Supply Voltage ( $V_{DD}, V_{HB} - V_{HS}$ )	-0.3V to 18V
Input Voltages ( $V_{LI}, V_{HI}$ )	-0.3V to $V_{DD} + 0.3V$
Voltage on LO ( $V_{LO}$ )	-0.3V to $V_{DD} + 0.3V$
Voltage on HO ( $V_{HO}$ )	$V_{HS} - 0.3V$ to $V_{HB} + 0.3V$
Voltage on HS (continuous)	-1V to 110V
Voltage on HB	118V
Average Current in VDD to HB Diode	100mA
Junction Temperature ( $T_J$ )	-55°C to +150°C
Storage Temperature ( $T_s$ )	-60°C to +150°C
ESD Rating	See note 3

### Operating Ratings<sup>(2)</sup>

Supply Voltage ( $V_{DD}$ )	+9V to +16V
Voltage on HS	-1V to 100V
Voltage on HS (repetitive transient)	-5V to 105V
HS Slew Rate	50V/ns
Voltage on HB	$V_{HS} + 8V$ to $V_{HS} + 16V$ and $V_{DD} - 1V$ to $V_{DD} + 100V$
Junction Temperature ( $T_J$ )	-40°C to +125°C
Junction Thermal Resistance	
SOIC-8L ( $\theta_{JA}$ )	140°C/W
3mm × 3mm MLF <sup>®</sup>	tdb°C/W

### Electrical Characteristics<sup>(4)</sup>

$V_{DD} = V_{HB} = 12V$ ;  $V_{SS} = V_{HS} = 0V$ ; No load on LO or HO;  $T_A = 25^\circ C$ ; unless noted. **Bold** values indicate  $-40^\circ C \leq T_J \leq +125^\circ C$ .

Symbol	Parameter	Condition	Min	Typ	Max	Units
<b>Supply Current</b>						
$I_{DD}$	$V_{DD}$ Quiescent Current	LI = HI = 0V		40	150 <b>200</b>	$\mu A$
$I_{DDO}$	$V_{DD}$ Operating Current	f = 500kHz		3.0	<b>4.0</b>	mA
$I_{HB}$	Total HB Quiescent Current	LI = HI = 0V		25	150 <b>200</b>	$\mu A$
$I_{HBO}$	Total HB Operating Current	f = 500kHz		1.5	2.5 <b>3</b>	mA
$I_{HBS}$	HB to $V_{SS}$ Current, Quiescent	$V_{HS} = V_{HB} = 110V$		0.05	1 <b>30</b>	$\mu A$
<b>Input Pins: MIC4103 (CMOS Input )</b>						
$V_{IL}$	Low Level Input Voltage Threshold		<b>4</b> <b>3</b>	5.3		V
$V_{IH}$	High Level Input Voltage Threshold			5.7	7 <b>8</b>	V
$V_{IHYS}$	Input Voltage Hysteresis			0.4		V
$R_i$	Input Pulldown Resistance		<b>100</b>	200	<b>500</b>	k $\Omega$
<b>Input Pins: MIC4104 (TTL Input )</b>						
$V_{IL}$	Low Level Input Voltage Threshold		<b>0.8</b>	1.5		V
$V_{IH}$	High Level Input Voltage Threshold			1.5	<b>2.2</b>	V
$R_i$	Input Pulldown Resistance		<b>100</b>	200	<b>500</b>	k $\Omega$
<b>Under Voltage Protection</b>						
$V_{DDR}$	$V_{DD}$ Rising Threshold		<b>6.5</b>	7.4	<b>8.0</b>	V
$V_{DDH}$	$V_{DD}$ Threshold Hysteresis			0.5		V
$V_{HBR}$	HB Rising Threshold		<b>6.0</b>	7.0	<b>8.0</b>	V
$V_{HBH}$	HB Threshold Hysteresis			0.4		V

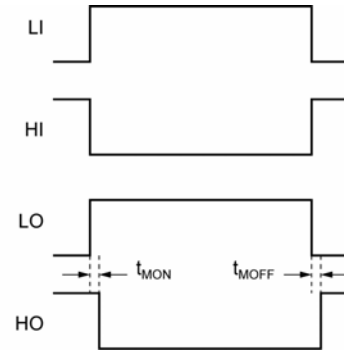
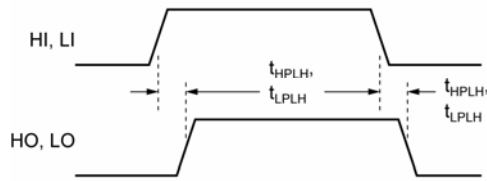
Symbol	Parameter	Condition	Min	Typ	Max	Units
<b>Bootstrap Diode</b>						
V <sub>DL</sub>	Low-Current Forward Voltage	I <sub>VDD-HB</sub> = 100μA		0.4	0.55 <b>0.70</b>	V
V <sub>DH</sub>	High-Current Forward Voltage	I <sub>VDD-HB</sub> = 100mA		0.7	0.8 <b>1.0</b>	V
R <sub>D</sub>	Dynamic Resistance	I <sub>VDD-HB</sub> = 100mA		1.0	1.5 <b>2.0</b>	Ω
<b>LO Gate Driver</b>						
V <sub>OLL</sub>	Low Level Output Voltage	I <sub>LO</sub> = 160mA		0.18	0.3 <b>0.4</b>	V
V <sub>OHL</sub>	High Level Output Voltage	I <sub>LO</sub> = -100mA, V <sub>OHL</sub> = V <sub>DD</sub> - V <sub>LO</sub>		0.25	0.3 <b>0.45</b>	V
I <sub>OHL</sub>	Peak Sink Current	V <sub>LO</sub> = 0V		3		A
I <sub>OLL</sub>	Peak Source Current	V <sub>LO</sub> = 12V		2		A
<b>HO Gate Driver</b>						
V <sub>OLH</sub>	Low Level Output Voltage	I <sub>HO</sub> = 160mA		0.22	0.3 <b>0.4</b>	V
V <sub>OHH</sub>	High Level Output Voltage	I <sub>HO</sub> = -100mA, V <sub>OHH</sub> = V <sub>HB</sub> - V <sub>HO</sub>		0.25	0.3 <b>0.45</b>	V
I <sub>OHH</sub>	Peak Sink Current	V <sub>HO</sub> = 0V		3		A
I <sub>OLH</sub>	Peak Source Current	V <sub>HO</sub> = 12V		2		A
<b>Switching Specifications</b>						
t <sub>LPHL</sub>	Lower Turn-Off Propagation Delay (LI Falling to LO Falling)	(MIC4103)		24	<b>45</b>	ns
t <sub>HPHL</sub>	Upper Turn-Off Propagation Delay (HI Falling to HO Falling)	(MIC4103)		24	<b>45</b>	ns
t <sub>LPLH</sub>	Lower Turn-On Propagation Delay (LI Rising to LO Rising)	(MIC4103)		24	<b>45</b>	ns
t <sub>HPLH</sub>	Upper Turn-On Propagation Delay (HI Rising to HO Rising)	(MIC4103)		24	<b>45</b>	ns
t <sub>LPHL</sub>	Lower Turn-Off Propagation Delay (LI Falling to LO Falling)	(MIC4104)		24	<b>45</b>	ns
t <sub>HPHL</sub>	Upper Turn-Off Propagation Delay (HI Falling to HO Falling)	(MIC4104)		24	<b>45</b>	ns
t <sub>LPLH</sub>	Lower Turn-On Propagation Delay (LI Rising to LO Rising)	(MIC4104)		24	<b>45</b>	ns
t <sub>HPLH</sub>	Upper Turn-On Propagation Delay (HI Rising to HO Rising)	(MIC4104)		24	<b>45</b>	ns
t <sub>MON</sub>	Delay Matching: Lower Turn-On and Upper Turn-Off			3	8 <b>10</b>	ns
t <sub>MOFF</sub>	Delay Matching: Lower Turn-Off and Upper Turn-On			3	8 <b>10</b>	ns
t <sub>RC</sub>	Output Rise Time	C <sub>L</sub> = 1000pF		10		ns
t <sub>FC</sub>	Output Fall Time	C <sub>L</sub> = 1000pF		6		ns

Symbol	Parameter	Condition	Min	Typ	Max	Units
<b>Switching Specifications (cont.)</b>						
$t_R$	Output Rise Time (3V to 9V)	$C_L = 0.1\mu\text{F}$		0.4	0.6 <b>0.8</b>	$\mu\text{s}$
$t_F$	Output Fall Time (3V to 9V)	$C_L = 0.1\mu\text{F}$		0.2	0.3 <b>0.4</b>	$\mu\text{s}$
$t_{PW}$	Minimum Input Pulse Width that Changes the Output	<b>Note 6</b>			<b>50</b>	ns
$t_{BS}$	Bootstrap Diode Turn-On or Turn-Off Time			10		ns

**Notes:**

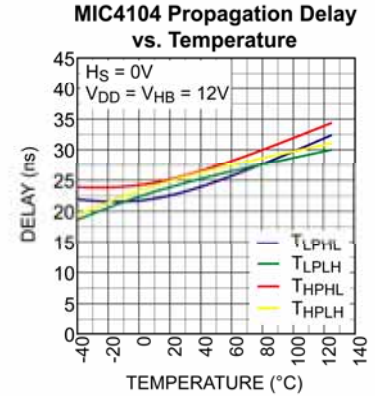
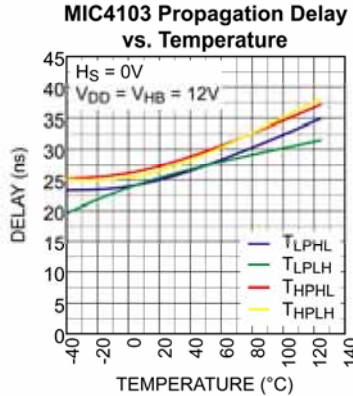
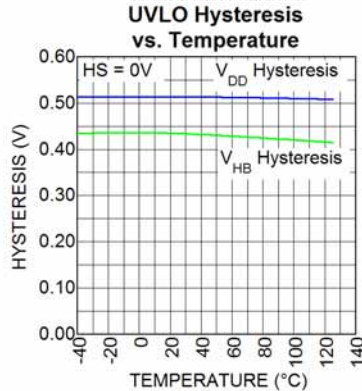
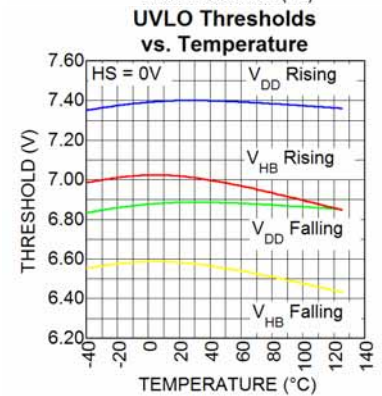
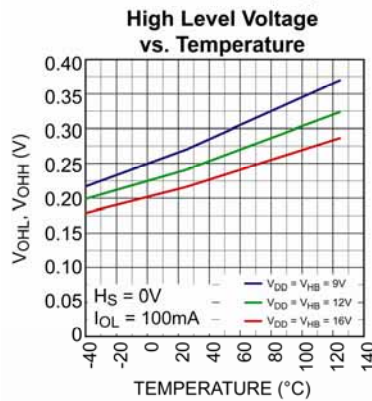
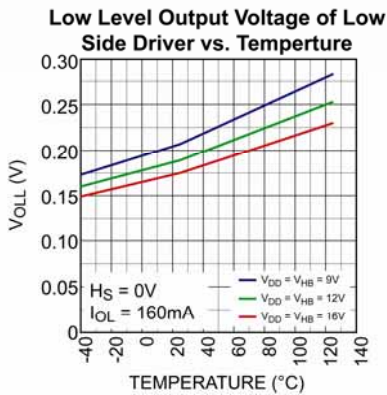
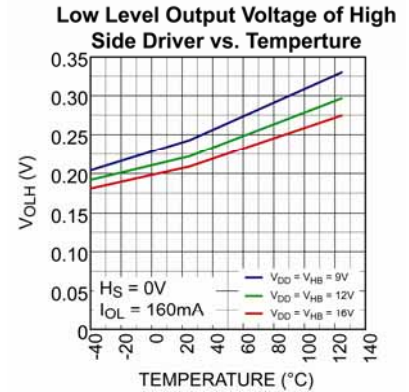
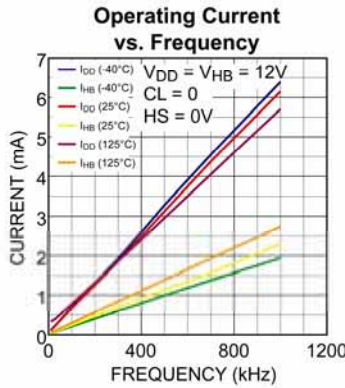
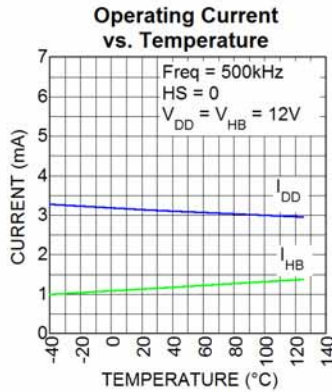
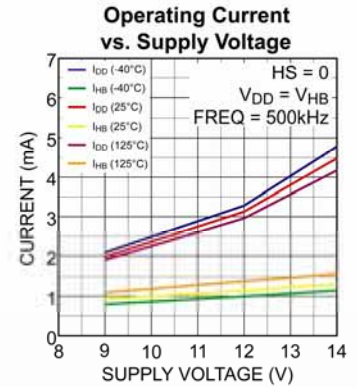
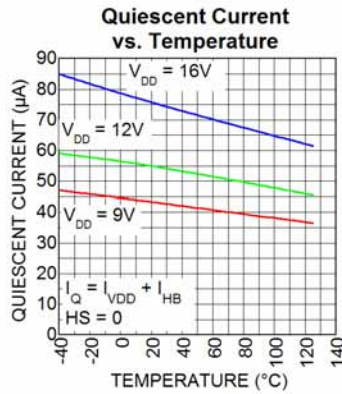
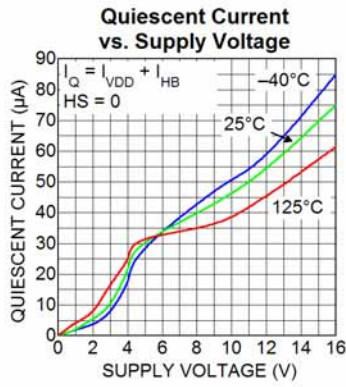
1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5k $\Omega$  in series with 100pF.
4. Specification for packaged product only.
5. All voltages relative to pin 7,  $V_{SS}$  unless otherwise specified
6. Guaranteed by design. Not production tested.

# Timing Diagrams



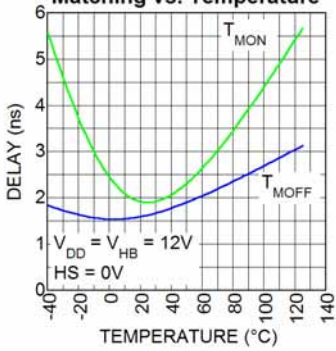
**Note:** All propagation delays are measured from the 50% voltage level.

# Typical Characteristics

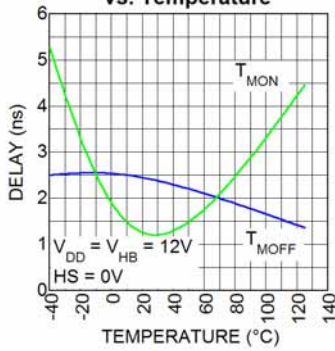


# Typical Characteristics

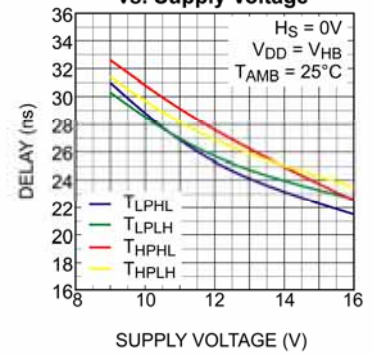
**MIC4103 Propagation Delay Matching vs. Temperature**



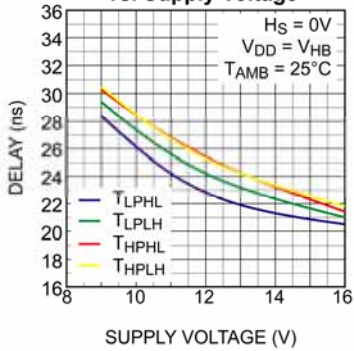
**MIC4104 Propagation Delay vs. Temperature**



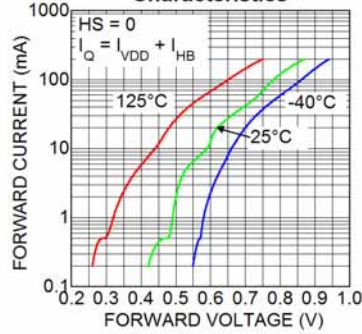
**MIC4103 Propagation Delay vs. Supply Voltage**



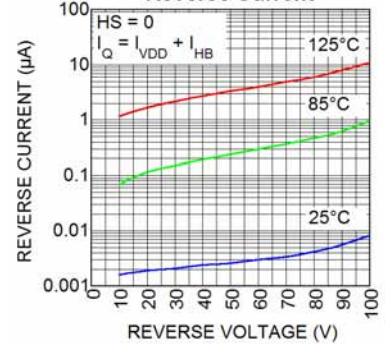
**MIC4104 Propagation Delay vs. Supply Voltage**



**Bootstrap Diode I-V Characteristics**



**Bootstrap Diode Reverse Current**





## Functional Characteristics

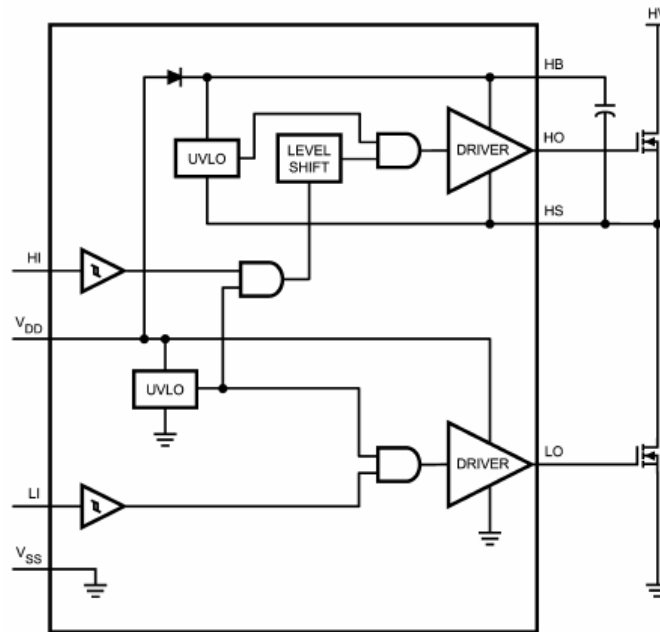


Figure 1. MIC4103/4 Functional Block Diagram

## Functional Description

The MIC4103 is a high voltage, non-inverting, dual MOSFET driver that is designed to independently drive both high-side and low-side N-Channel MOSFETs. The block diagram of the MIC4103 is shown in Figure 1.

Both drivers contain an input buffer with hysteresis, a UVLO circuit and an output buffer. The high-side output buffer includes a high speed level-shifting circuit that is referenced to the HS pin. An internal diode is used as part of a bootstrap circuit to provide the drive voltage for the high-side output.

### Startup and UVLO

The UVLO circuit forces the driver output low until the supply voltage exceeds the UVLO threshold. The low-side UVLO circuit, monitors the voltage between the VDD and VSS pins. The high-side UVLO circuit monitors the voltage between the HB and HS pins. Hysteresis in the UVLO circuit prevents noise and finite circuit impedance from causing chatter during turn-on.

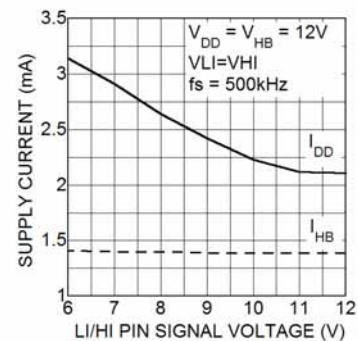
### Input Stage

The MIC4103 and MIC4104 have different input stages, which lets these parts cover a wide range of driver applications. Both the HI and LI pins are referenced to the VSS pin.

The MIC4103 has a high impedance, CMOS compatible input threshold and is recommended for applications

where the input signal is noisy or where the input signal swings the full range of voltage (from  $V_{DD}$  to GND). There is typically 400mV of hysteresis on the input pins throughout the VDD range. The hysteresis improves noise immunity and prevents input signals with slow rise times from falsely triggering the output. The threshold voltage of the MIC4103 varies proportionally with the VDD supply voltage.

The amplitude of the input signal affects the VDD supply current.  $V_{in}$  voltages that are a diode drop less than the VDD supply voltage will cause an increase in the VDD pin current. The graph in Figure 2 shows the typical dependence between  $I_{VDD}$  and  $V_{in}$  for  $V_{DD}=12V$ .



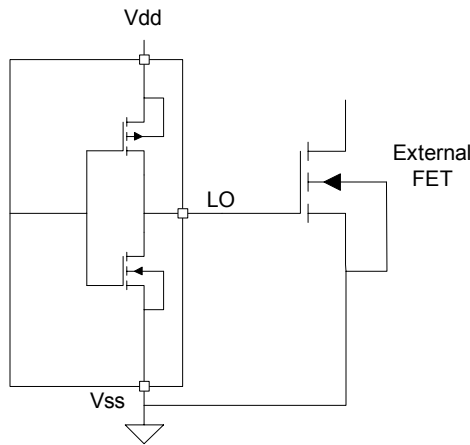
**Figure 2. MIC4103 Supply Current vs. Input Voltage**

The MIC4104 has a TTL compatible input range and is recommended for use with inputs signals whose amplitude is less than the supply voltage. The threshold level is independent of the  $V_{DD}$  supply voltage and there is no dependence between  $I_{VDD}$  and the input signal amplitude with the MIC4104. This feature makes the MIC4104 an excellent level translator that will drive high threshold MOSFETs from a low voltage PWM IC.

**Low-Side Driver**

A block diagram of the low-side driver is shown in Figure 3. The low-side driver is designed to drive a ground ( $V_{SS}$  pin) referenced N-channel MOSFET. Low driver impedances allow the external MOSFET to be turned on and off quickly. The rail-to-rail drive capability of the output ensures full enhancement of the external MOSFET.

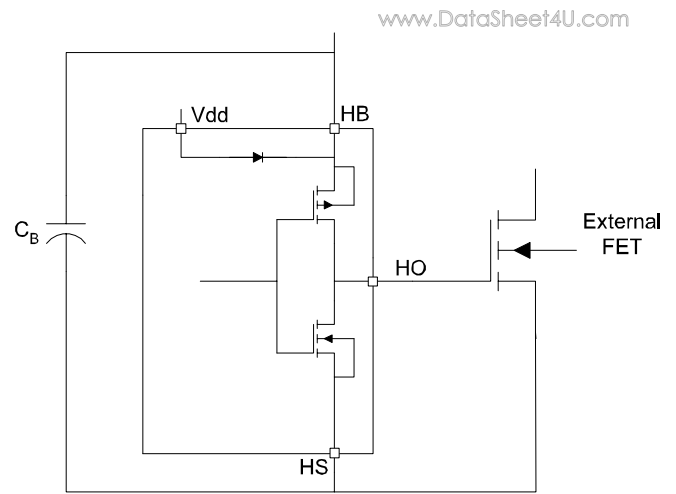
A high level applied to LI pin causes the upper driver FET to turn on and  $V_{DD}$  voltage is applied to the gate of the external MOSFET. A low level on the LI pin turns off the upper driver and turns on the low side driver to ground the gate of the external MOSFET.



**Figure 3. Low-Side Driver Block Diagram**

**High-Side Driver and Bootstrap Circuit**

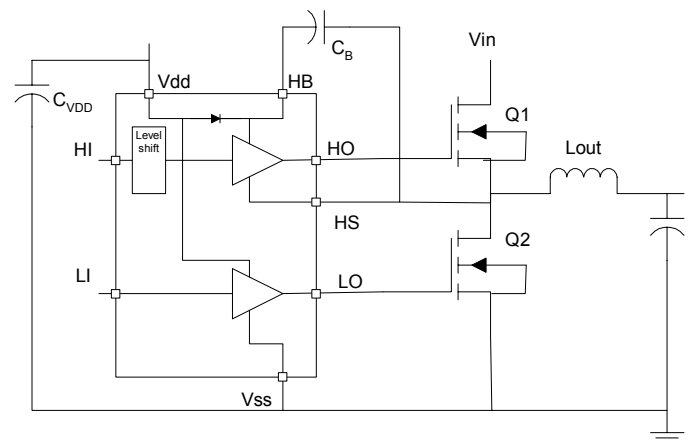
A block diagram of the high-side driver and bootstrap circuit is shown in Figure 4. This driver is designed to drive a floating N-channel MOSFET, whose source terminal is referenced to the HS pin.



**Figure 4. High-Side Driver and Bootstrap Circuit Block Diagram**

A low power, high speed, level shifting circuit isolates the low side ( $V_{SS}$  pin) referenced circuitry from the high-side ( $HS$  pin) referenced driver. Power to the high-side driver and UVLO circuit is supplied by the bootstrap circuit while the voltage level of the  $HS$  pin is shifted high.

The bootstrap circuit consists of an internal diode and external capacitor,  $C_B$ . In a typical application, such as the synchronous buck converter shown in Figure 5, the  $HS$  pin is at ground potential while the low-side MOSFET is on. The internal diode allows capacitor  $C_B$  to charge up to  $V_{DD} - V_D$  during this time (where  $V_D$  is the forward voltage drop of the internal diode). After the low-side MOSFET is turned off and the  $HO$  pin turns on, the voltage across capacitor  $C_B$  is applied to the gate of the upper external MOSFET. As the upper MOSFET turns on, voltage on the  $HS$  pin rises with the source of the high-side MOSFET until it reaches  $V_{IN}$ . As the  $HS$  and  $HB$  pin rise, the internal diode is reverse biased preventing capacitor  $C_B$  from discharging.



**Figure 5. High-Side Driver and Bootstrap Circuit**

**Power Dissipation Considerations**

Power dissipation in the driver can be separated into three areas:

- Internal diode dissipation in the bootstrap circuit
- Internal driver dissipation
- Quiescent current dissipation used to supply the internal logic and control functions.

**Bootstrap Circuit Power Dissipation**

Power dissipation of the internal bootstrap diode primarily comes from the average charging current of the  $C_B$  capacitor times the forward voltage drop of the diode. Secondary sources of diode power dissipation are the reverse leakage current and reverse recovery effects of the diode.

The average current drawn by repeated charging of the high-side MOSFET is calculated by:

$$I_{F(AVE)} = Q_{gate} \times f_S$$

where :  $Q_{gate}$  = Total Gate Charge at  $V_{HB}$

$f_S$  = gate drive switching frequency

The average power dissipated by the forward voltage drop of the diode equals:

$$P_{diode_{fwd}} = I_{F(AVE)} \times V_F$$

where :  $V_F$  = Diode forward voltage drop

The value of  $V_F$  should be taken at the peak current through the diode, however, this current is difficult to calculate because of differences in source impedances. The peak current can either be measured or the value of  $V_F$  at the average current can be used and will yield a good approximation of diode power dissipation.

The reverse leakage current of the internal bootstrap diode is typically 11µA at a reverse voltage of 100V and 125°C. Power dissipation due to reverse leakage is typically much less than 1mW and can be ignored.

Reverse recovery time is the time required for the injected minority carriers to be swept away from the depletion region during turn-off of the diode. Power dissipation due to reverse recovery can be calculated by computing the average reverse current due to reverse recovery charge times the reverse voltage across the diode. The average reverse current and power dissipation due to reverse recovery can be estimated by:

$$I_{RR(AVE)} = 0.5 \times I_{RRM} \times t_{rr} \times f_S$$

$$P_{diode_{RR}} = I_{RR(AVE)} \times V_{REV}$$

where :  $I_{RRM}$  = Peak Reverse Recovery Current

$t_{rr}$  = Reverse Recovery Time

**Application Information**

The total diode power dissipation is:

$$P_{diode_{total}} = P_{diode_{fwd}} + P_{diode_{RR}}$$

An optional external bootstrap diode may be used instead of the internal diode (Figure 6). An external diode may be useful if high gate charge MOSFETs are being driven and the power dissipation of the internal diode is contributing to excessive die temperatures. The voltage drop of the external diode must be less than the internal diode for this option to work. The reverse voltage across the diode will be equal to the input voltage minus the  $V_{DD}$  supply voltage. A 100V Schottky diode will work for most 72V input telecom applications. The above equations can be used to calculate power dissipation in the external diode, however, if the external diode has significant reverse leakage current, the power dissipated in that diode due to reverse leakage can be calculated as:

$$P_{diode_{REV}} = I_R \times V_{REV} \times (1 - D)$$

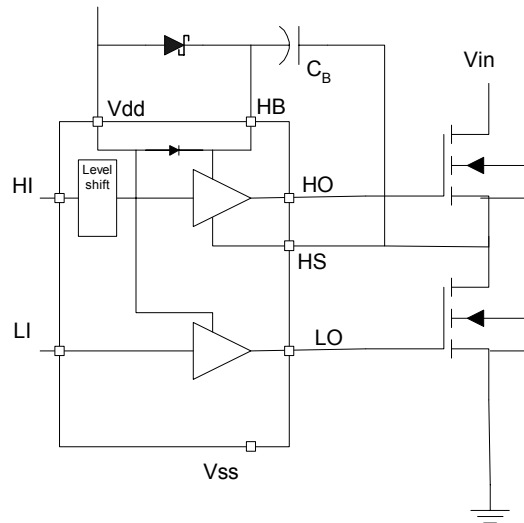
where :  $I_R$  = Reverse current flow at  $V_{REV}$  and  $T_J$

$V_{REV}$  = Diode Reverse Voltage

$D$  = Duty Cycle =  $t_{ON} / f_S$

$f_S$  = switching frequency of the power supply

The on-time is the time the high-side switch is conducting. In most power supply topologies, the diode is reverse biased during the switching cycle off-time.

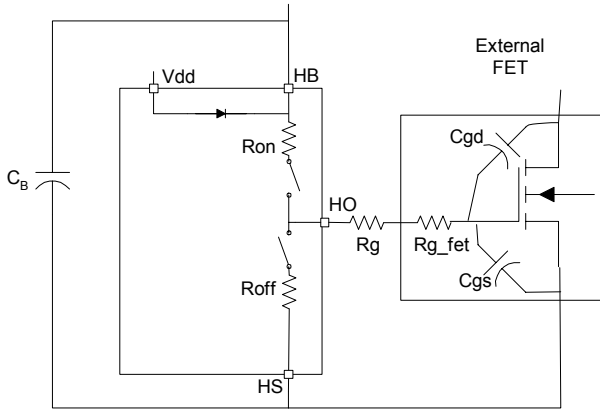


**Figure 6. Optional Bootstrap Diode**

**Gate Driver Power Dissipation**

Power dissipation in the output driver stage is mainly caused by charging and discharging the gate to source

and gate to drain capacitance of the external MOSFET. Figure 7 shows a simplified equivalent circuit of the MIC4103 driving an external MOSFET.



**Figure 7. MIC4103 Driving an External MOSFET**

*Dissipation during the external MOSFET Turn-On*

Energy from capacitor  $C_B$  is used to charge up the input capacitance of the MOSFET ( $C_{GD}$  and  $C_{GS}$ ). The energy delivered to the MOSFET is dissipated in the three resistive components,  $R_{ON}$ ,  $R_G$ , and  $R_{G\_FET}$ .  $R_{ON}$  is the on resistance of the upper driver MOSFET in the MIC4103.  $R_G$  is the series resistor (if any) between the driver IC and the MOSFET.  $R_{G\_FET}$  is the gate resistance of the MOSFET.  $R_{G\_FET}$  is usually listed in the power MOSFET's specifications. The ESR of capacitor  $C_B$  and the resistance of the connecting trace can be ignored since they are much less than  $R_{ON}$  and  $R_{G\_FET}$ .

The effective capacitance of  $C_{GD}$  and  $C_{GS}$  is difficult to calculate since they vary non-linearly with  $I_D$ ,  $V_{GS}$ , and  $V_{DS}$ . Fortunately, most power MOSFET specifications include a typical graph of total gate charge vs.  $V_{GS}$ . Figure 8 shows a typical gate charge curve for an arbitrary power MOSFET. This chart shows that for a gate voltage of 10V, the MOSFET requires about 23.5nC of charge. The energy dissipated by the resistive components of the gate drive circuit during turn-on is calculated as:

$$E = \frac{1}{2} \times C_{iss} \times V_{gs}^2$$

but

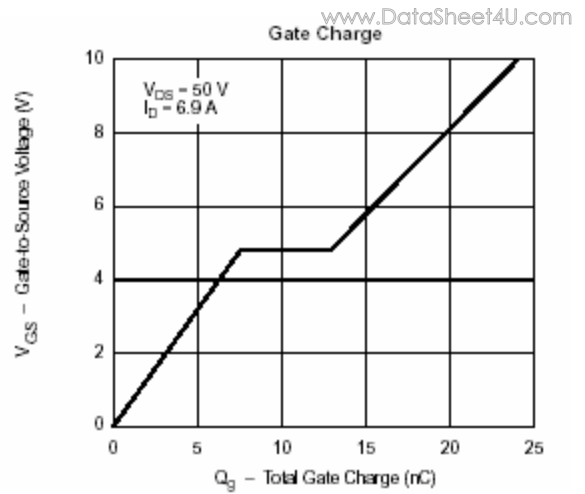
$$Q = C \times V$$

so

$$E = 1/2 \times Q_g \times V_{gs}$$

where

$C_{iss}$  is the total gate capacitance of the MOSFET



**Figure 8. Typical Gate Charge vs.  $V_{GS}$**

The same energy is dissipated by  $R_{OFF}$ ,  $R_G$ , and  $R_{G\_FET}$  when the driver IC turns the MOSFET off. Assuming  $R_{ON}$  is approximately equal to  $R_{OFF}$ , the total energy and power dissipated by the resistive drive elements is:

$$E_{driver} = Q_G \times V_{GS}$$

and

$$P_{driver} = Q_G \times V_{GS} \times fs$$

where

$E_{driver}$  is the energy dissipated per switching cycle

$P_{driver}$  is the power dissipated by switching the MOSFET on and off

$Q_G$  is the total gate charge at  $V_{gs}$

$V_{GS}$  is the gate to source voltage on the MOSFET

$fs$  is the switching frequency of the gate drive circuit

The power dissipated inside the MIC4103/4 is equal to the ratio of  $R_{ON}$  &  $R_{OFF}$  to the external resistive losses in  $R_G$  and  $R_{G\_FET}$ . Letting  $R_{ON} = R_{OFF}$ , the power dissipated in the MIC4103 due to driving the external MOSFET is:

$$P_{diss\_drive} = P_{driver} \frac{R_{ON}}{R_{ON} + R_G + R_{G\_FET}}$$

**Supply Current Power Dissipation**

Power is dissipated in the MIC4103 even if there is nothing being driven. The supply current is drawn by the bias for the internal circuitry, the level shifting circuitry, and shoot-through current in the output drivers. The supply current is proportional to operating frequency and the  $V_{DD}$  and  $V_{HB}$  voltages. The typical characteristic graphs show how supply current varies with switching frequency and supply voltage.

The power dissipated by the MIC4103 due to supply current is:

$$P_{diss\_supply} = V_{DD} \times I_{DD} + V_{HB} \times I_{HB}$$

### Total power dissipation and Thermal Considerations

Total power dissipation in the MIC4103 or MIC4104 is equal to the power dissipation caused by driving the external MOSFETs, the supply current, and the internal bootstrap diode.

$$P_{diss_{total}} = P_{diss_{supply}} + P_{diss_{drive}} + P_{diode_{total}}$$

The die temperature may be calculated once the total power dissipation is known.

$$T_J = T_A + P_{diss_{total}} \times \theta_{JA}$$

where :

$T_A$  is the maximum ambient temperature

$T_J$  is the junction temperature (°C)

$P_{diss_{total}}$  is the power dissipation of the MIC4103/4

$\theta_{JC}$  is the thermal resistance from junction to ambient air (°C/W)

### Propagation Delay and Delay Matching and other Timing Considerations

Propagation delay and signal timing is an important consideration in a high performance power supply. The MIC4103 is designed not only to minimize propagation delay but to minimize the mismatch in delay between the high-side and low-side drivers.

Fast propagation delay between the input and output drive waveform is desirable. It improves overcurrent protection by decreasing the response time between the control signal and the MOSFET gate drive. Minimizing propagation delay also minimizes phase shift errors in power supplies with wide bandwidth control loops.

Many power supply topologies use two switching MOSFETs operating 180° out of phase from each other. These MOSFETs must not be on at the same time or a short circuit will occur, causing high peak currents and higher power dissipation in the MOSFETs. The MIC4103 and MIC4104 output gate drivers are not designed with anti-shoot-through protection circuitry. The output drive signals simply follow the inputs. The power supply design must include timing delays (dead-time) between the input signals to prevent shoot-through. The MIC4103 & MIC4104 drivers specify delay matching between the two drivers to help improve power supply performance by reducing the amount of dead-time required between the input signals.

Care must be taken to insure the input signal pulse width is greater than the minimum specified pulse width. An input signal that is less than the minimum pulse width may result in no output pulse or an output pulse whose width is significantly less than the input.

The maximum duty cycle (ratio of high side on-time to switching period) is controlled by the minimum pulse width of the low side and by the time required for the  $C_B$  capacitor to charge during the off-time. Adequate time

must be allowed for the  $C_B$  capacitor to charge up before the high-side driver is turned on.

### Decoupling and Bootstrap Capacitor Selection

Decoupling capacitors are required for both the low side (Vdd) and high side (HB) supply pins. These capacitors supply the charge necessary to drive the external MOSFETs as well as minimize the voltage ripple on these pins. The capacitor from HB to HS serves double duty by providing decoupling for the high-side circuitry as well as providing current to the high-side circuit while the high-side external MOSFET is on. Ceramic capacitors are recommended because of their low impedance and small size. Z5U type ceramic capacitor dielectrics are not recommended due to the large change in capacitance over temperature and voltage. A minimum value of 0.1uF is required for each of the capacitors, regardless of the MOSFETs being driven. Larger MOSFETs may require larger capacitance values for proper operation. The voltage rating of the capacitors depends on the supply voltage, ambient temperature, and the voltage derating used for reliability. 25V rated X5R or X7R ceramic capacitors are recommended for most applications. The minimum capacitance value should be increased if low voltage capacitors are used since even good quality dielectric capacitors, such as X5R, will lose 40% to 70% of their capacitance value at the rated voltage.

Placement of the decoupling capacitors is critical. The bypass capacitor for Vdd should be placed as close as possible between the Vdd and Vss pins. The bootstrap capacitor ( $C_B$ ) for the HB supply pin must be located as close as possible between the HB and HS pins. The trace connections must be short, wide, and direct. The use of a ground plane to minimize connection impedance is recommended. Refer to the section on layout and component placement for more information.

The voltage on the bootstrap capacitor drops each time it delivers charge to turn on the MOSFET. The voltage drop depends on the gate charge required by the MOSFET. Most MOSFET specifications specify gate charge vs. Vgs voltage. Based on this information and a recommended  $\Delta V_{HB}$  of less than 0.1V, the minimum value of bootstrap capacitance is calculated as:

$$C_B \geq \frac{Q_{gate}}{\Delta V_{HB}}$$

where :  $Q_{gate}$  = Total Gate Charge at  $V_{HB}$

$\Delta V_{HB}$  = Voltage drop at the HB pin

The decoupling capacitor for the Vdd input may be calculated with the same formula, however, the two capacitors are usually equal in value.

### Grounding, Component Placement, and Circuit Layout

Nanosecond switching speeds and ampere peak currents

in and around the MIC4103 and MIC4104 drivers require proper placement and trace routing of all components. Improper placement may cause degraded noise immunity, false switching, excessive ringing or circuit latch-up.

Figure 9 shows the critical current paths when the driver outputs go high and turn on the external MOSFETs. It also helps demonstrate the need for a low impedance ground plane. Charge needed to turn-on the MOSFET gates comes from the decoupling capacitors  $C_{VDD}$  and  $C_B$ . Current in the low-side gate driver flows from  $C_{VDD}$  through the internal driver, into the MOSFET gate and out the Source. The return connection back to the decoupling capacitor is made through the ground plane. Any inductance or resistance in the ground return path causes a voltage spike or ringing to appear on the source of the MOSFET. This voltage works against the gate drive voltage and can either slow down or turn off the MOSFET during the period where it should be turned on.

Current in the high-side driver is sourced from capacitor  $C_B$  and flows into the HB pin and out the HO pin, into the gate of the high side MOSFET. The return path for the current is from the source of the MOSFET and back to capacitor  $C_B$ . The high-side circuit return path usually does not have a low impedance ground plane so the trace connections in this critical path should be short and wide to minimize parasitic inductance. As with the low-side circuit, impedance between the MOSFET source and the decoupling capacitor causes negative voltage feedback which fights the turn-on of the MOSFET.

It is important to note that capacitor  $C_B$  must be placed close to the HB and HS pins. This capacitor not only provides all the energy for turn-on but it must also keep HB pin noise and ripple low for proper operation of the high-side drive circuitry.

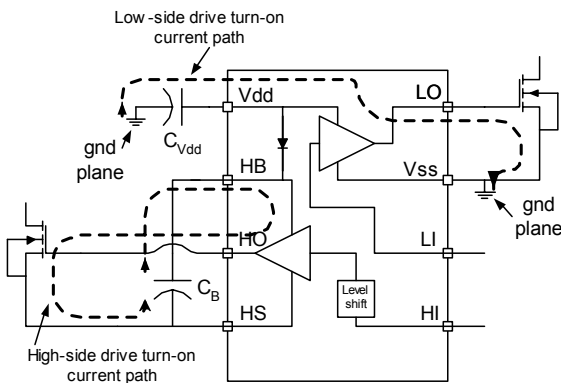


Figure 9. Turn-On Current Paths

Figure 10 shows the critical current paths when the driver outputs go low and turn off the external MOSFETs. Short,

low impedance connections are important during turn-off for the same reasons given in the turn-on explanation. Remember that during turn-off current flowing through the internal diode replenishes charge in the bootstrap capacitor,  $C_B$ .

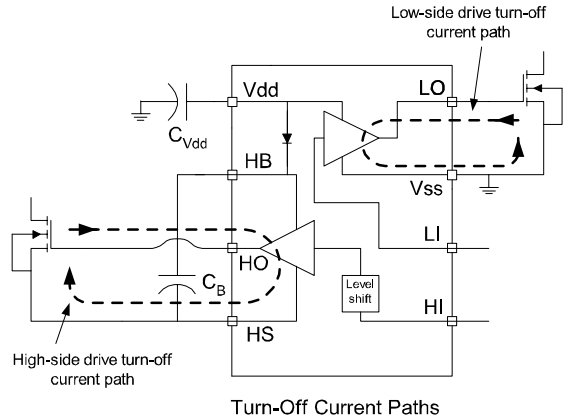


Figure 10. Turn-Off Current Paths

The following circuit guidelines should be adhered to for optimum circuit performance:

1. The  $V_{DD}$  and HB bypass capacitors must be placed close to the supply and ground pins. It is critical that the trace length between the high side decoupling capacitor ( $C_B$ ) and the HB & HS pins be minimized to reduce trace inductance.
2. A ground plane should be used to minimize parasitic inductance and impedance of the return paths. The MIC4103 is capable of greater than 2A peak currents and any impedance between the MIC4103, the decoupling capacitors, and the external MOSFET will degrade the performance of the driver.
3. Trace out the high  $di/dt$  and  $dv/dt$  paths, as shown in Figures 9 and 10 and minimize trace length and loop area for these connections. Minimizing these parameters decreases the parasitic inductance and the radiated EMI generated by fast rise and fall times.

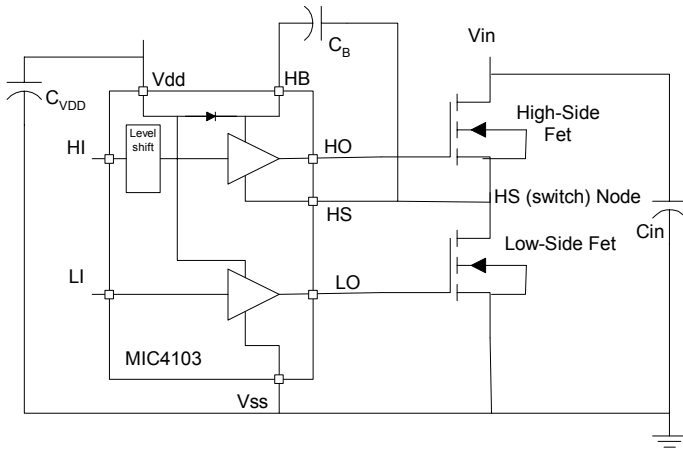
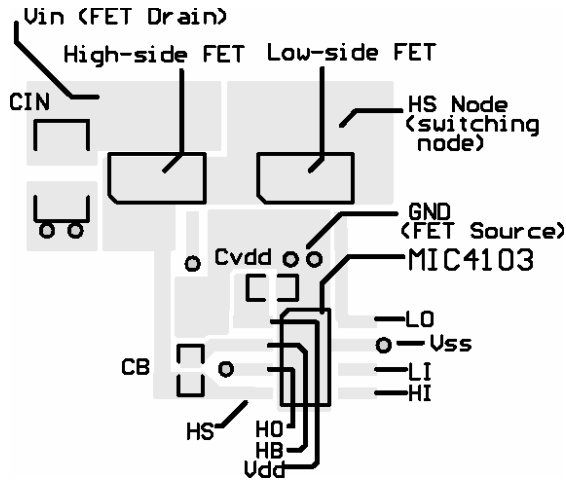


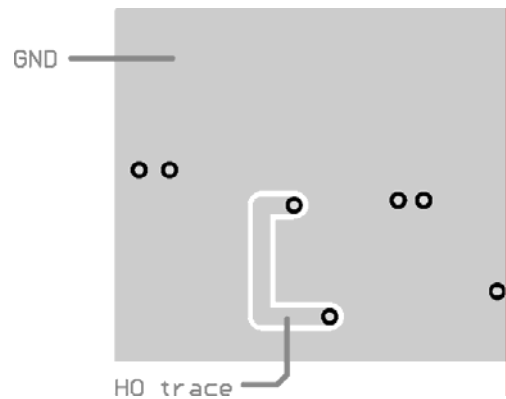
Figure 11. Synchronous Buck Converter Power Stage

A typical layout of a synchronous Buck converter power stage (Figure 11) is shown in Figure 12.

The circuit is configured as a synchronous buck power stage. The high-side MOSFET drain connects to the input supply voltage and the source connects to the switching node. The low-side MOSFET drain connects to the switching node and its source is connected to ground. The buck converter output inductor (not shown) would connect to the switching node. The high-side drive trace, HO, is routed on top of its return trace, HS, to minimize loop area and parasitic inductance. The low-side drive trace LO is routed over the ground plane which minimizes the impedance of that current path. The decoupling capacitors,  $C_B$  and  $C_{VDD}$  are placed to minimize trace length between the capacitors and their respective pins. This close placement is necessary to efficiently charge capacitor  $C_B$  when the HS node is low. All traces are 0.025" wide or greater to reduce impedance.  $C_{in}$  is used to decouple the high current path through the MOSFETs.



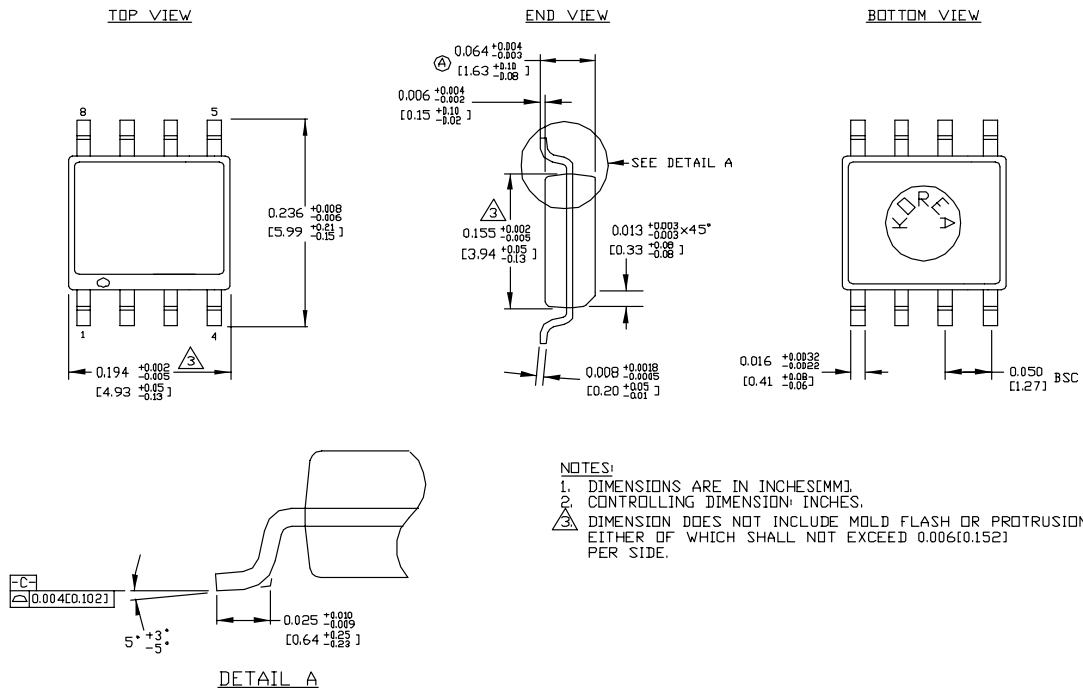
Top Side



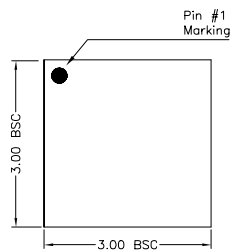
Bottom Side

Figure 12. Typical Layout of a Synchronous Buck Converter Power Stage

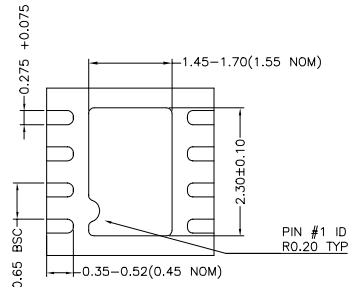
### Package Information



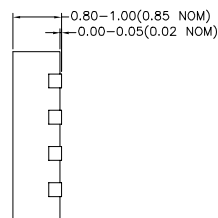
### 8-Pin SOIC (M)



TOP VIEW



BOTTOM VIEW



SIDE VIEW

### 8-Pin MLF<sup>®</sup> (ML)



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