MIC45205-1/-2

26V/6A DC-to-DC Power Module

General Description

Micrel's MIC45205 is a synchronous step-down regulator module, featuring a unique adaptive ON-time control architecture. The module incorporates a DC-to-DC controller, power MOSFETs, bootstrap diode, bootstrap capacitor, and an inductor in a single package; simplifying the design and layout process for the end user.

This highly-integrated solution expedites system design and improves product time-to-market. The internal MOSFETs and inductor are optimized to achieve high efficiency at a low output voltage. The fully-optimized design can deliver up to 6A current under a wide input voltage range of 4.5V to 26V, without requiring additional cooling.

The MIC45205-1 uses Micrel's HyperLight Load® (HLL) MIC45205-2 uses Micrel's Hyper Speed Control™ architecture which enables ultra-fast load transient response, allowing for a reduction of output capacitance. The MIC45205 offers 1% output accuracy that can be adjusted from 0.8V to 5.5V with two external resistors. Additional features include thermal shutdown protection, input undervoltage lockout, adjustable current limit, and short circuit protection. The MIC45205 allows for safe start-up into a pre-biased output.

Datasheet and other support documentation can be found on Micrel's web site at: www.micrel.com.

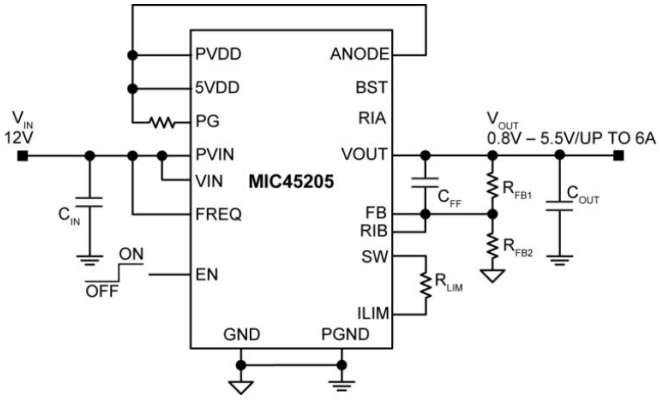
Features

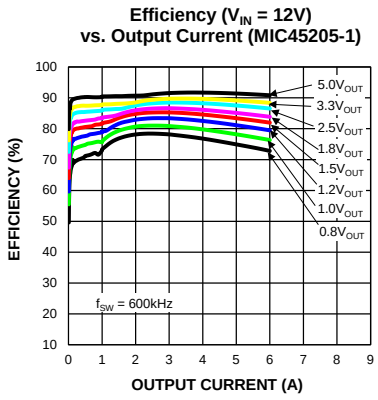
- No compensation required
- Up to 6A output current
- >93% peak efficiency
- Output voltage: 0.8V to 5.5V with ±1% accuracy
- Adjustable switching frequency from 200kHz to 600kHz
- Enable input and open-drain power good output
- Hyper Speed Control (MIC45205-2) architecture enables fast transient response
- HyperLight Load (MIC45205-1) improves light load efficiency
- Supports safe startup into pre-biased output
- CISPR22, Class B compliant
- –40°C to +125°C junction temperature range
- Thermal-shutdown protection
- Short-circuit protection with hiccup mode
- Adjustable current limit
- Available in 52-pin 8mm × 8mm × 3mm QFN package

Applications

- High power density point-of-load conversion
- Servers, routers, Networking, and base stations
- FPGAs, DSP, and low-voltage ASIC power supplies
- Industrial and medical equipment

Typical Application





Hyper Speed Control is a trademark of Micrel, Inc.

HyperLight Load is a registered trademark of Micrel, Inc.

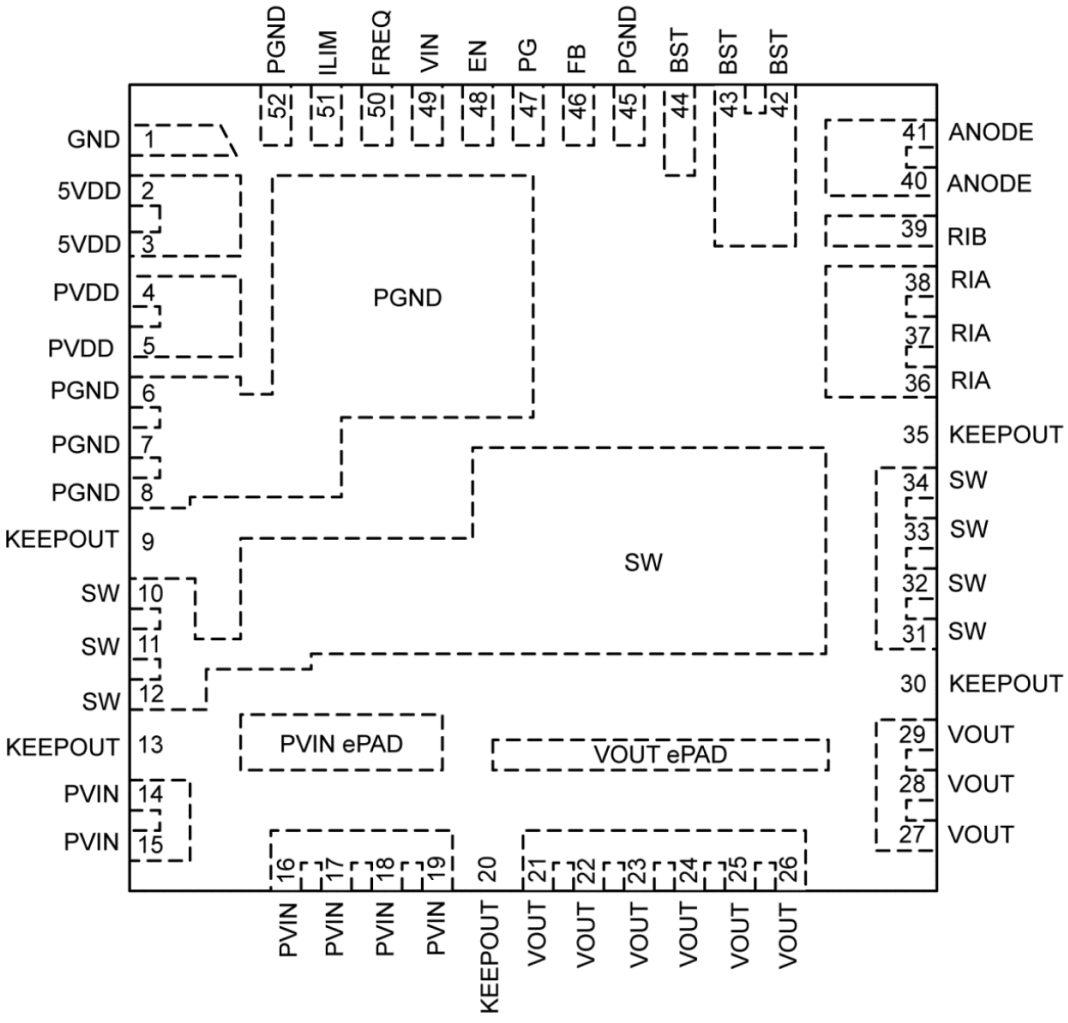
Ordering Information[1]

Part Number	Switching Frequency	Features	Junction Temperature Range	Package	Lead Finish
MIC45205-1YMP	200kHz to 600kHz	Hyper Light Load	–40°C to +125°C	52-pin 8mm × 8mm × 3mm QFN	Pb-Free
MIC45205-2YMP	200kHz to 600kHz	Hyper Speed Control	–40°C to +125°C	52-pin 8mm × 8mm × 3mm QFN	Pb-Free

Note:

1. Devices are ESD sensitive. Handling precautions are recommended.

Pin Configuration



52-Pin 8mm × 8mm × 3mm QFN
(Top View)

Pin Description

MIC45205 Pin Number	Pin Name	Pin Function
1	GND	Analog Ground. Connect bottom feedback resistor to GND. GND and PGND should be connected together at a low impedance point.
2, 3	5VDD	Internal +5V Linear Regulator Output. Powered by VIN, 5VDD is the internal supply bus for the device. In the applications with VIN < +5.5V, 5VDD should be tied to VIN to by-pass the linear regulator.
4, 5	PVDD	PVDD. Supply input for the internal low-side power MOSFET driver.
6 – 8, 45, 52	PGND	Power Ground. PGND is the return path for the step-down power module power stage. The PGND pin connects to the sources of internal low-side power MOSFET, the negative terminals of input capacitors, and the negative terminals of output capacitors.
10 – 12, 31 – 34	SW	The SW pin connects directly to the switch node. Due to the high-speed switching on this pin, the SW pin should be routed away from sensitive nodes. The SW pin also senses the current by monitoring the voltage across the low-side MOSFET during OFF time.
14 –19	PVIN	Power Input Voltage. Connection to the drain of the internal high side power MOSFET. Connect an input capacitor from PVIN to PGND.
21 – 29	VOUT	Output Voltage. Connected to the internal inductor, the output capacitor should be connected from this pin to PGND as close to the module as possible.
36 – 38	RIA	Ripple Injection Pin A. Leave floating, no connection.
39	RIB	Ripple Injection Pin B. Connect this pin to FB.
40, 41	ANODE	Anode Bootstrap Diode. Anode connection of internal bootstrap diode, this pin should be connected to the PVDD pin.
42 – 44	BST	Connection to the internal bootstrap circuitry and high-side power MOSFET drive circuitry. Connect all three BST pins together.
46	FB	Feedback. Input to the transconductance amplifier of the control loop. The FB pin is referenced to 0.8V. A resistor divider connecting the feedback to the output is used to set the desired output voltage. Connect the bottom resistor from FB to GND.
47	PG	Power Good. Open drain output. If used, connect to an external pull-up resistor of at least 10kohm between PG and the external bias voltage.
48	EN	Enable. A logic signal to enable or disable the step-down regulator module operation. The EN pin is TTL/CMOS compatible. Logic high = enable, logic low = disable or shutdown. EN pin has an internal 1MΩ (typical) pull-down resistor to GND. Do not leave floating
49	VIN	Internal 5V Linear Regulator Input. A 1µF ceramic capacitor from VIN to GND is required for decoupling.
50	FREQ	Switching Frequency Adjust. Use a resistor divider from VIN to GND to program the switching frequency. Connecting FREQ to VIN sets frequency = 600kHz.
51	ILIM	Current Limit. Connect a resistor between ILIM and SW to program the current limit.
9, 13, 20, 30, 35	KEEPOUT	Depopulated pin positions.
–	PVIN ePAD	PVIN Exposed Pad. Internally connected to PVIN pins. Please see *PCB Layout Recommendations* section.
–	VOUT ePAD	VOUT Exposed Pad. Internally connected to VOUT pins. Please see *PCB Layout Recommendations* section.

Absolute Maximum Ratings[2]

V_{PVIN}, V_{VIN} to PGND ..... –0.3V to +30V
V_{PVDD}, V_{5VDD}, V_{ANODE} to PGND..... –0.3V to +6V
V_{SW}, V_{FREQ}, V_{ILIM}, V_{EN} to PGND ..... –0.3V to (V_{IN} +0.3V)
V_{BST} to V_{SW} ..... –0.3V to 6V
V_{BST} to PGND ..... –0.3V to 36V
V_{PG} to PGND ..... –0.3V to (5VDD + 0.3V)
V_{FB}, V_{RIB} to PGND ..... –0.3V to (5VDD + 0.3V)
PGND to GND ..... –0.3V to +0.3V
Junction Temperature ..... +150°C
Storage Temperature (T_S) ..... –65°C to +150°C
Lead Temperature (soldering, 10s) ..... 260°C

Operating Ratings[3]

Supply Voltage (V_{PVIN}, V_{VIN}) ..... 4.5V to 26V
Output Current 6A
Enable Input (V_{EN}) ..... 0V to V_{IN}
Power Good (V_{PG}) ..... 0V to 5VDD
Junction Temperature (T_J) ..... –40°C to +125°C
Junction Thermal Resistance[4]
8mm × 8mm × 3mm QFN-52 (θ_{JA}) ..... 21.7°C/W
8mm × 8mm × 3mm QFN-52 (θ_{JC}) ..... 5.0°C/W

Electrical Characteristics[5]

V_{IN} = V_{EN} = 12V, V_{OUT} = 3.3V, V_{BST} – V_{SW} = 5V, T_J = +25ºC. **Bold** values indicate –40ºC < T_J < +125ºC, unless otherwise noted.

Parameter	Condition	Min.	Typ.	Max.	Units
Power Supply Input					
Input Voltage Range (V_{PVIN}, V_{IN})		**4.5**		**26**	V
Quiescent Supply Current (MIC45205-1)	V_{FB} = 1.5V		0.35	**0.75**	mA
Quiescent Supply Current (MIC45205-2)	V_{FB} = 1.5V		2.1	**3**	mA
Operating Current	V_{PVIN} = V_{IN} = 12V, V_{OUT} = 1.8V, I_{OUT} = 0A f_{SW} = 600kHz (MIC45205-2)		31		mA
Shutdown Supply Current	SW = unconnected, V_{EN} = 0V		0.1	**10**	µA
5VDD Output					
5VDD Output Voltage	V_{IN} = 7V to 26V, I_{5VDD} = 10mA	**4.8**	5.1	**5.4**	V
5VDD UVLO Threshold	V_{5VDD} rising	**3.8**	4.2	**4.6**	V
5VDD UVLO Hysteresis	V_{5VDD} falling		400		mV
LDO Load Regulation	I_{5VDD} = 0 to 40mA	0.6	2	3.6	%
Reference					
Feedback Reference Voltage	T_J = 25°C	0.792	0.8	0.808	V
	–40°C ≤ T_J ≤ 125°C	**0.784**	0.8	**0.816**	
FB Bias Current	V_{FB} = 0.8V		5	**500**	nA

Notes:

2. Exceeding the absolute maximum rating may damage the device.
3. The device is not guaranteed to function outside operating range.
4. θ_{JA} and θ_{JC} were measured using the MIC45205 evaluation board.
5. Specification for packaged product only.

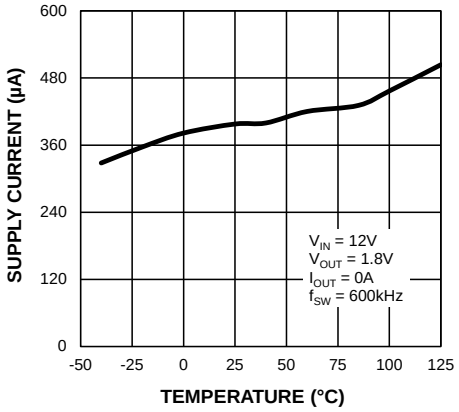
Electrical Characteristics[5] (Continued)

$V_{IN} = V_{EN} = 12V$, $V_{OUT} = 3.3V$, $V_{BST} - V_{SW} = 5V$, $T_J = +25°C$. **Bold** values indicate $-40°C < T_J < +125°C$, unless otherwise noted.

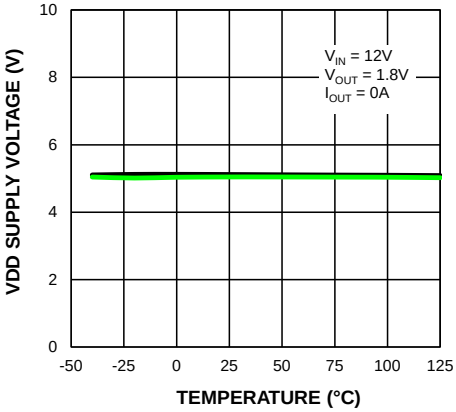
Parameter	Condition	Min.	Typ.	Max.	Units
Enable Control					
EN Logic Level High		**1.8**			V
EN Logic Level Low				**0.6**	V
EN Hysteresis			200		mV
EN Bias Current	$V_{EN} = 12V$		5	**10**	µA
Oscillator					
Switching Frequency	$V_{FREQ} = V_{IN}$, $I_{OUT} = 2A$	**400**	600	**750**	kHz
	$V_{FREQ} = 50\% V_{IN}$, $I_{OUT} = 2A$		350		
Maximum Duty Cycle			85		%
Minimum Duty Cycle	$V_{FB} = 1V$		0		%
Minimum Off-Time		140	200	260	ns
Soft-Start					
Soft-Start Time			5		ms
Short-Circuit Protection					
Current-Limit Threshold	$V_{FB} = 0.79V$	–30	–14	0	mV
Short-Circuit Threshold	$V_{FB} = 0V$	–23	–7	9	mV
Current-Limit Source Current	$V_{FB} = 0.79V$	55	70	85	µA
Short-Circuit Source Current	$V_{FB} = 0V$	25	35	45	µA
Leakage					
SW, BST Leakage Current				10	µA
FREQ Leakage Current				10	µA
Power Good (PG)					
PG Threshold Voltage	Sweep V_{FB} from Low-to-High	**85**	90	**95**	% V_{OUT}
PG Hysteresis	Sweep V_{FB} from High-to-Low		6		% V_{OUT}
PG Delay Time	Sweep V_{FB} from Low-to-High		100		µs
PG Low Voltage	$V_{FB} < 90\% \times V_{NOM}$, $I_{PG} = 1mA$		70	**200**	mV
Thermal Protection					
Overtemperature Shutdown	T_J Rising		160		°C
Overtemperature Shutdown Hysteresis			15		°C

Typical Characteristics

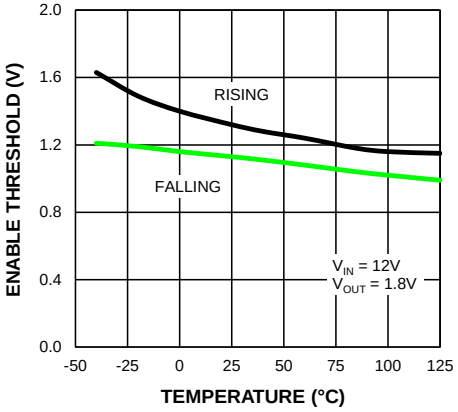
VIN Operating Supply Current vs. Temperature (MIC45205-1)



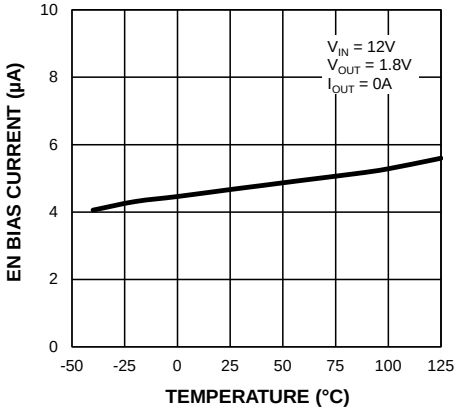
VDD Supply Voltage vs. Temperature



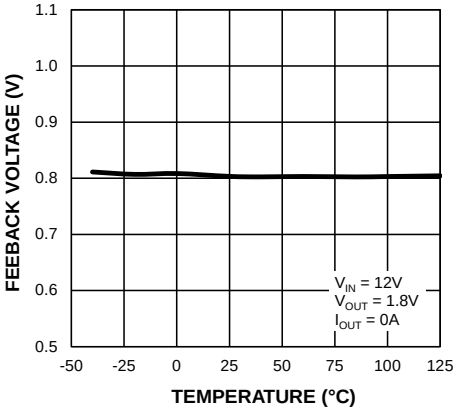
Enable Threshold vs. Temperature



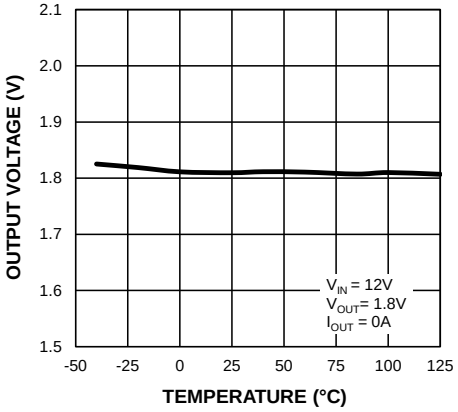
EN Bias Current vs. Temperature



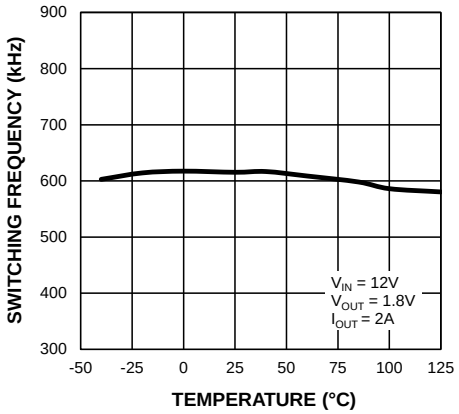
Feedback Voltage vs. Temperature



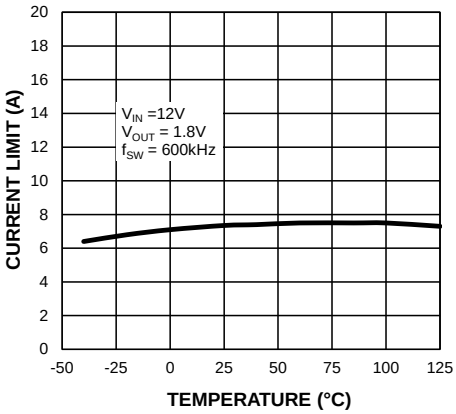
Output Voltage vs. Temperature



Switching Frequency vs. Temperature

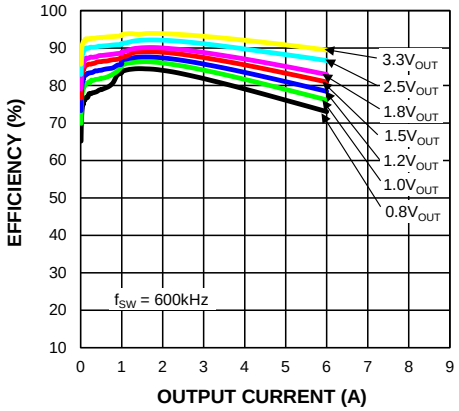


Output Peak Current Limit vs. Temperature

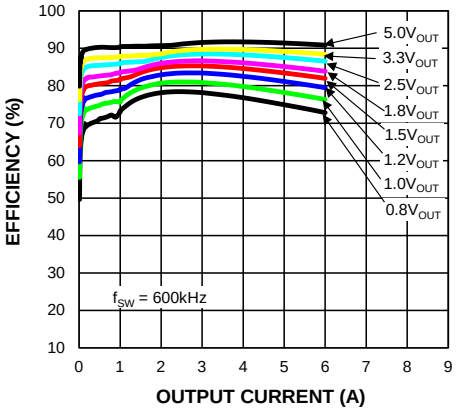


Typical Characteristics (Continued)

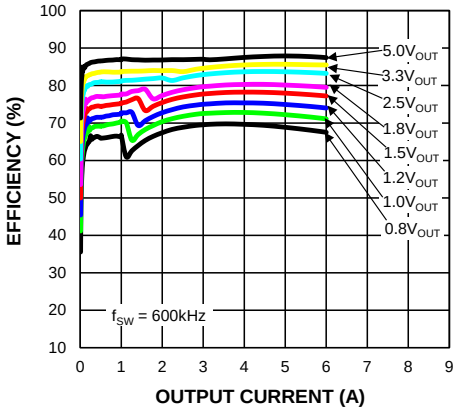
Efficiency (V_{IN} = 5V) vs. Output Current (MIC4205-1)



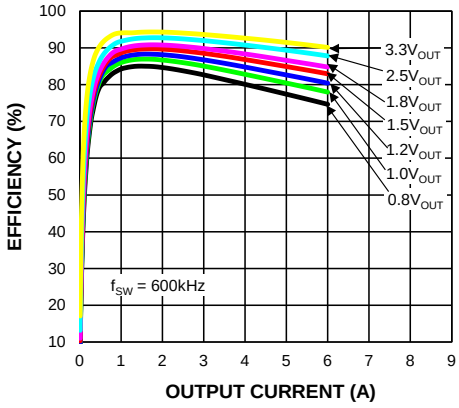
Efficiency (V_{IN} = 12V) vs. Output Current (MIC45205-1)



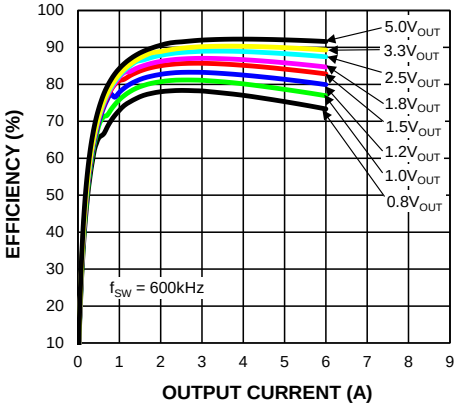
Efficiency (V_{IN} = 24V) vs. Output Current (MIC45205-1)



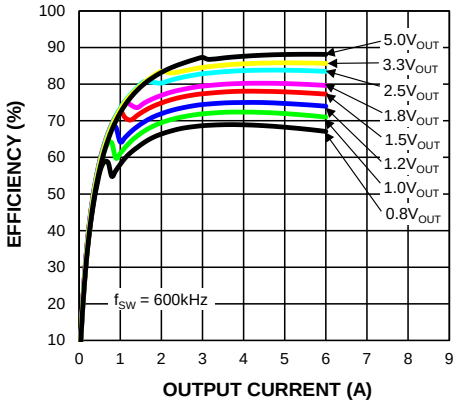
Efficiency (V_{IN} = 5V) vs. Output Current (MIC45205-2)



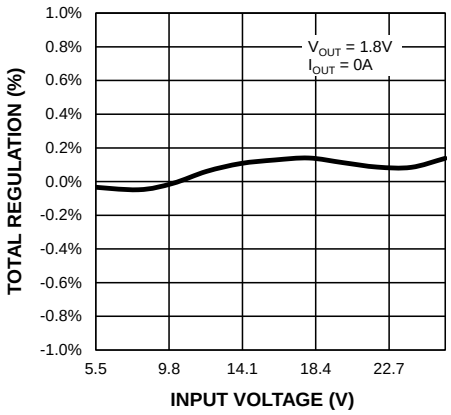
Efficiency (V_{IN} = 12V) vs. Output Current (MIC45205-2)



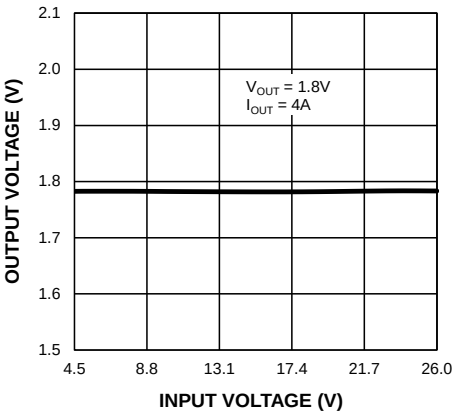
Efficiency (V_{IN} = 24V) vs. Output Current (MIC45205-2)



Line Regulation

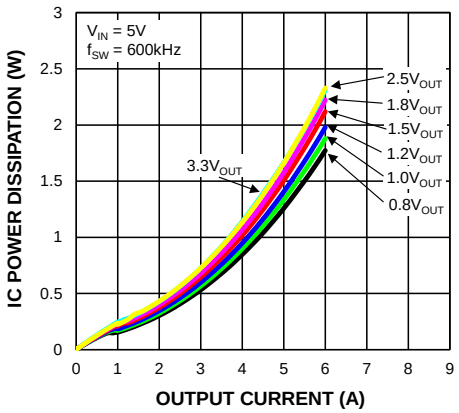


Output Voltage vs. Input Voltage

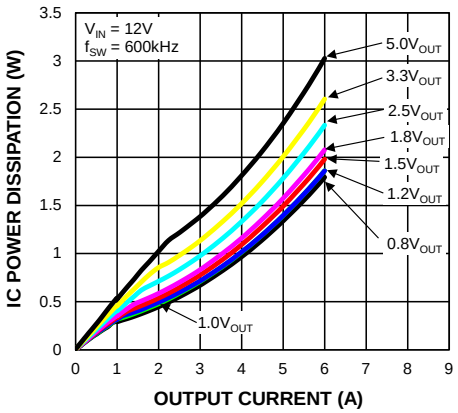


Typical Characteristics (Continued)

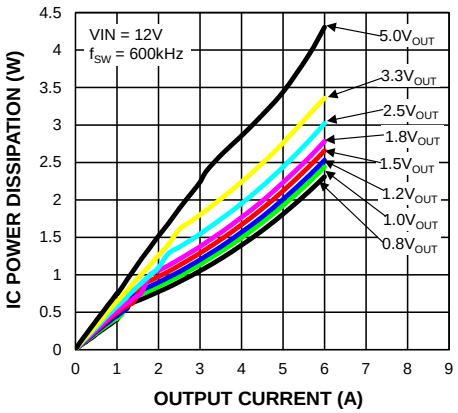
IC Power Dissipation (V_{IN} = 5V) vs. Output Current



IC Power Dissipation (V_{IN} = 12V) vs. Output Current

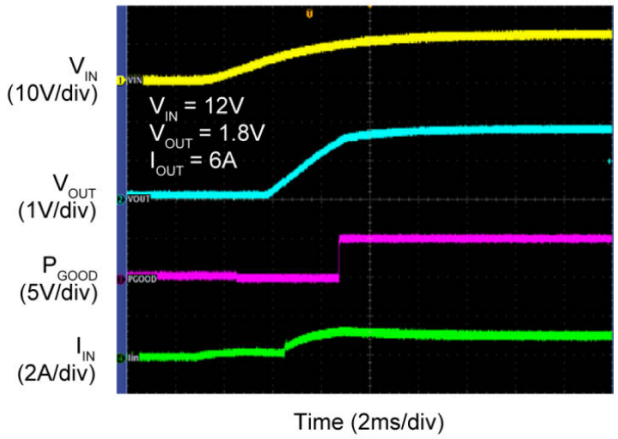


IC Power Dissipation (VIN = 24V) vs. Output Current

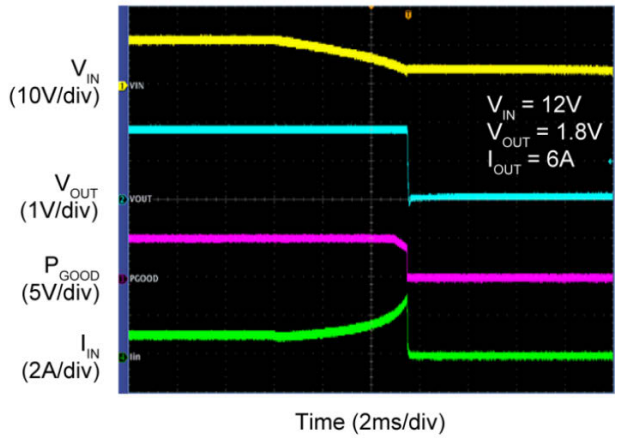


Functional Characteristics

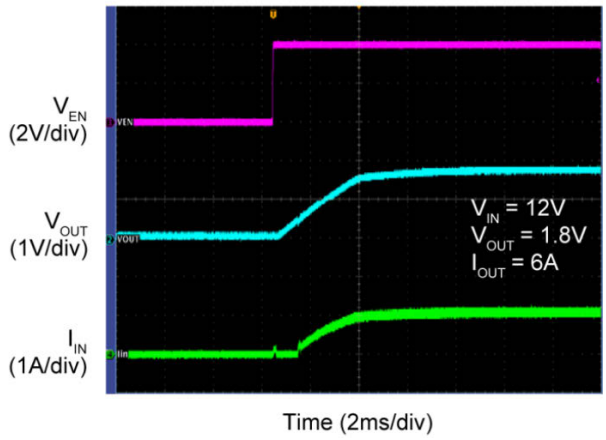
V_{IN} Soft Turn-On



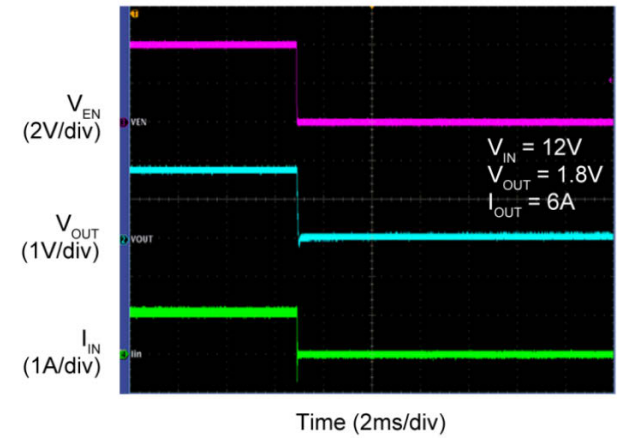
V_{IN} Soft Turn-Off



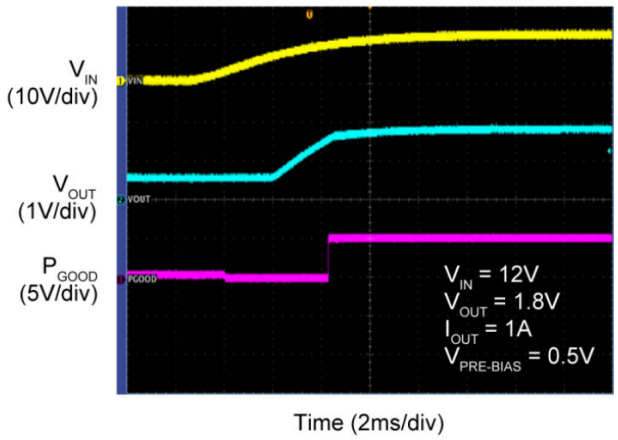
Enable Turn-On Delay and Rise Time



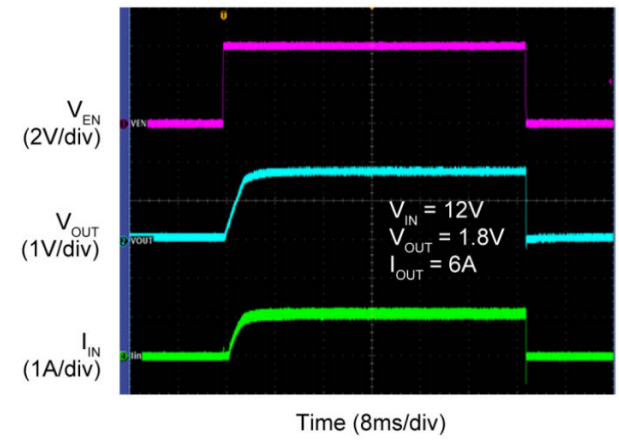
Enable Turn-Off Delay and Fall Time



V_{IN} Start-Up with Pre-Biased Output

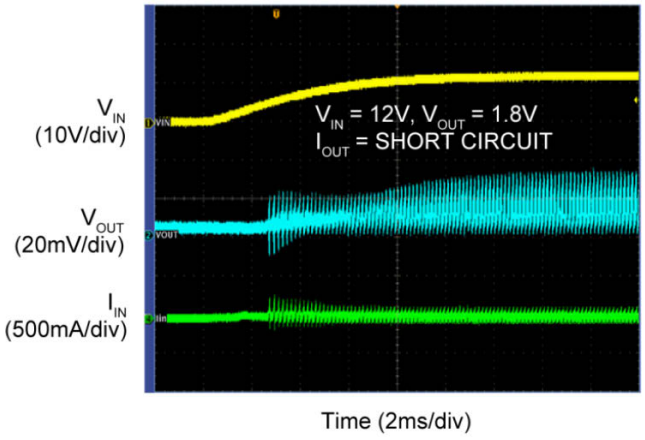


Enable Turn-On/Off

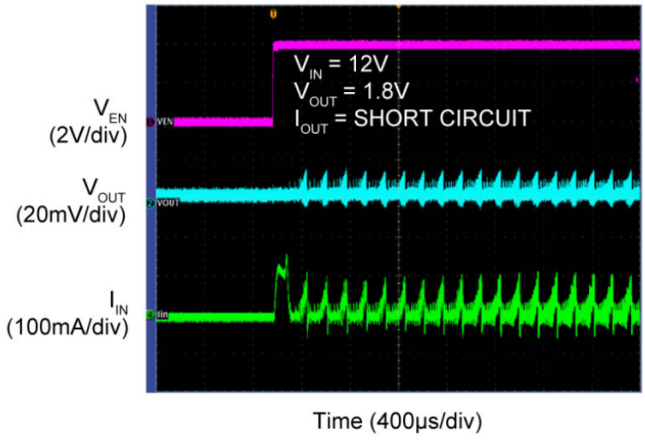


Functional Characteristics (Continued)

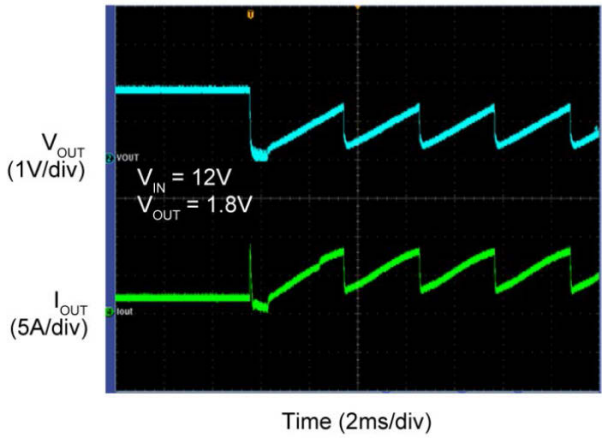
Power-Up into Short Circuit



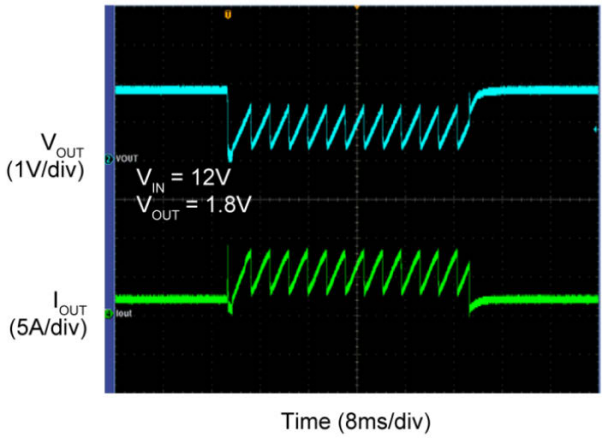
Enabled into Short



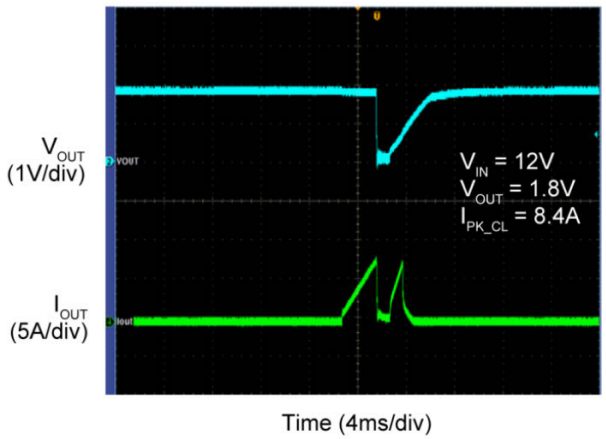
Short Circuit



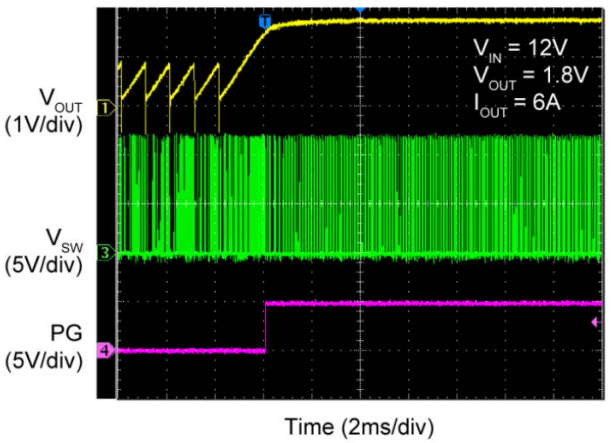
Output Recovery from Short Circuit



Peak Current-Limit Threshold

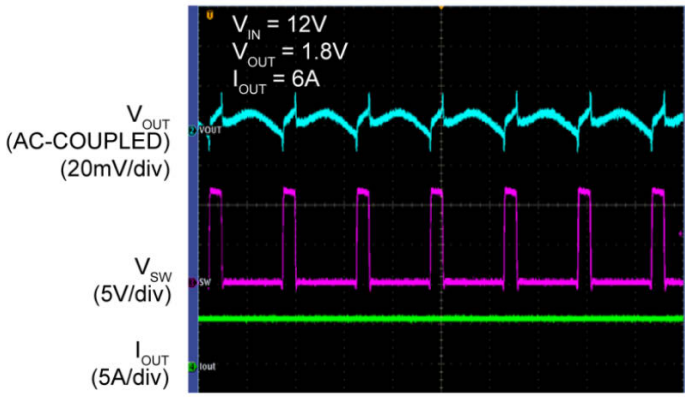


Output Recovery from Thermal Shutdown

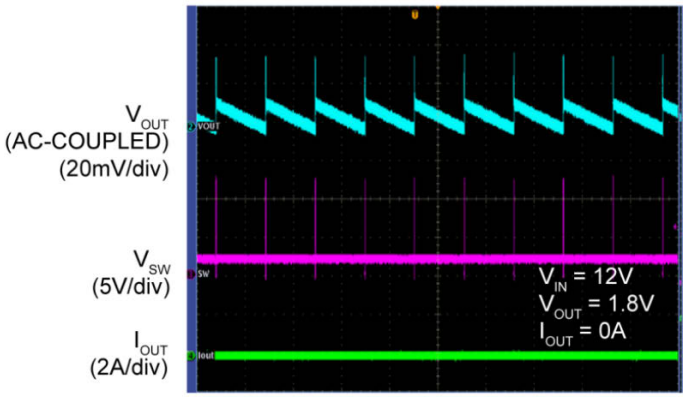


Functional Characteristics (Continued)

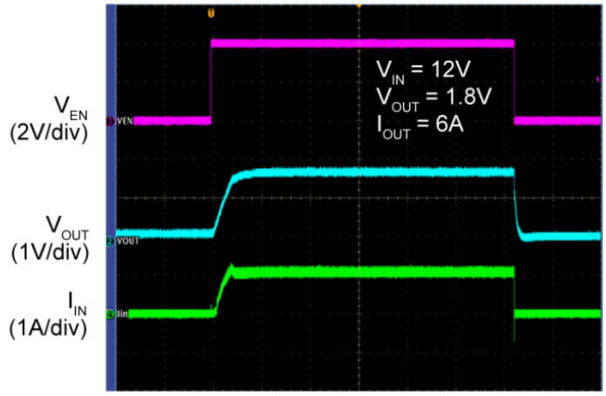
Switching Waveforms
(I_{OUT} = 6A)



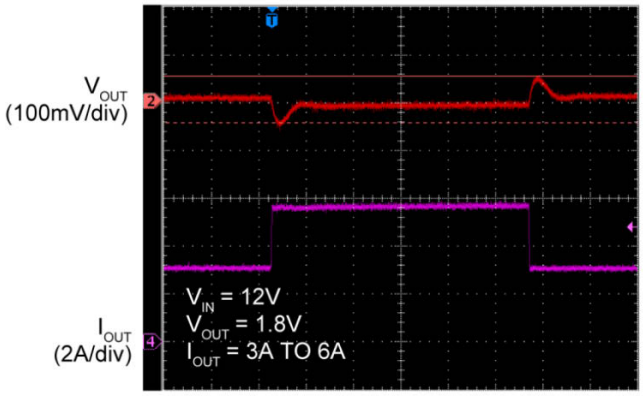
Switching Waveforms – MIC45205-1
(I_{OUT} = 0A)



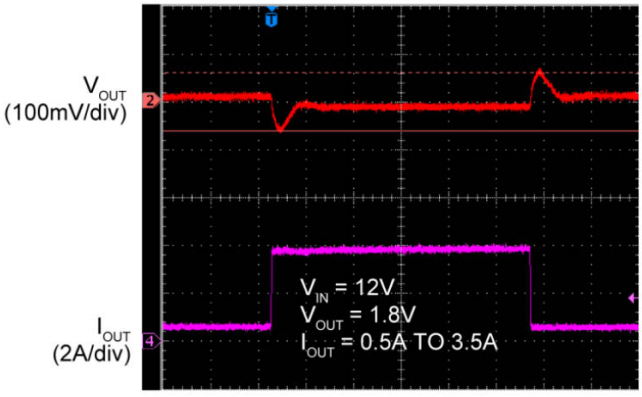
Inrush with C_{OUT} = 3000µF



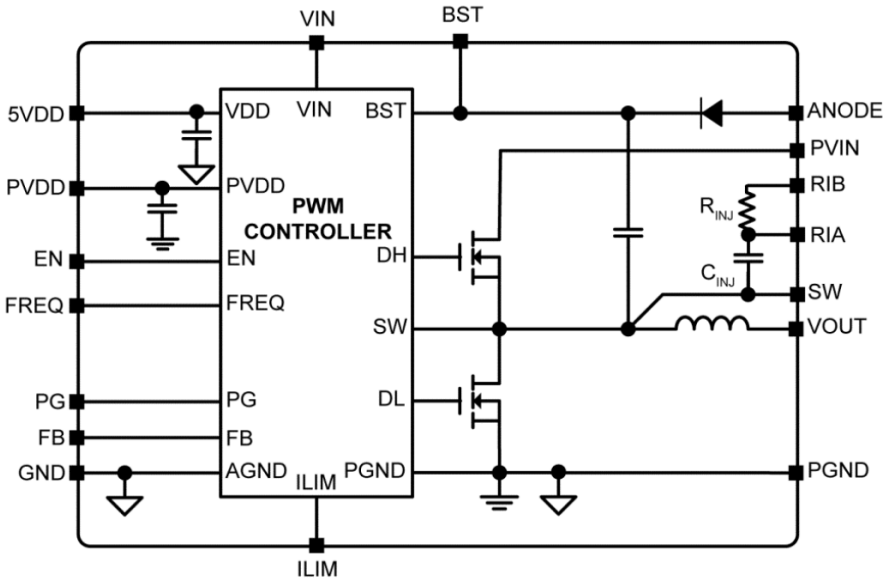
Transient Response – MIC45205-1
(I_{OUT} = 3A to 6A)



Transient Response – MIC45205-1
(I_{OUT} = 0.5A to 3.5A)



Functional Diagram



Functional Description

The MIC45205 is an adaptive on-time synchronous buck regulator module built for high-input voltage to low-output voltage conversion applications. The MIC45205 is designed to operate over a wide input voltage range, from 4.5V to 26V, and the output is adjustable with an external resistor divider. An adaptive on-time control scheme is employed to obtain a constant switching frequency in steady state and to simplify the control compensation. Hiccup mode over-current protection is implemented by sensing low-side MOSFET's $R_{DS(ON)}$. The device features internal soft-start, enable, UVLO, and thermal shutdown. The module has integrated switching FETs, inductor, bootstrap diode, resistor, and capacitor.

Theory of Operation

As shown in Figure 1 (in association with Equation 1), the output voltage is sensed by the MIC45205 feedback pin (FB) via the voltage divider R_{FB1} and R_{FB2} and compared to a 0.8V reference voltage (V_{REF}) at the error comparator through a low-gain transconductance (gm) amplifier. If the feedback voltage decreases, and the amplifier output falls below 0.8V, then the error comparator will trigger the control logic and generate an ON-time period. The ON-time period length is predetermined by the "Fixed t_{ON} Estimator" circuitry:

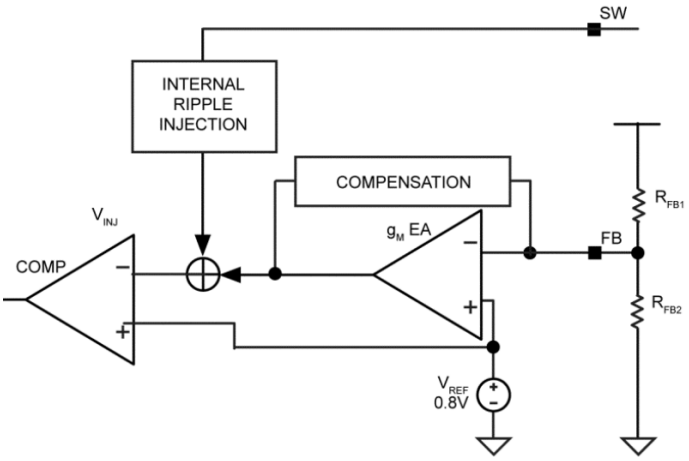


Figure 1. Output Voltage Sense via FB Pin

$$t_{ON(ESTIMATED)} = \frac{V_{OUT}}{V_{IN} \times f_{SW}} \qquad \text{Eq. 1}$$

where V_{OUT} is the output voltage, V_{IN} is the power stage input voltage, and f_{SW} is the switching frequency.

At the end of the ON-time period, the internal high-side driver turns off the high-side MOSFET and the low-side driver turns on the low-side MOSFET. The OFF-time period length depends upon the feedback voltage in most cases. When the feedback voltage decreases and the output of the g_m amplifier falls below 0.8V, the ON-time period is triggered and the OFF-time period ends. If the OFF-time period determined by the feedback voltage is less than the minimum OFF-time $t_{OFF(MIN)}$, which is about 200ns, the MIC45205 control logic will apply the $t_{OFF(MIN)}$ instead. $t_{OFF(MIN)}$ is required to maintain enough energy in the boost capacitor (C_{BST}) to drive the high-side MOSFET.

The maximum duty cycle is obtained from the 200ns $t_{OFF(MIN)}$:

$$D_{MAX} = \frac{t_S - t_{OFF(MIN)}}{t_S} = 1 - \frac{200ns}{t_S} \qquad \text{Eq. 2}$$

Where:

$t_S = 1/f_{SW}$. It is not recommended to use MIC45205 with an OFF-time close to $t_{OFF(MIN)}$ during steady-state operation.

The adaptive ON-time control scheme results in a constant switching frequency in the MIC45205 during steady state operation. The actual ON-time and resulting switching frequency will vary with the different rising and falling times of the MOSFETs. Also, the minimum t_{ON} results in a lower switching frequency in high V_{IN} to V_{OUT} applications. During load transients, the switching frequency is changed due to the varying OFF-time.

To illustrate the control loop operation, we will analyze both the steady-state and load transient scenarios. For easy analysis, the gain of the g_m amplifier is assumed to be 1. With this assumption, the inverting input of the error comparator is the same as the feedback voltage.

Figure 2 shows the MIC45205 control loop timing during steady-state operation. During steady-state, the g_m amplifier senses the feedback voltage ripple, which is proportional to the output voltage ripple plus injected voltage ripple, to trigger the ON-time period. The ON-time is predetermined by the t_{ON} estimator. The termination of the OFF-time is controlled by the feedback voltage. At the valley of the feedback voltage ripple, which occurs when V_{FB} falls below V_{REF}, the OFF period ends and the next ON-time period is triggered through the control logic circuitry.

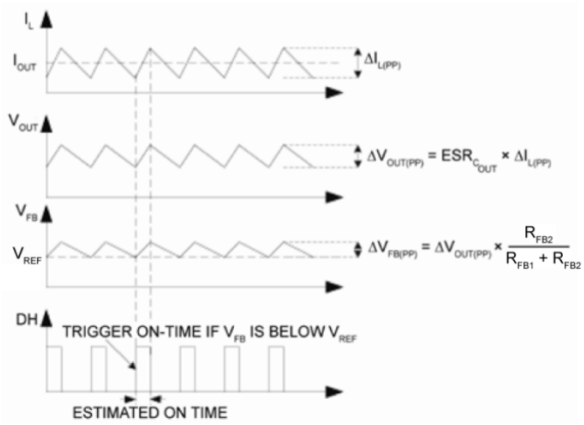


Figure 2. MIC45205 Control Loop Timing

Figure 3 shows the operation of the MIC45205 during a load transient. The output voltage drops due to the sudden load increase, which causes the V_{FB} to be less than V_{REF}. This will cause the error comparator to trigger an ON-time period. At the end of the ON-time period, a minimum OFF-time $t_{OFF(MIN)}$ is generated to charge the bootstrap capacitor (C_{BST}) since the feedback voltage is still below V_{REF}. Then, the next ON-time period is triggered due to the low feedback voltage. Therefore, the switching frequency changes during the load transient, but returns to the nominal fixed frequency once the output has stabilized at the new load current level. With the varying duty cycle and switching frequency, the output recovery time is fast and the output voltage deviation is small. Note that the instantaneous switching frequency during load transient remains bounded and cannot increase arbitrarily. The minimum is limited by t_{ON} + $t_{OFF(MIN)}$ .Since the variation in V_{OUT} is relatively limited during load transient, t_{ON} stays virtually close to its steady-state value.

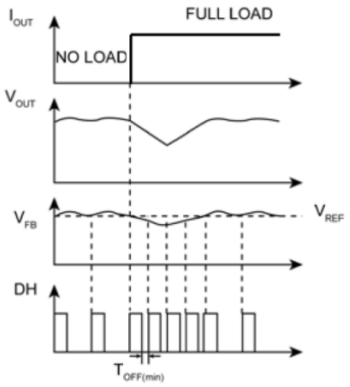


Figure 3. MIC45205 Load Transient Response

Unlike true current-mode control, the MIC45205 uses the output voltage ripple to trigger an ON-time period. The output voltage ripple is proportional to the inductor current ripple if the ESR of the output capacitor is large enough.

In order to meet the stability requirements, the MIC45205 feedback voltage ripple should be in phase with the inductor current ripple and are large enough to be sensed by the g_m amplifier and the error comparator. The recommended feedback voltage ripple is 20mV~100mV over full input voltage range. If a low ESR output capacitor is selected, then the feedback voltage ripple may be too small to be sensed by the g_m amplifier and the error comparator. Also, the output voltage ripple and the feedback voltage ripple are not necessarily in phase with the inductor current ripple if the ESR of the output capacitor is very low. In these cases, ripple injection is required to ensure proper operation. Please refer to "Ripple Injection" subsection in the *Application Information* section for more details about the ripple injection technique.

Discontinuous Mode (MIC45205-1 only)

In continuous mode, the inductor current is always greater than zero; however, at light loads, the MIC45205-1 is able to force the inductor current to operate in discontinuous mode. Discontinuous mode is where the inductor current falls to zero, as indicated by trace (I_L) shown in Figure 4. During this period, the efficiency is optimized by shutting down all the non-essential circuits and minimizing the supply current as the switching frequency is reduced. The MIC45205-1 wakes up and turns on the high-side MOSFET when the feedback voltage V_{FB} drops below 0.8V.

The MIC45205-1 has a zero crossing comparator (ZC) that monitors the inductor current by sensing the voltage drop across the low-side MOSFET during its ON-time. If the V_{FB} > 0.8V and the inductor current goes slightly negative, then the MIC45205-1 automatically powers down most of the IC circuitry and goes into a low-power mode.

Once the MIC45205-1 goes into discontinuous mode, both DL and DH are low, which turns off the high-side and low-side MOSFETs. The load current is supplied by the output capacitors and V_{OUT} drops. If the drop of V_{OUT} causes V_{FB} to go below V_{REF}, then all the circuits will wake up into normal continuous mode. First, the bias currents of most circuits reduced during the discontinuous mode are restored, and then a t_{ON} pulse is triggered before the drivers are turned on to avoid any possible glitches. Finally, the high-side driver is turned on. Figure 4 shows the control loop timing in discontinuous mode.

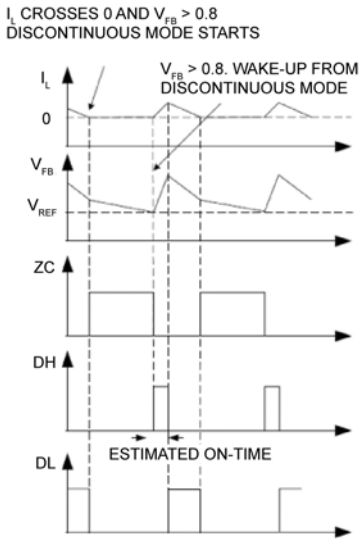


Figure 4. MIC45205-1 Control Loop Timing (Discontinuous Mode)

During discontinuous mode, the bias current of most circuits is substantially reduced. As a result, the total power supply current during discontinuous mode is only about 350µA, allowing the MIC45205-1 to achieve high efficiency in light load applications.

Soft-Start

Soft-start reduces the input power supply surge current at startup by controlling the output voltage rise time. The input surge appears while the output capacitor is charged up.

The MIC45205 implements an internal digital soft-start by making the 0.8V reference voltage V_{REF} ramp from 0 to 100% in about 5ms with 9.7mV steps. Therefore, the output voltage is controlled to increase slowly by a stair-case V_{FB} ramp. Once the soft-start cycle ends, the related circuitry is disabled to reduce current consumption. PVDD must be powered up at the same time or after V_{IN} to make the soft-start function correctly.

Current Limit

The MIC45205 uses the $R_{DS(ON)}$ of the low-side MOSFET and external resistor connected from ILIM pin to SW node to set the current limit.

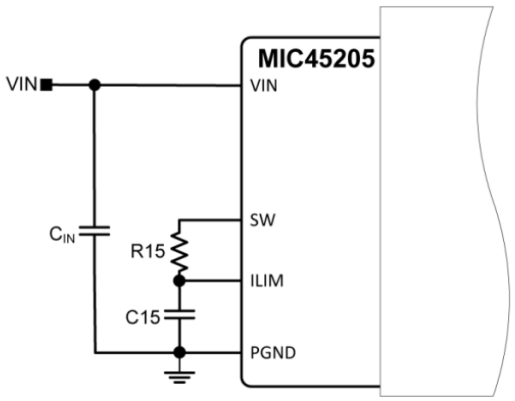


Figure 5. MIC45205 Current-Limiting Circuit

In each switching cycle of the MIC45205, the inductor current is sensed by monitoring the low-side MOSFET in the OFF period. The sensed voltage V_{ILIM} is compared with the power ground (PGND) after a blanking time of 150ns. In this way the drop voltage over the resistor R15 (V_{CL}) is compared with the drop over the bottom FET generating the short current limit. The small capacitor (C15) connected from ILIM pin to PGND filters the switching node ringing during the off-time allowing a better short-limit measurement. The time constant created by R15 and C6 should be much less than the minimum off time.

The V_{CL} drop allows programming of short limit through the value of the resistor (R15). If the absolute value of the voltage drop on the bottom FET becomes greater than $V_{CL,}$ and the V_{ILIM} falls below PGND, an overcurrent is triggered causing the IC to enter hiccup mode. The hiccup sequence including the soft-start reduces the stress on the switching FETs and protects the load and supply for severe short conditions.

The short-circuit current limit can be programmed by using Equation 3.

$$R15 = \frac{(I_{CLIM} - \Delta I_{L(PP)} \times 0.5) \times R_{DS(ON)} + V_{CL}}{I_{CL}} \quad \text{Eq. 3}$$

Where:

I_{CLIM} = Desired current limit

$R_{DS(ON)}$ = On-resistance of low-side power MOSFET, 16mΩ typically.

V_{CL} = Current-limit threshold (typical absolute value is 14mV per the *Electrical Characteristics* table*).*

I_{CL} = Current-limit source current (typical value is 70µA, per the *Electrical Characteristics* table).

$\Delta I_{L(PP)}$ = Inductor current peak-to-peak, since the inductor is integrated use Equation 4 to calculate the inductor ripple current.

The peak-to-peak inductor current ripple is:

$$\Delta I_{L(PP)} = \frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{V_{IN(max)} \times f_{sw} \times L} \quad \text{Eq. 4}$$

The MIC45205 has a 1.0µH inductor integrated into the module. In case of a hard short, the short limit is folded down to allow an indefinite hard short on the output without any destructive effect. It is mandatory to make sure that the inductor current used to charge the output capacitance during soft-start is under the folded short limit; otherwise the supply will go in hiccup mode and may not finish the soft-start successfully.

The MOSFET $R_{DS(ON)}$ varies 30% to 40% with temperature; therefore, it is recommended to add a 50% margin to I_{CLIM} in Equation 3 to avoid false current limiting due to increased MOSFET junction temperature rise.

With R15 = 1.37kΩ and C15 = 15pF, the typical output current limit is 8A.

Application Information

Setting the Switching Frequency

The MIC45205 switching frequency can be adjusted by changing the value of resistors R1 and R2.

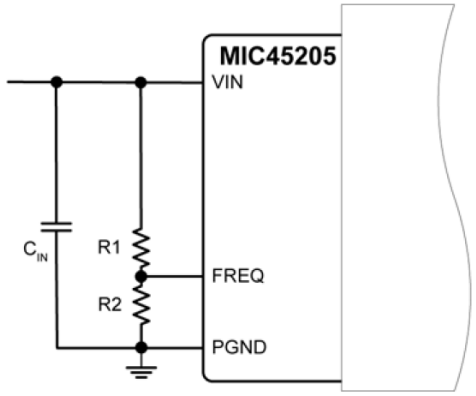


Figure 6. Switching Frequency Adjustment

Equation 5 gives the estimated switching frequency:

$$f_{SW} = f_O \times \frac{R2}{R1 + R2} \qquad \text{Eq. 5}$$

Where:

f_O = 600kHz (typical per the *Electrical Characteristics*[5] table)

R1= 100kΩ is recommended.

R2 needs to be selected in order to set the required switching frequency.

Switching Frequency

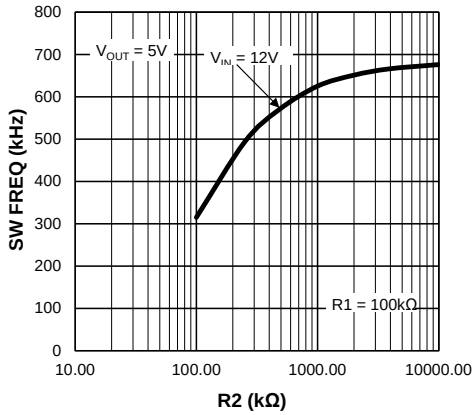


Figure 7. Switching Frequency vs. R2

The switching frequency also depends upon VIN, VOUT and load conditions as MIC45205 uses and adaptive ON-time architecture as explained in the "Theory of Operation" subsection in the *Functional Description*.

Output Capacitor Selection

The type of the output capacitor is usually determined by the application and its equivalent series resistance (ESR). Voltage and RMS current capability are two other important factors for selecting the output capacitor. Recommended capacitor types are MLCC, OS-CON and POSCAP. The output capacitor's ESR is usually the main cause of the output ripple. The MIC45205 requires ripple injection and the output capacitor ESR affects the control loop from a stability point of view.

The maximum value of ESR is calculated as in Equation 6:

$$ESR_{COUT} \le \frac{\Delta V_{OUT(PP)}}{\Delta I_{L(PP)}} \qquad \text{Eq. 6}$$

Where:

$\Delta V_{OUT(PP)}$ = Peak-to-peak output voltage ripple

$\Delta I_{L(PP)}$ = Peak-to-peak inductor current ripple

The total output ripple is a combination of the ESR and output capacitance. The total ripple is calculated in Equation 7:

$$\Delta V_{OUT(PP)} = \sqrt{\left(\frac{\Delta I_{L(PP)}}{C_{OUT} \times f_{SW} \times 8}\right)^2 + \left(\Delta I_{L(PP)} \times ESR_{C_{OUT}}\right)^2}$$

Eq. 7

Where:

D = Duty cycle

C_{OUT} = Output capacitance value

f_{sw} = Switching frequency

As described in the "Theory of Operation" subsection in the *Functional Description*, the MIC45205 requires at least 20mV peak-to-peak ripple at the FB pin to make the gm amplifier and the error comparator behave properly. Also, the output voltage ripple should be in phase with the inductor current. Therefore, the output voltage ripple caused by the output capacitors value should be much smaller than the ripple caused by the output capacitor ESR. If low-ESR capacitors, such as ceramic capacitors, are selected as the output capacitors, a ripple injection method should be applied to provide enough feedback voltage ripple. Please refer to "Ripple Injection" subsection in the *Application Information* section for more details.

The output capacitor RMS current is calculated in Equation 8:

$$I_{C_{OUT}(RMS)} = \frac{\Delta I_{L(PP)}}{\sqrt{12}}$$

Eq. 8

The power dissipated in the output capacitor is:

$$P_{DISS(C_{OUT})} = I_{C_{OUT}(RMS)}^2 \times ESR_{C_{OUT}}$$

Eq. 9

Input Capacitor Selection

The input capacitor for the power stage input PVIN should be selected for ripple current rating and voltage rating. The input voltage ripple will primarily depend on the input capacitor's ESR. The peak input current is equal to the peak inductor current, so:

$$\Delta V_{IN} = I_{L(pk)} \times ESR_{C_{IN}}$$

Eq. 10

The input capacitor must be rated for the input current ripple. The RMS value of input capacitor current is determined at the maximum output current. Assuming the peak-to-peak inductor current ripple is low:

$$I_{C_{IN(RMS)}} \approx I_{OUT(MAX)} \times \sqrt{D \times (1 - D)}$$

Eq.11

The power dissipated in the input capacitor is:

$$P_{DISS(CIN)} = I_{C_{IN(RMS)}}^2 \times ESR_{C_{IN}}$$

Eq. 12

The general rule is to pick the capacitor with a ripple current rating equal to or greater than the calculated worst-case RMS capacitor current.

Equation 13 should be used to calculate the input capacitor. Also it is recommended to keep some margin on the calculated value:

$$C_{IN} \approx \frac{I_{OUT(MAX)} \times (1 - D)}{f_{SW} \times dV}$$

Eq. 13

Where:

dV = The input ripple

f_{SW} = Switching frequency

Output Voltage Setting Components

The MIC45205 requires two resistors to set the output voltage as shown in Figure 8:

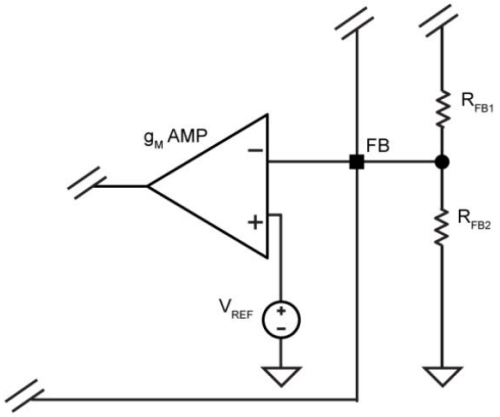


Figure 8. Voltage-Divider Configuration

The output voltage is determined by Equation 14:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right) \quad \text{Eq. 14}$$

Where:

V_{FB} = 0.8V

A typical value of R_{FB1} used on the standard evaluation board is 10kΩ. If R1 is too large, it may allow noise to be introduced into the voltage feedback loop. If R_{FB1} is too small in value, it will decrease the efficiency of the power supply, especially at light loads. Once R_{FB1} is selected, R_{FB2} can be calculated using Equation 15:

$$R_{FB2} = \frac{V_{FB} \times R_{FB1}}{V_{OUT} - V_{FB}} \quad \text{Eq. 15}$$

For fixed R_{FB1} = 10kΩ, output voltage can be selected by R_{FB2}. Table 1 provides R_{FB2} values for some common output voltages.

Table 1. V_{OUT} Programming Resistor Look-Up

R_{FB2}	V_{OUT}
OPEN	0.8V
40.2kΩ	1.0V
20kΩ	1.2V
11.5kΩ	1.5V
8.06kΩ	1.8V
4.75kΩ	2.5V
3.24kΩ	3.3V
1.91kΩ	5.0V

Ripple Injection

The V_{FB} ripple required for proper operation of the MIC45205 g_M amplifier and error comparator is 20mV to 100mV. However, the output voltage ripple is generally too small to provide enough ripple amplitude at the FB pin and this issue is more visible in lower output voltage applications. If the feedback voltage ripple is so small that the g_M amplifier and error comparator cannot sense it, then the MIC45205 will lose control and the output voltage is not regulated. In order to have some amount of V_{FB} ripple, a ripple injection method is applied for low output voltage ripple applications.

The applications are divided into two situations according to the amount of the feedback voltage ripple:

1. Enough ripple at the feedback voltage due to the large ESR of the output capacitors:

   As shown in Figure 9, the converter is stable without any ripple injection.

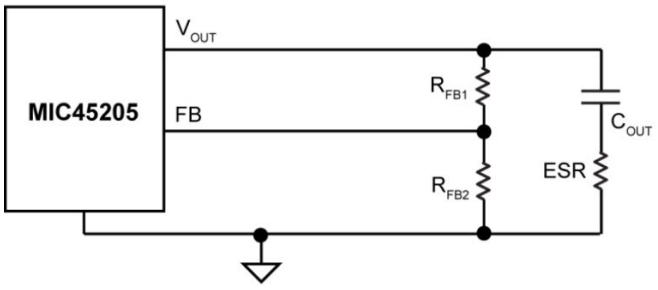


Figure 9. Enough Ripple at FB from ESR

The feedback voltage ripple is:

$$\Delta V_{FB(PP)} = \frac{R_{FB2}}{R_{FB1} + R_{FB2}} \times ESR_{C_{OUT}} \times \Delta I_{L(PP)}$$

Eq. 16

Where:

$\Delta I_{L(PP)}$ = The peak-to-peak value of the inductor current ripple

2. Virtually no or inadequate ripple at the FB pin voltage due to the very-low ESR of the output capacitors, such is the case with ceramic output capacitor. In this case, the V_{FB} ripple waveform needs to be generated by injecting suitable signal. MIC45205 has provisions to enable an internal series RC injection network, R_{INJ} and C_{INJ} as shown in Figure 10 by connecting RIB to FB pin. This network injects a square-wave current waveform into FB pin, which by means of integration across the capacitor (C14) generates an appropriate sawtooth FB ripple waveform.

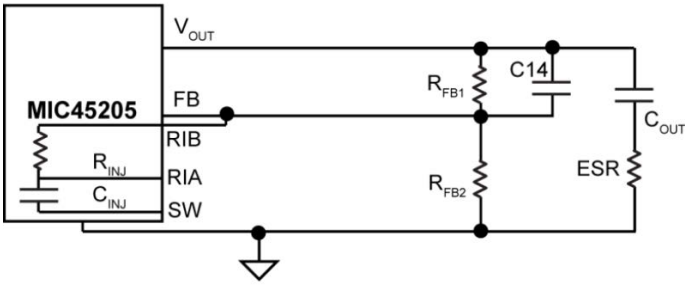


Figure 10. Internal Ripple Injection at FB via RIB Pin

The injected ripple is:

$$\Delta V_{FB(PP)} = V_{IN} \times K_{div} \times D \times (1 - D) \times \frac{1}{f_{SW} \times \tau}$$

Eq.17

$$K_{div} = \frac{R_{FB1} // R_{FB2}}{R_{INJ} + R_{FB1} // R_{FB2}}$$

Eq.18

Where:

V_{IN} = Power stage input voltage

D = Duty cycle

f_{SW} = Switching frequency

$\tau = (R_{FB1} // R_{FB2} // R_{INJ}) \times C14$

R_{INJ}= 10kΩ

C_{INJ} = 0.1µF

In Equations 18 and 19, it is assumed that the time constant associated with C14 must be much greater than the switching period:

$$\frac{1}{f_{SW} \times \tau} = \frac{T}{\tau} << 1$$

Eq. 19

If the voltage divider resistors R_{FB1} and R_{FB2} are in the kΩ range, then a C14 of 1nF to 100nF can easily satisfy the large time constant requirements.

Thermal Measurements and Safe Operating Area (SOA)

Measuring the IC's case temperature is recommended to ensure it is within its operating limits. Although this might seem like a very elementary task, it is easy to get erroneous results. The most common mistake is to use the standard thermal couple that comes with a thermal meter. This thermal couple wire gauge is large, typically 22 gauge, and behaves like a heatsink, resulting in a lower case measurement.

Two methods of temperature measurement are using a smaller thermal couple wire or an infrared thermometer. If a thermal couple wire is used, it must be constructed of 36-gauge wire or higher (smaller wire size) to minimize the wire heat-sinking effect. In addition, the thermal couple tip must be covered in either thermal grease or thermal glue to make sure that the thermal couple junction is making good contact with the case of the IC. Omega brand thermal couple (5SC-TT-K-36-36) is adequate for most applications.

Wherever possible, an infrared thermometer is recommended. The measurement spot size of most infrared thermometers is too large for an accurate reading on a small form factor ICs. However, an IR thermometer from Optris has a 1mm spot size, which makes it a good choice for measuring the hottest point on the case. An optional stand makes it easy to hold the beam on the IC for long periods of time.

The safe operating area (SOA) of the MIC45205 is shown in Figure 11, Figure 12, Figure 13, Figure 14, and Figure 15. These thermal measurements were taken on MIC45205 evaluation board. Since the MIC45205 is an entire system comprised of switching regulator controller, MOSFETs and inductor, the part needs to be considered as a system. The SOA curves will give guidance to reasonable use of the MIC45205.

SOA curves should only be used as a point of reference. SOA data was acquired using the MIC45205 evaluation board. Thermal performance depends on the PCB layout, board size, copper thickness, number of thermal vias, and actual airflow.

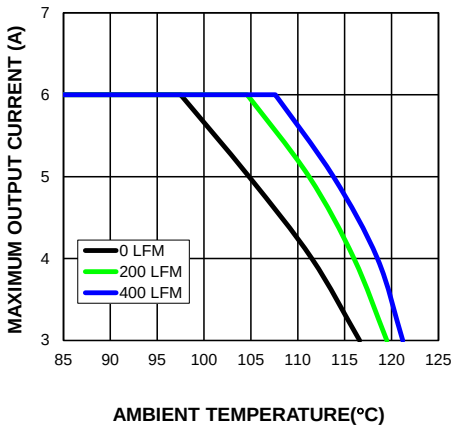


Figure 11. MIC45205 Power Derating vs. Airflow ($5V_{IN}$ to $1.5V_{OUT}$)

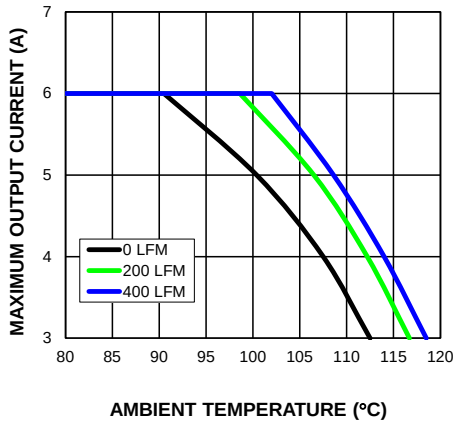


Figure 12. MIC45205 Power Derating vs. Airflow ($12V_{IN}$ to $1.5V_{OUT}$)

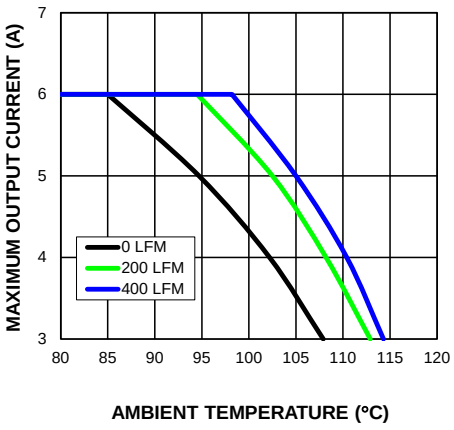


Figure 13. MIC45205 Power Derating vs. Airflow ($12V_{IN}$ to $3.3V_{OUT}$)

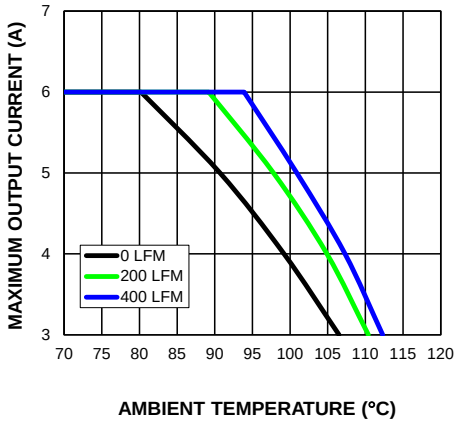


Figure 14. MIC45205 Power Derating vs. Airflow ($24V_{IN}$ to $1.5V_{OUT}$)

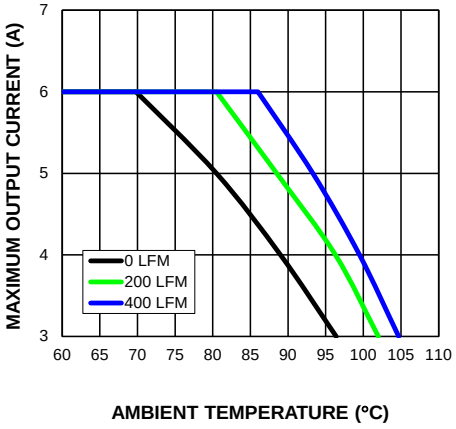


Figure 15. MIC45205 Power Derating vs. Airflow ($24V_{IN}$ to $3.3V_{OUT}$)

PCB Layout Guidelines

Warning: To minimize EMI and output noise, follow these layout recommendations.

PCB layout is critical to achieve reliable, stable and efficient performance. A ground plane is required to control EMI and minimize the inductance in power, signal and return paths.

Figure 16 is optimized from a small form factor point of view shows top and bottom layer of a four layer PCB. It is recommended to use mid layer 1 as a continuous ground plane.

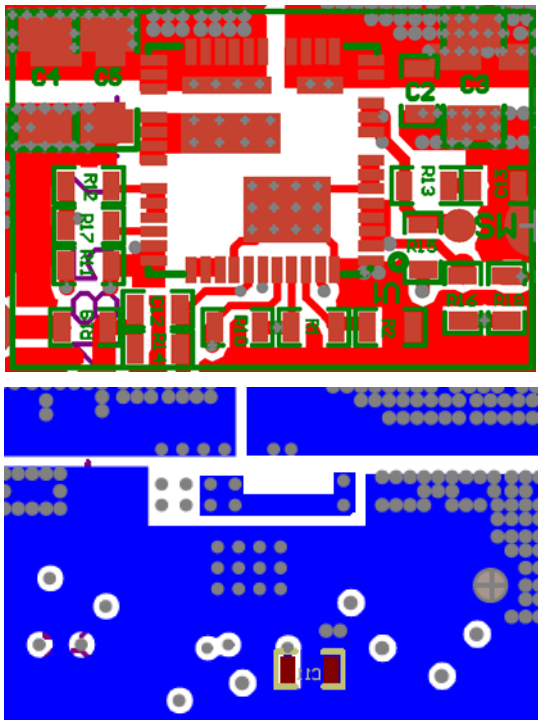


Figure 16. Top And Bottom Layer of a Four-Layer Board

The following guidelines should be followed to insure proper operation of the MIC45205 module:

IC

- The analog ground pin (GND) must be connected directly to the ground planes. Place the IC close to the point-of-load (POL).
- Use thick traces to route the input and output power lines.
- Analog and power grounds should be kept separate and connected at only one location with a low impedance.

Input Capacitor

- Place the input capacitors on the same side of the board and as close to the IC as possible.
- Place several vias to the ground plane close to the input capacitor ground terminal.
- Use either X7R or X5R dielectric input capacitors. Do not use Y5V or Z5U type capacitors.
- Do not replace the ceramic input capacitor with any other type of capacitor. Any type of capacitor can be placed in parallel with the ceramic input capacitor.
- If a non-ceramic input capacitor is placed in parallel with the input capacitor, it must be recommended for switching regulator applications and the operating voltage.
- In “Hot-Plug” applications, an Electrolytic bypass capacitor must be used to limit the over-voltage spike seen on the input supply with power is suddenly applied. If hot-plugging is the normal operation of the system, using an appropriate hot-swap IC is recommended.

RC Snubber (Optional)

- Depending on the operating conditions, a RC snubber on the same side of the board can be used. Place the RC and as close to the SW pin as possible if needed.

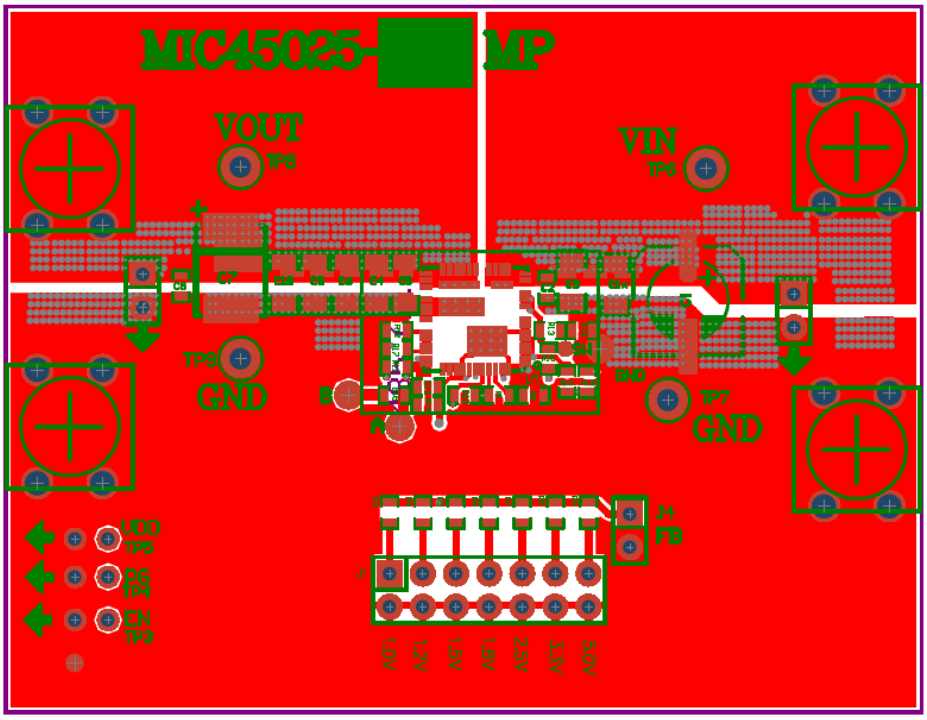
SW Node

- Do not route any digital lines underneath or close to the SW node.
- Keep the switch node (SW) away from the feedback (FB) pin.

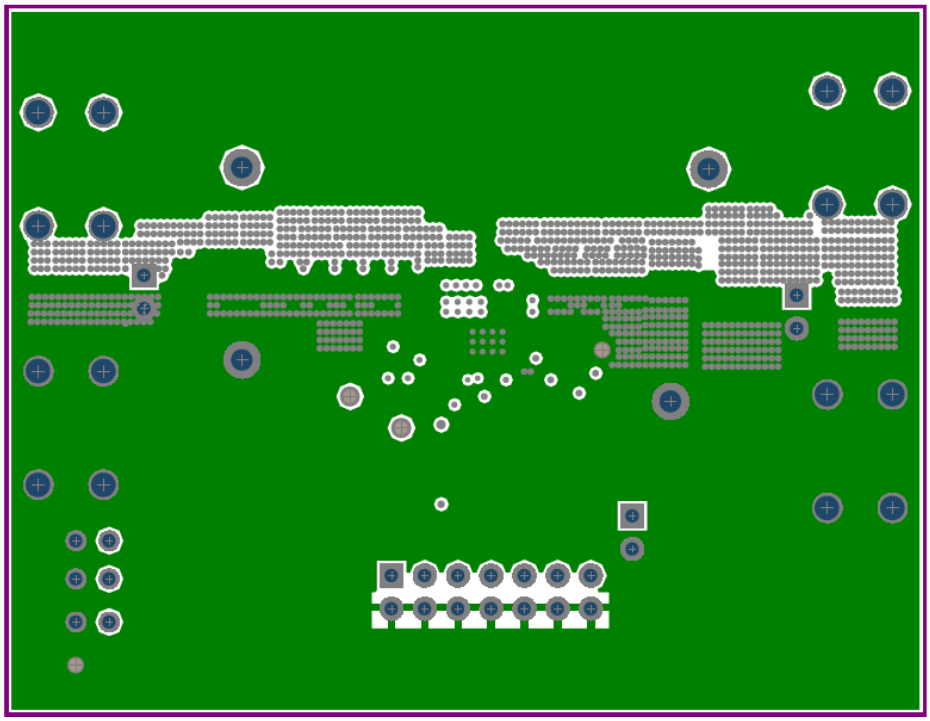
Output Capacitor

- Use a wide trace to connect the output capacitor ground terminal to the input capacitor ground terminal.
- Phase margin will change as the output capacitor value and ESR changes.
- The feedback trace should be separate from the power trace and connected as close as possible to the output capacitor. Sensing a long high-current load trace can degrade the DC load regulation.

PCB Layout Recommendations

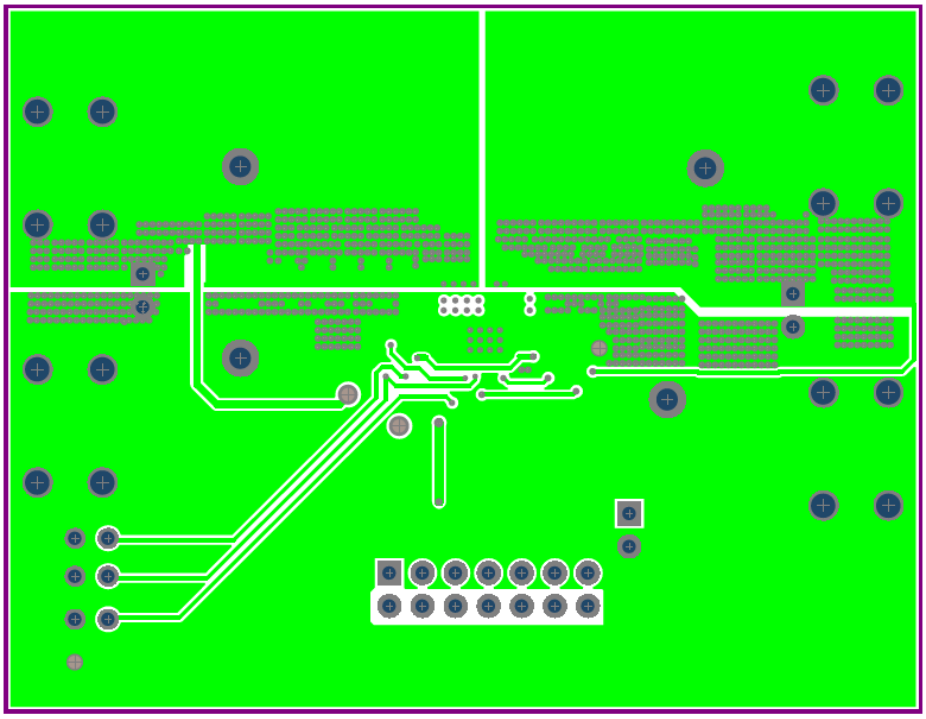


Top – Copper Layer 1

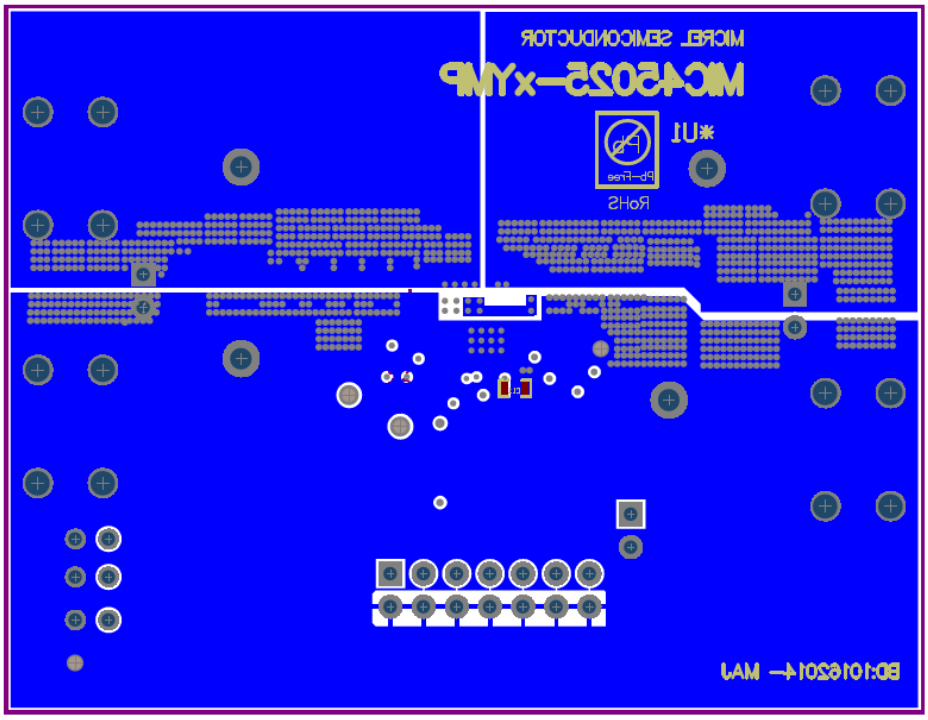


Copper Layer 2

PCB Layout Recommendations (Continued)



Copper Layer 3



Bottom – Copper Layer 4

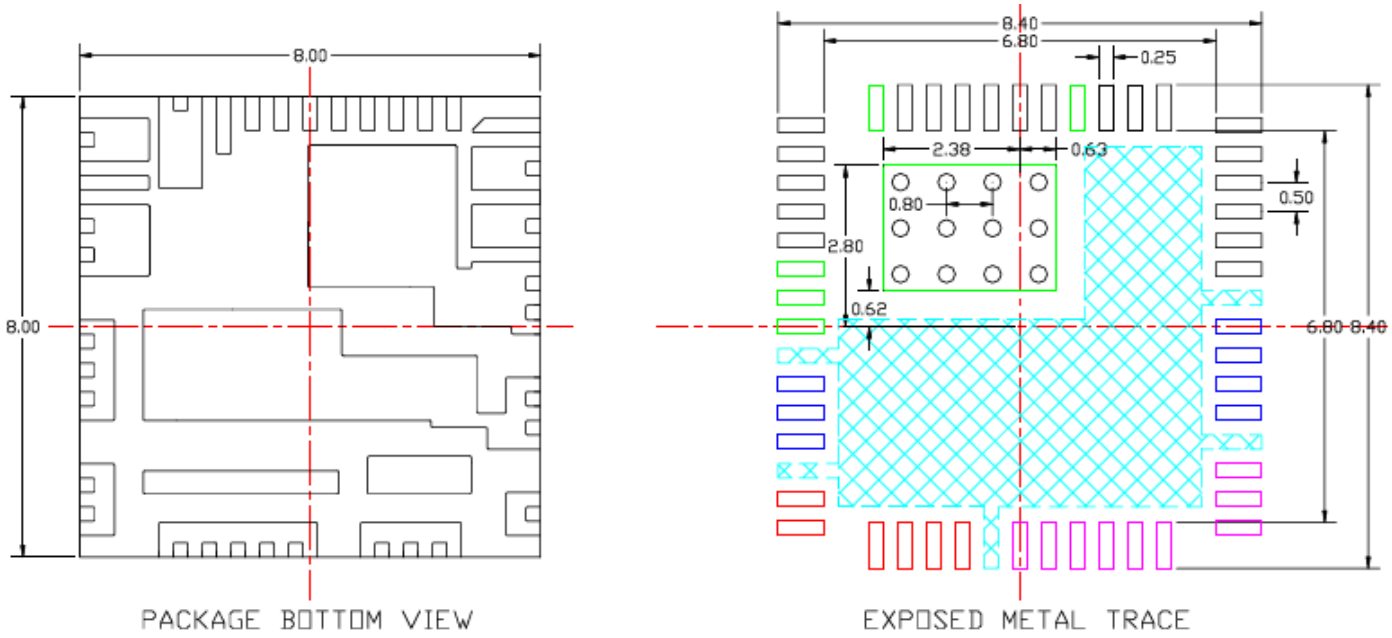
Simplified PCB Design Recommendations

Periphery I/O Pad Layout and Large Pad for Exposed Heatsink

The board design should begin with copper/metal pads that sit beneath the periphery leads of a mounted QFN. The board pads should extend outside the QFN package edge a distance of approximately 0.20mm per side:

Total pad length = 8.00mm + (0.20mm per side × 2 sides) = 8.40mm

After completion of the periphery pad design, the larger exposed pads will be designed to create the mounting surface of the QFN exposed heatsink. The primary transfer of heat out of the QFN will be directly through the bottom surface of the exposed heatsink. To aid in the transfer of generated heat into the PCB, the use of an array of plated through-hole vias beneath the mounted part is recommended. The typical via hole diameter is 0.30mm to 0.35mm, with center-to-center pitch of 0.80mm to 1.20mm.



Note:

Exposed metal trace is “mirror image” of package bottom view.

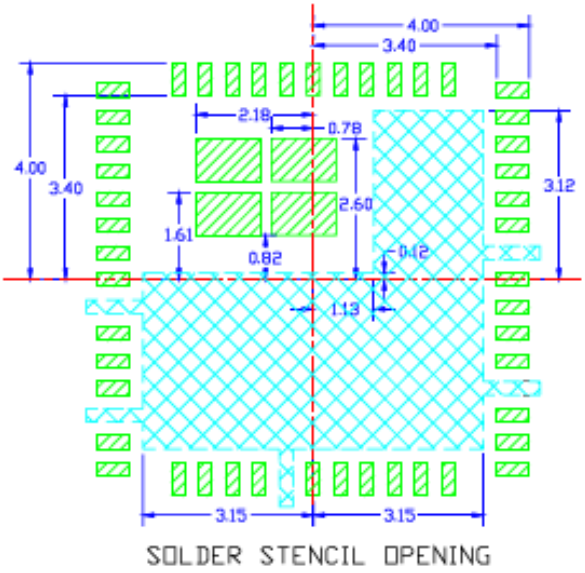
Figure 17. Package Bottom View vs. PCB Recommended Exposed Metal Trace

Solder Paste Stencil Design (Recommend Stencil Thickness = 112.5 ±12.5µm)

The solder stencil aperture openings should be smaller than the periphery or large PCB exposed pads to reduce any chance of build-up of excess solder at the large exposed pad area which can result to solder bridging.

The suggested reduction of the stencil aperture opening is typically 0.20mm smaller than exposed metal trace.

Note: A critical requirement is to *not* duplicate land pattern of the exposed metal trace as solder stencil opening as the design and dimension values are different.



Note:

Cyan-colored shaded pad indicate exposed trace keep out area.

Figure 18. Solder Stencil Opening

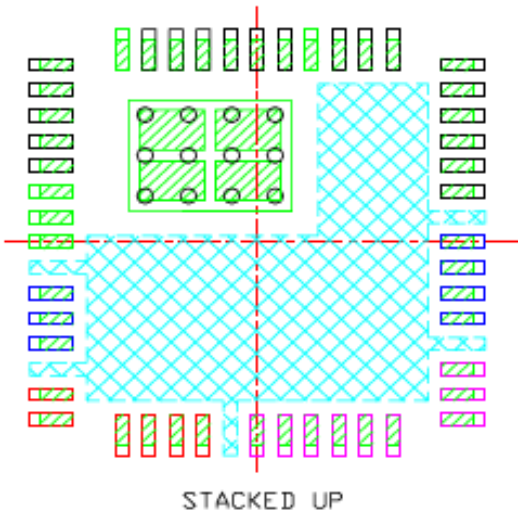
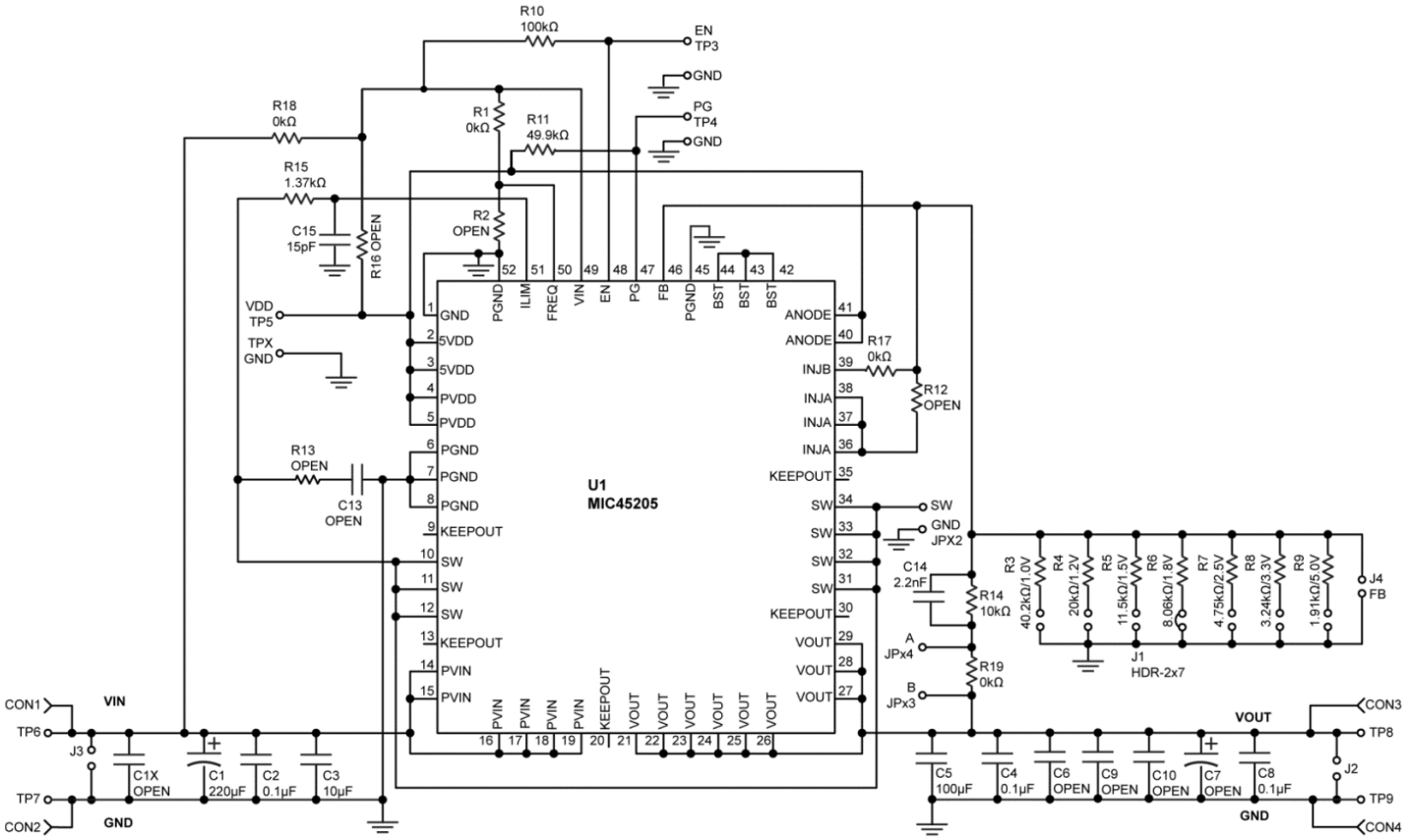


Figure 19. Stack-Up of Pad Layout and Solder Paste Stencil

Evaluation Board Schematic



Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C1	EEE-FK1V221P	Panasonic[6]	220µF/35V, ALE Capacitor (optional)	1
C1X, C6, C9, C10, C7, C13			Open	6
C3	C3216X5R1H106M160AB	TDK[7]	10uF/50V, 1206, X5R, 10%, MLCC	1
C2, C4, C8	GRM188R71H104KA93D	Murata[8]	0.1µF/50V, X7R, 0603, 10%, MLCC	3
C5	C3216X5R0J107M160AB	TDK	100µF/6.3V, X5R, 1206, 20%, MLCC	1
C12	C1608C0G1H222JT	TDK	2.2nF/50V, NP0, 0603, 5%, MLCC	1
C11	GRM1885C1H150JA01D	Murata	15pF/50V, NP0, 0603, 5%, MLCC	3
CON1, CON2, CON3, CON4	8174	Keystone[9]	15A, 4-Prong Through-Hole Screw Terminal	4

Notes:

6. Panasonic: www.panasonic.com.
7. TDK: www.TDK.com.
8. Murata: www.murata.com.
9. Keystone: www.keyelco.com.

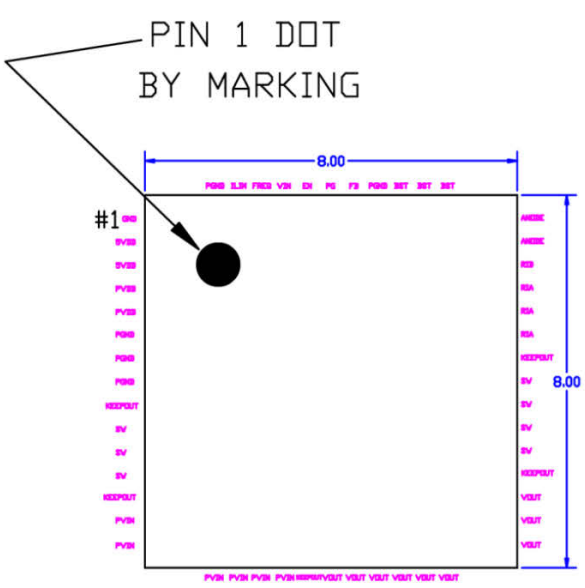
Bill of Materials (Continued)

Item	Part Number	Manufacturer	Description	Qty.
J1	M50-3500742	Harwin[10]	Header 2x7	1
J2, J3, J4, TP3 – TP5	90120-0122	Molex[11]	Header 2	6
JPx1, JPx2			Open	2
R1, R10	CRCW0603100K0FKEA	Vishay Dale[12]	100kΩ, 1%, 1/10W, 0603, Thick Film	2
R2, R12, R13, R16			Open	4
R3	CRCW060340K2FKEA	Vishay Dale	40.2kΩ, 1%, 1/10W, 0603, Thick Film	1
R4	CRCW06020K0FKEA	Vishay Dale	20kΩ, 1%, 1/10W, 0603, Thick Film	1
R5	CRCW060311K5FKEA	Vishay Dale	11.5kΩ, 1%, 1/10W, 0603, Thick Film	1
R6	CRCW06038K06FKEA	Vishay Dale	8.06kΩ, 1%, 1/10W, 0603, Thick Film	1
R7	CRCW06034K75FKEA	Vishay Dale	4.75kΩ, 1%, 1/10W, 0603, Thick Film	1
R8	CRCW06033K24FKEA	Vishay Dale	3.24kΩ, 1%, 1/10W, 0603, Thick Film	1
R9	CRCW06031K91FKEA	Vishay Dale	1.91kΩ, 1%, 1/10W, 0603, Thick Film	1
R11	CRCW060349K9FKEA	Vishay Dale	49.9kΩ, 1%, 1/10W, 0603, Thick Film	1
R14	CRCW060310K0FKEA	Vishay Dale	10kΩ, 1%, 1/10W, 0603, Thick Film	1
R15	CRCW06031K37FKEA	Vishay Dale	1.37kΩ, 1%, 1/10W, 0603, Thick Film	1
R17, R18, R19	RCG06030000Z0EA	Vishay Dale	0Ω Resistor, 1%, 1/10W, 0603, Thick Film	3
TP6 – TP9, JPx3, JPx4	1502-2	Keystone	Single-End, Through-Hole Terminal	6
U1	**MIC45205-1YMP**	**Micrel, Inc.[13]**	**26V/6A DC-to-DC Power Module**	**1**
	MIC45205-2YMP			

Notes:

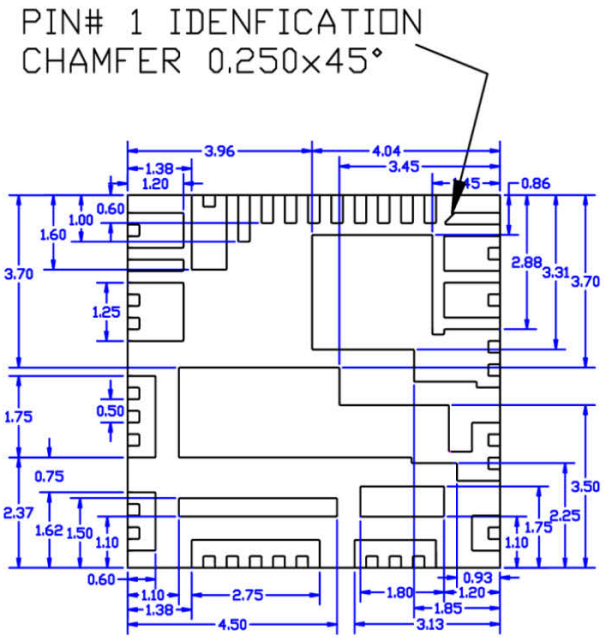
10. Harwin: http://www.harwin.com
11. Molex: www.molex.com.
12. Vishay-Dale: www.vishay.com.
13. **Micrel: www.micrel.com.**

Package Information and Recommended Landing Pattern[14]



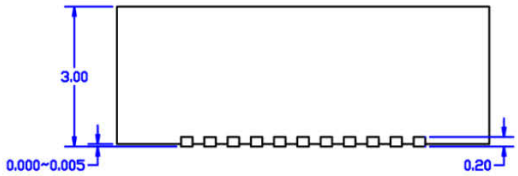
Top View

NOTE: 1, 2, 3



Bottom View

NOTE: 1, 2, 3



Side View

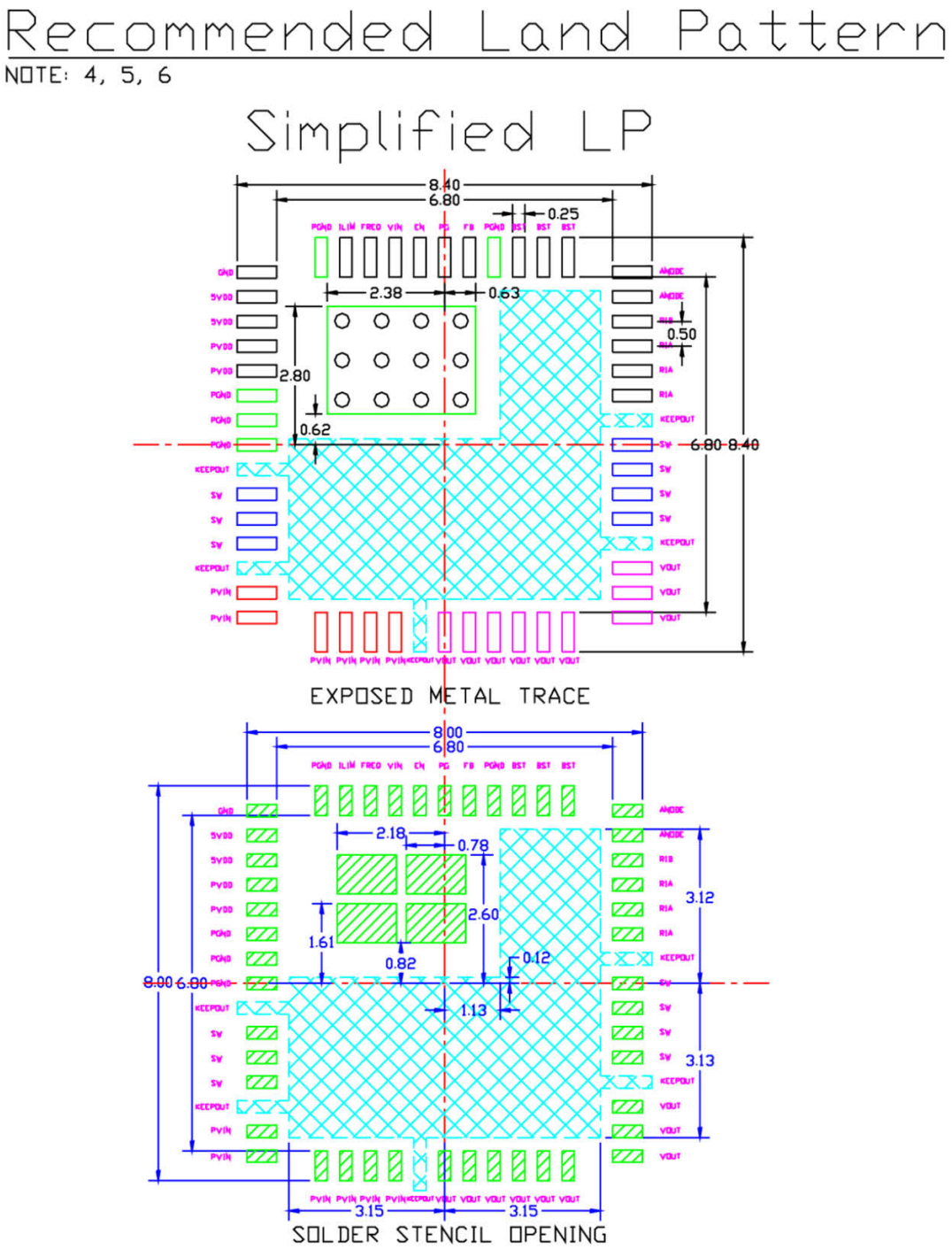
NOTE: 1, 2, 3

52-Pin 8mm × 8mm QFN (MP)

Note:

14. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

Package Information and Recommended Landing Pattern[14] (Continued)

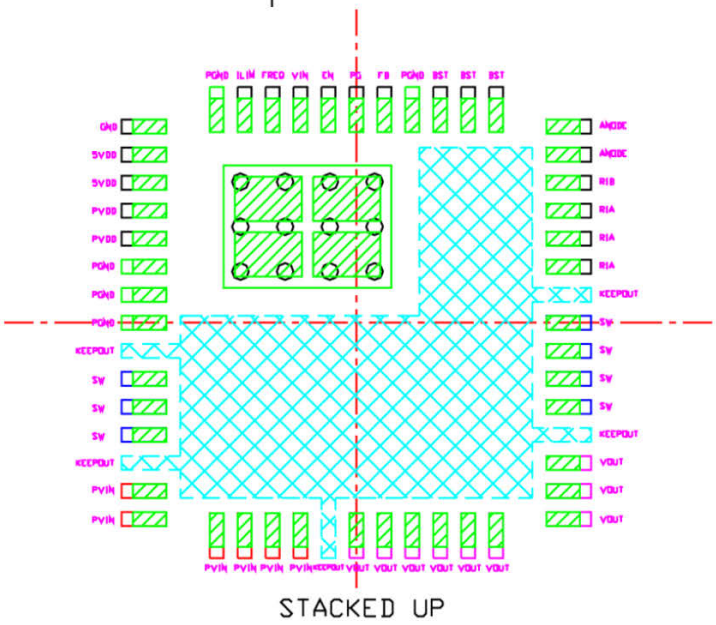


Package Information and Recommended Landing Pattern[14] (Continued)

Recommended Land Pattern

NOTE: 4, 5, 6

Simplified LP

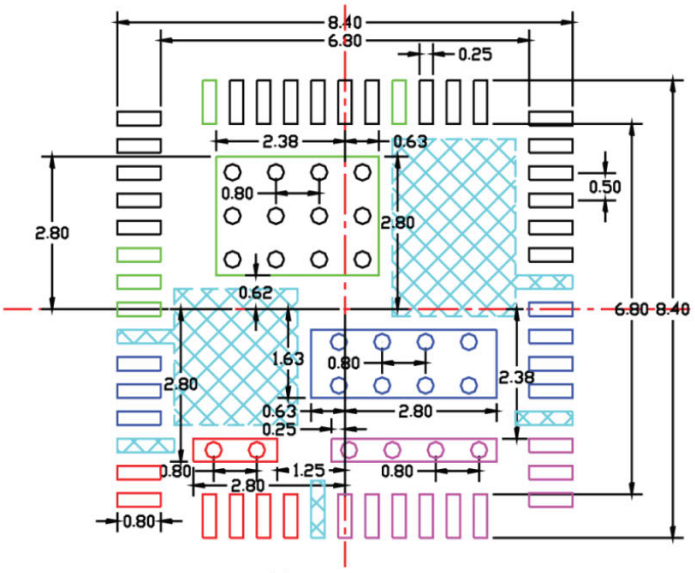


STACKED UP

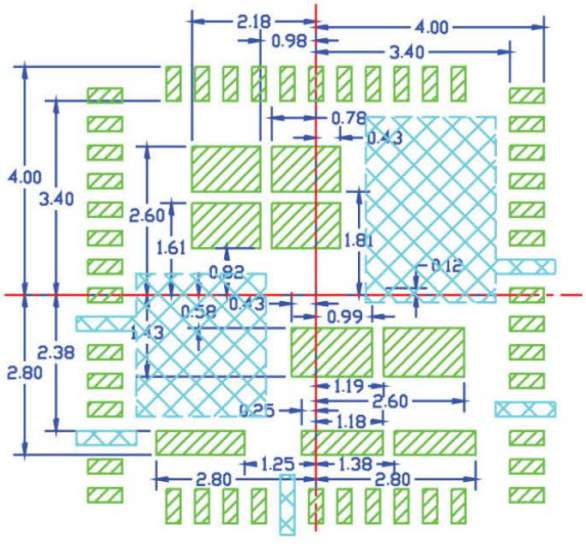
NOTE:

1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. BLACK CIRCLES IN LAND PATTERN REPRESENT THERMAL VIA, RECOMMENDED SIZE IS 0.30-0.35mm, AT 0.80mm PITCH & SHOULD BE CONNECTED TO GND FOR MAXIMUM PERFORMANCE.
5. GREEN RECTANGLES (SHADED AREA) REPRESENT SOLDER STENCIL OPENING ON EXPOSED PAD AREA.
6. CYAN COLORED SHADED PAD REPRESENT EXPOSED TRACE KEEP OUT AREA.

Thermally-Enhanced Landing Pattern

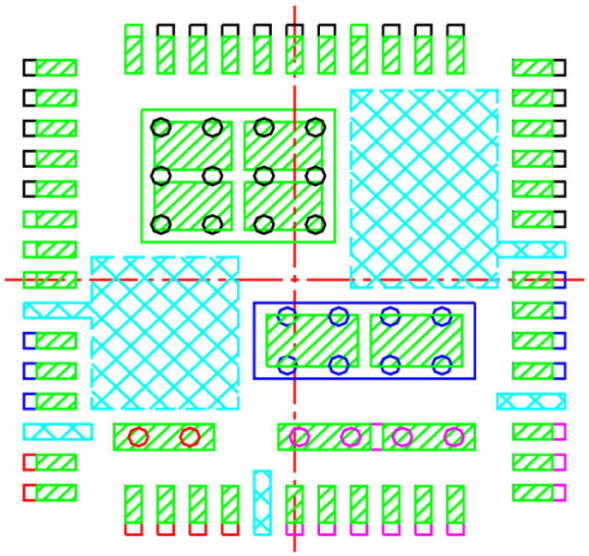


EXPOSED METAL TRACE



SOLDER STENCIL OPENING

Thermally-Enhanced Landing Pattern (Continued)



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MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA

TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http://www.micrel.com

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