MIC5002CN/5005CN/5007CN

4-Digit Counter/Display Decoder

T-67-31-51

General Description

The MIC5002/5/7 is an ion-implanted, P-channel MOS, four-decade synchronous counter with latches, multiplexing circuits, and a read-only memory programmed for seven-segment outputs and BCD outputs. In addition, many on-chip control circuits provide flexibility of use with a minimum of external components.

The MIC5002/5/7 provides a means of counting up to 9999, transferring the count into latches without interrupting the counting operation, and supplying the latched information to the outputs one decade at a time. Scanning is controlled by the SCAN input which increments a one-of-four counter on its negative edge, thereby scanning the latches from MSD (Most Significant Digit) to LSD (Least Significant Digit).

Low-threshold voltages for input DTL/TTL compatibility are achieved through an ion-implementation process. Enhancement mode devices, as well as depletion-mode devices, are fabricated on the chip, allowing it to operate from a single +5V power supply. Depletion-mode technology also allows the entire circuit to operate on less than 25mW of power.

The block diagram, Figure 1, shows all options available on the MIC5002 MOS/LSI. Other members of this family which

Features

- Single-supply operation or double-supply for higher output drive
- Multiplexed seven-segment and/or BCD outputs
- TTL-compatible inputs
- Four decades of synchronous counting
- Minimum external component count
- Low power consumption

Ordering Information

Part Number	Temperature Range	Package
MIC5002CN	0°C to +70°C	28-Pin Plastic DIP
MIC5005CN	0°C to +70°C	24-Pin Plastic DIP
MIC5007CN	0°C to +70°C	16-Pin Plastic DIP

Functional Diagram

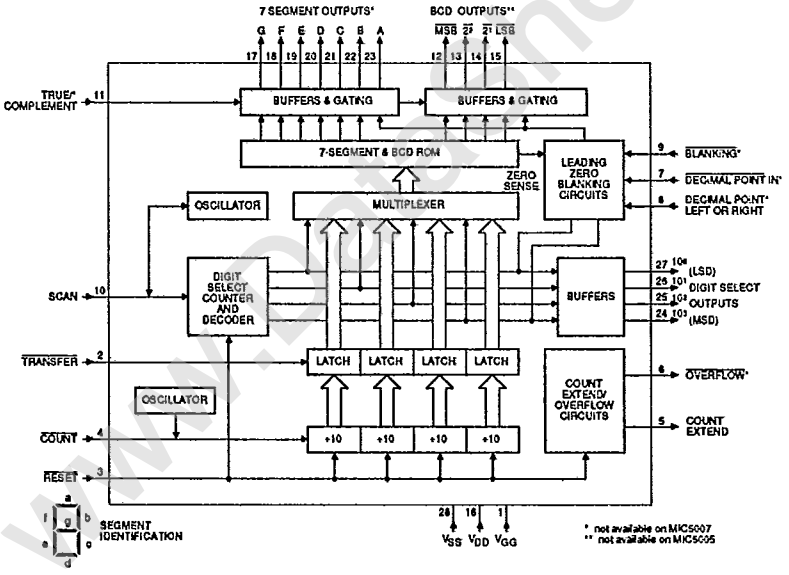

Figure 1

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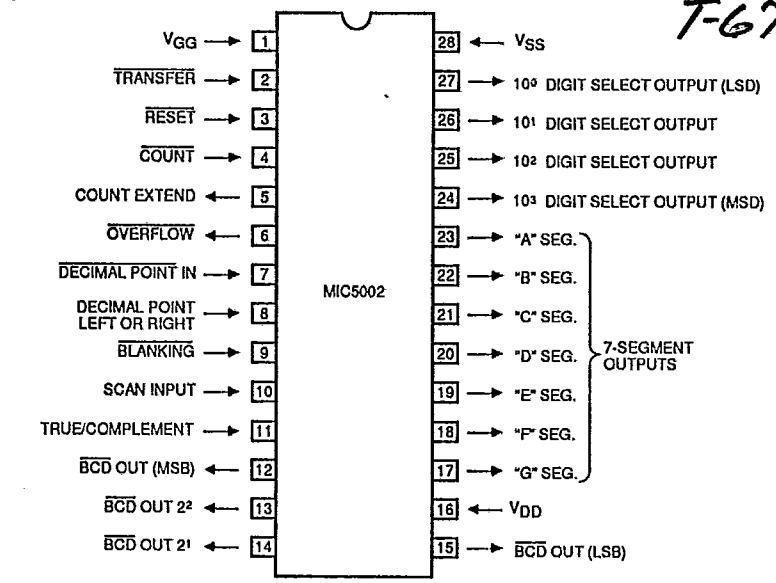
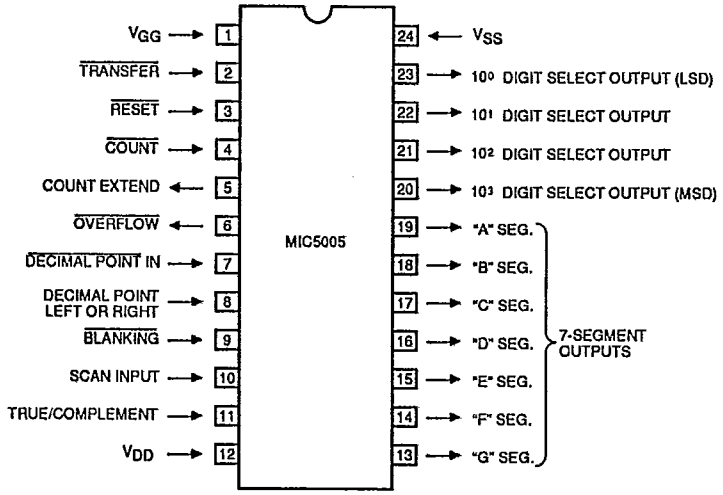
Pin Configurations





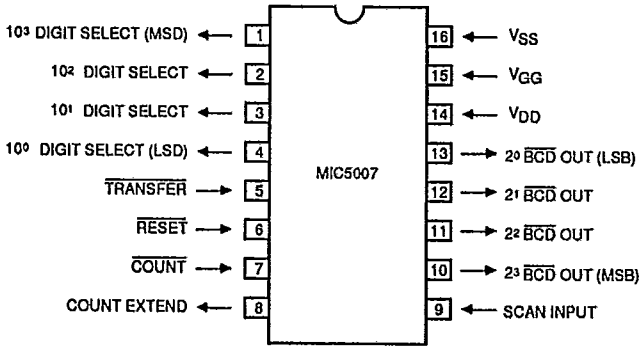


Figure 2

are different versions of this same chip are the MIC5005 and MIC5007. The MIC5005 is supplied in a 24-pin package and does not include the BCD outputs. The MIC5007 is supplied in a 16-pin package. (See Figure 2 for these members of the display counter/decoder family.)

Functional Description (MIC5002)

V_{GG}, Pin 1

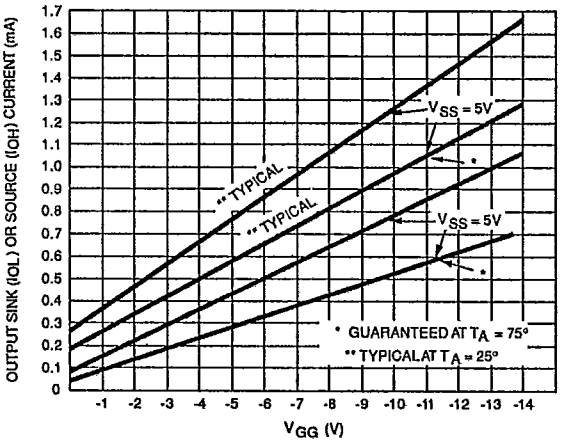
V_{GG} is the output gate drive voltage supply. It must be tied to a supply which is no greater than V_{DD} and no less than V_{DD} - 13.2V. Higher output drive capability is realized when V_{GG} is maintained at the recommended level of V_{DD} - 12V. (See Figure 3 for typical output characteristics.)

$\overline{\text{TRANSFER}}$, Pin 2

While $\overline{\text{TRANSFER}}$ is at logic 0, data in the decade counters is continuously transferred to the latches. This input may be left at 0 for a continuous transfer and display mode or may be driven high to subsequently cause the latches to store the current counter contents.

Storage occurs internally when $\overline{\text{TRANSFER}}$ is taken to a 1 and the next negative edge of $\overline{\text{COUNT}}$ INPUT occurs. This allows asynchronous $\overline{\text{COUNT}}$ and $\overline{\text{TRANSFER}}$ operation since the transfer is terminated internally prior to incrementing the counters. This means that a $\overline{\text{COUNT}}$ negative edge must follow a $\overline{\text{TRANSFER}}$ command before a reset is applied to assure transfer of data. An external reset command must be delayed at least one $\overline{\text{COUNT}}$ negative edge following a transfer. External transfer should terminate at least 1 µS prior to this $\overline{\text{COUNT}}$ negative edge and $\overline{\text{RESET}}$ should occur no sooner than 1 µS following that edge.

Output Drive Characteristics



(I_{OL} @ $V_O = V_{SS}$-0.75V; T_A = 25°C and T_A = 75°C
I_{OH} @ $V_O = V_{DD}$ + 0.75V; V_{DD} = 0V)

Figure 3

$\overline{\text{RESET}}$, Pin 3

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The decade counters are reset to 0000 when $\overline{\text{RESET}}$ is at logic 0. The $\overline{\text{RESET}}$ input at logic 0 also forces the scan counter to the MSD output and resets the $\overline{\text{OVERFLOW}}$ latch output to a logic 1. It maintains this condition as long as a logic 0 is present at $\overline{\text{RESET}}$ and overrides all other associated inputs. As indicated previously, the decade counter should not be reset until a transfer has been terminated.

Since the $\overline{\text{RESET}}$ input resets the scan counter to the MSD, the scan rate must be much faster than the reset rate to allow the lesser significant digits to be enabled. Therefore, F_{SCAN} should be much greater than four times F_{RESET}.

Ideally, the reset pulse should also be made narrow to prevent its duration from causing the MSD to be on much longer than the other digits and thus appear to be brighter.

$\overline{\text{COUNT}}$, Pin 4

The decade counters are synchronously incremented on the negative edge of the $\overline{\text{COUNT}}$ input. The internal oscillator on this input may be overridden by an external signal source or may be allowed to oscillate at a frequency set by a single capacitor tied to this input from the V_{SS} or V_{DD} supply. In systems with considerable noise, better oscillator stability exists when the capacitor is tied to V_{SS}. (See Table 1.)

COUNT EXTEND, Pin 5

COUNT EXTEND is a feature provided to enable MIC5002s to be cascaded. Whenever the counter state attains 9999 count, the COUNT EXTEND output goes high. This output remains logical 1 only until the next negative transition of $\overline{\text{COUNT}}$ occurs or a $\overline{\text{RESET}}$ signal is applied.

Typical Count Oscillator Frequencies vs. Capacitance Between V_{SS} and $\overline{\text{COUNT}}$

Capacitance	Typical Frequency
470 pF	135 kHz
1000 pF	90 kHz
4700 pF	33 kHz
20000 pF	9.5 kHz

(V_{SS} = 5.75V; V_{DD} = 0V; V_{GG} = −12V; T_A = 25°C)

Table 1

Typical Scan Oscillator Frequencies vs. Capacitance Between V_{SS} and SCAN Input

Capacitance	Typical Frequency
470 pF	17 kHz
1000 pF	11.2 kHz
4700 pF	4.0 kHz
20000 pF	1.33 kHz

(V_{SS} = 5.75V; V_{DD} = 0V; V_{GG} = −12V; T_A = 25°C)

Table 2

$\overline{\text{OVERFLOW}}$, Pin 6 (N/A on MIC5007)

$\overline{\text{OVERFLOW}}$ occurs on the 10,000th count input following a reset. It is normally high and, when activated, goes low to indicate that the decade counters have gone from 9999 to 0000 without encountering a reset. Once activated, the $\overline{\text{OVERFLOW}}$ latch will remain low until $\overline{\text{RESET}}$ is pulled low.

$\overline{\text{DECIMAL POINT}}$ IN, Pin 7 (N/A on MIC5007)

With $\overline{\text{DECIMAL POINT}}$ IN held high, the device employs leading zero blanking. This causes any leading zeros in the display latches to be blanked when their DIGIT SELECT goes high. At the start of each MSD to LSD scan, blanking of leading zeros occurs until the first non-zero number occurs in the display or $\overline{\text{DECIMAL POINT}}$ IN is clocked to a 0. Any number following will be displayed. Leading zero blanking does not affect the $\overline{\text{BCD}}$ outputs or the LSD in the display which is displayed even if zero. The LSD output resets the blanking circuitry to begin blanking zeros in the next scan cycle.

Leading zero blanking may be inhibited by wiring $\overline{\text{DECIMAL POINT}}$ IN to ground. The MIC5007 does not have a pin for $\overline{\text{DECIMAL POINT}}$ IN and therefore does not have leading zero blanking.

In the $\overline{\text{DECIMAL POINT}}$ RIGHT mode, even though the $\overline{\text{DECIMAL POINT}}$ IN is clocked, unblanking is delayed until the following digit is enabled.

DECIMAL POINT LEFT OR RIGHT, Pin 8 (N/A on MIC5007)

Bringing this control to logic 1 allows the use of displays with the decimal point physically located on the left side of the numeral. Logic 0 on this input allows for a right-handed decimal point.

$\overline{\text{BLANKING}}$, Pin 9

The $\overline{\text{BLANKING}}$ input at logic 0 forces the 7-segment outputs to the off-state and $\overline{\text{BCD}}$ to the equivalent of the number zero. This condition is maintained on a dc basis as long as the $\overline{\text{BLANKING}}$ input is zero. The DIGIT SELECT outputs continue to operate at the scan rate as described.

SCAN INPUT, Pin 10

The DIGIT SELECT COUNTER is incremented by a negative edge on the SCAN INPUT. During the time the SCAN INPUT is at 0, the SEGMENT and DIGIT SELECT outputs are forced off and the complement $\overline{\text{BCD}}$ outputs are forced to logic 1. The off level of the 7-segment and BCD outputs is determined by the state of the TRUE/COMPLEMENT input. This remains until the SCAN INPUT returns to logic 1.

The DIGIT SELECT COUNTER is a one-of-four counter, scanning from MSD to LSD, enabling one quad latch output at a time, and presenting a logic 1 to the corresponding DIGIT SELECT output.

The internal oscillator on this input may be overridden by an external signal source or may be allowed to oscillate at a frequency set by a single capacitor tied to this input from the V_{SS} or V_{DD} supply. In systems with considerable noise, better oscillator stability exists when the capacitor is tied to V_{SS}. (See Table 2.)

TRUE/COMPLEMENT, Pin 11 (N/A on MIC5007)

When this control is driven to 0, inversion of both the $\overline{\text{BCD}}$ and 7-segment outputs occurs. Depending upon the display used, combinations of the $\overline{\text{BLANKING}}$ input and TRUE/COMPLEMENT control can be chosen to give a lamp test.

$\overline{\text{BCD}}$ OUT, Pins 12 through 15 (N/A on MIC5005)

The $\overline{\text{BCD}}$ outputs are push-pull and are designed to drive directly to the base of common emitter transistors. Output characteristics are shown in Figure 3.

V_{DD}, Pin 16 T-67-31-51

V_{DD} is the negative supply and is nominally ground.

SEGMENT OUTPUTS, Pins 17 through 23 (N/A on MIC5007)

The SEGMENT OUTPUT buffers are identical to the $\overline{\text{BCD}}$ output buffers.

DIGIT SELECT OUTPUTS, Pins 24 through 27

The DIGIT SELECT OUTPUTS are push-pull and go high during their appropriate times to accomplish the multiplexing of the digits.

V_{SS}, Pin 28

V_{SS} is the positive supply voltage and is nominally maintained at 5Vdc with respect to V_{DD}.

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Absolute Maximum Ratings* (See Notes 1 and 2)

Absolute Maximum V_{SS}	7.5V
V_{GG} Supply Range	$0V \geq V_{GG} \geq -13.2V$
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Operating Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{SS}	Supply Voltage	V_{SS} - V_{DD}	4.5	5.0	7.5	V	1,2
V_{GG}	Supply Voltage	V_{GG} - V_{DD}	−13.2	−12	V_{DD}	V	1,2
F_C	Count Frequency		dc		250	kHz	

DC Characteristics

(V_{SS} = +5V ±5%; V_{GG} = V_{DD} = 0V; 0°C ≤ T_A ≤ 70°C unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
V_{IL}	Input Voltage, Logic 0 (Low)		V_{DD}	V_{DD}+0.8	V	
V_{IH}	Input Voltage, Logic 1 (High)	V_{SS} - 1	V_{SS}	V_{SS}+0.3	V	3
I_{SS}	Supply Current, V_{SS}		2.5	5.0	mA	4, Inputs open
I_{GG}	Supply Current, V_{GG}		0.2	0.5	mA	V_{GG} = −12V
C_{IN}	Input Capacitance		3	10	pF	T_A = 25°C, f = 1MHz, V_{IN} = V_{SS}
I_{IL}	Input Current, Logic 0, Count Input Scan Input Decimal Point Input Other Logic Inputs			1.6 1.6 1.0 1.0	mA mA µA mA	5 5
I_{OL}	Output Current, Logic 0	0.5			mA	6, V_{GG} = −12V
I_{OH}	Output Current, Logic 1	0.5			mA	6, V_{GG} = −12V
V_{OL}	Output Voltage, Logic 0			V_{DD}+0.2	V	4
V_{OH}	Output Voltage, Logic 1	V_{DD}−0.2			V	4

NOTES:
1. V_{DD} = 0V.
2. V_{SS} - V_{GG} no more than 20.7V.
3. Internal pull-up resistors (approx. 10k) are provided at all inputs other than $\overline{\text{Count Input}}$, Scan Input and $\overline{\text{Decimal Point Input}}$.
4. V_{GG} = −12V ± 10%. Outputs open.
5. Measurement made at $V_I = V_{DD}$ + 0.4V. This condition is sufficient to represent a logic 0 and hold off or override the internal oscillators. Maximum current at V_I = +0.4V is 1.6mA. 400µA source current is sufficient to represent a logic 1 and hold off or override the internal oscillators.
6. I_{OL} measured at $V_0 = V_{SS}$ - 0.75V. (Direct driving base pnp emitter to V_{SS}.) I_{OH} measured at $V_0 = V_{DD}$ + 0.75V. (Direct driving base npn emitter to V_{DD}.)

AC Characteristics

(V_{SS} = +5V ±%; V_{GG} = V_{DD} = 0V; 0°C ≤ T_A ≤ 70°C unless otherwise noted) T-67-31-51

Symbol	Parameter		Min.	Typ.	Max.	Units	Notes
f_{CI}	$\overline{\text{Count Input}}$ Frequency		dc		250	kHz	
f_{SI}	Scan Input Frequency		dc		50	kHz	
t_{RD}	Reset to Any Output Delay				15	µS	
t_{PW}	Logic 0 Pulse Width,	$\overline{\text{Reset Input}}$	1.0			µS	
		$\overline{\text{Count Input}}$	1.0			µS	
		Scan Input	10.0			µS	
		Transfer Input	2.5			µS	
t_{PH}	Logic 1 Time	$\overline{\text{Count Input}}$	3.0			µS	
		Scan Input	10.0			µS	
t_{SD}	Scan to Output Disable Time						
		Digit Select Outputs			15	µS	7
		All Data Outputs			15	µS	7
t_{SE}	Scan to Output Enable Time						
		Digit Select Outputs			15	µS	8
		All Data Outputs			15	µS	8
t_{CE}	Count Input to Count Extend Delay to 1 or 0				15	µS	9
t_{OF}	Count Input to Overflow Delay (On)				15	µS	9
t_{ROF}	Reset Input to Overflow Delay (Off)				5	µS	

NOTES:
1. V_{DD} = 0V.
2. V_{SS} - V_{GG} no more than 20.7V.
3. Internal pull-up resistors (approx. 10k) are provided at all inputs other than $\overline{\text{Count Input}}$, Scan Input and $\overline{\text{Decimal Point Input}}$.
4. V_{GG} = −12V ± 10%. Outputs open.
5. Measurement made at $V_I = V_{DD} + 0.4V$. This condition is sufficient to represent a logic 0 and hold off or override the internal oscillators. Maximum current at V_I = +0.4V is 1.6mA. 400µA source current is sufficient to represent a logic 1 and hold off or override the internal oscillators.
6. I_{OL} measured at $V_O = V_{SS} - 0.75V$. (Direct driving base pnp emitter to V_{SS}.) I_{OH} measured at $V_O = V_{DD} + 0.75V$. (Direct driving base npn emitter to V_{DD}.)
7. Delay measured from the negative edge of the SCAN input.
8. Delay measured from the rising edge of the SCAN input.
9. Delay measured from the negative edge of the $\overline{\text{COUNT}}$ input.

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Typical Application: Revolution Counter

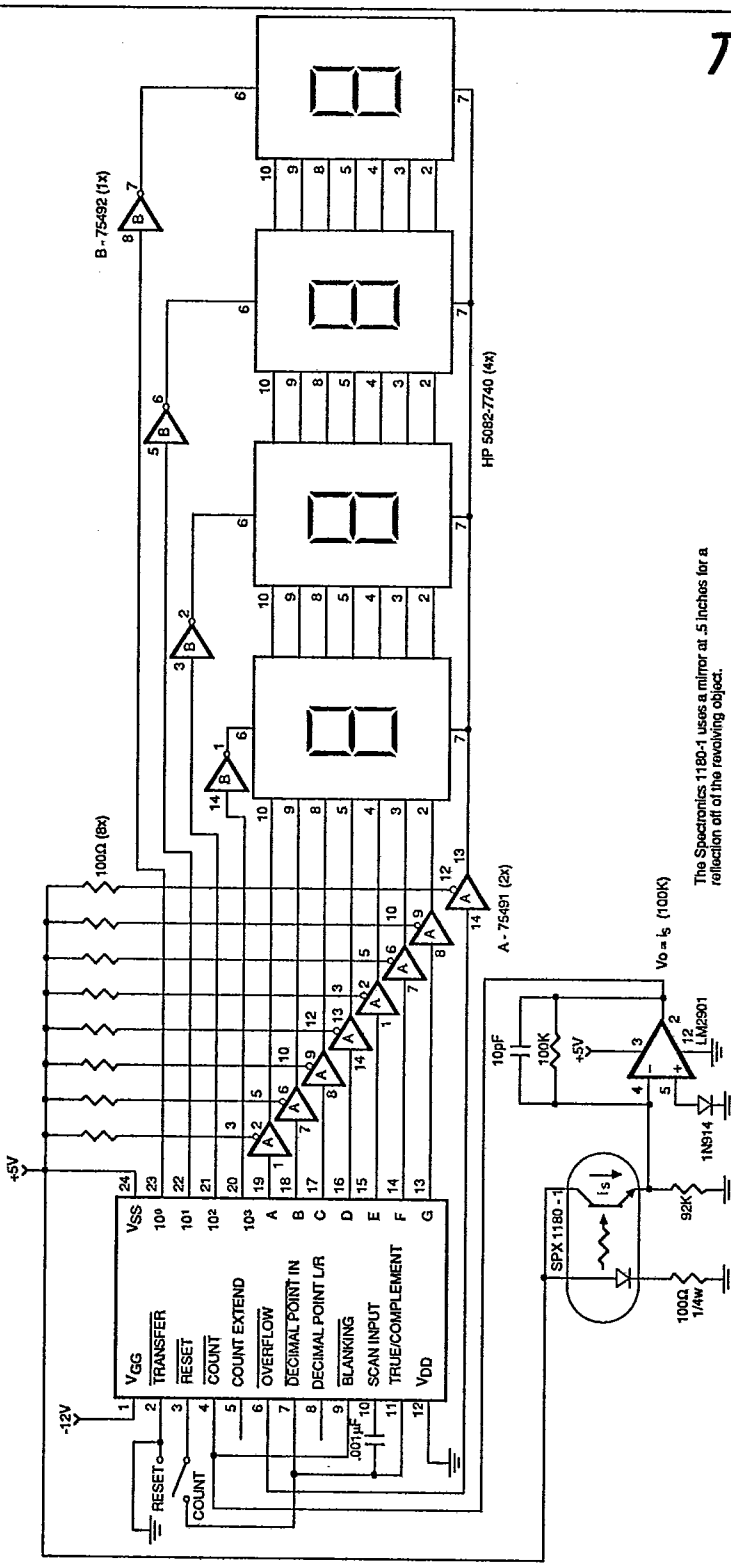

Figure 5