MIC5283

120 V_{IN}, 150 mA, Ultra-Low I_Q, High-PSRR Linear Regulator

Features

- Wide Input Voltage Range: 6V to 120V DC
- Ultra-Low Quiescent Current: 8 µA
- 150 mA Guaranteed Output Current
- Adjustable Output from 1.22V to 5.5V
- Stable with Ceramic Capacitors
- Ultra-High PSRR (75 dB at 10 kHz)
- Ultra-High Line Rejection (Load Dump)
- High Output Accuracy
  - ±3% Initial Accuracy
- Thermal-Shutdown and Current-Limit Protection
- Thermally-Efficient, 8-Lead ePad SOIC Package
- Very Low-Profile 3 mm × 3 mm VDFN Package

Applications

- Industrial Applications
- Remote Keyless Entry Power Supply
- Telecom Applications
- Off-Line Power Supplies

General Description

The MIC5283 high-performance linear regulator offers a very-wide input operating voltage range, up to 120V DC, and supplies an output current of up to 150 mA.

Ideal for high input voltage applications such as industrial and telecom, the MIC5283 offers ±3% initial accuracy, extremely high-power supply rejection ratio (75 dB at 10 kHz) and an ultra-low quiescent current of 8 µA. The MIC5283 is optimized for high-voltage line transients, making it ideal for harsh environment applications.

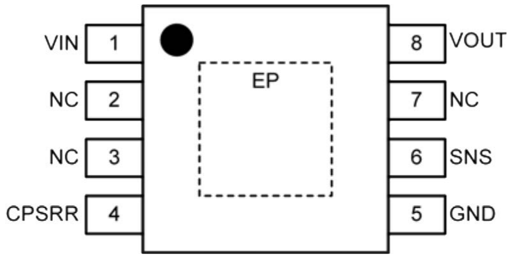
The MIC5283 is offered in both fixed output voltage (3.3V or 5.0V) and adjustable output voltage (1.22V to 5.5V) options.

The MIC5283 operates over a −40°C to +125°C temperature range and is available in lead-free, RoHS compliant, ePad SOIC-8 and 3 mm × 3 mm VDFN packages

Package Types

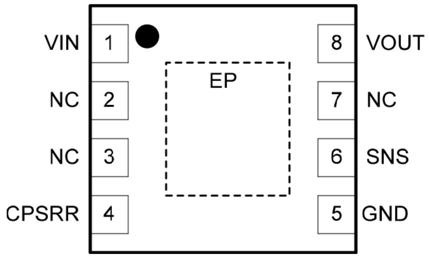
MIC5283YME

8-Lead SOIC | Fixed Voltages



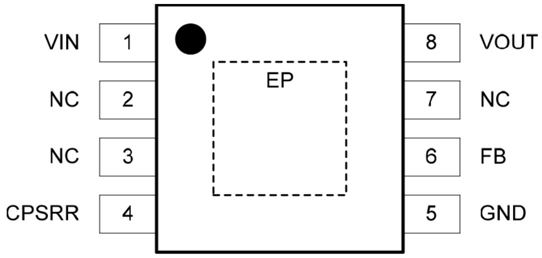
MIC5283YML

8-Lead VDFN | Fixed Voltages



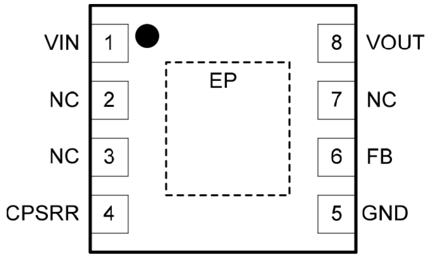
MIC5283-x.xYME

8-Lead SOIC | Adjustable Voltages

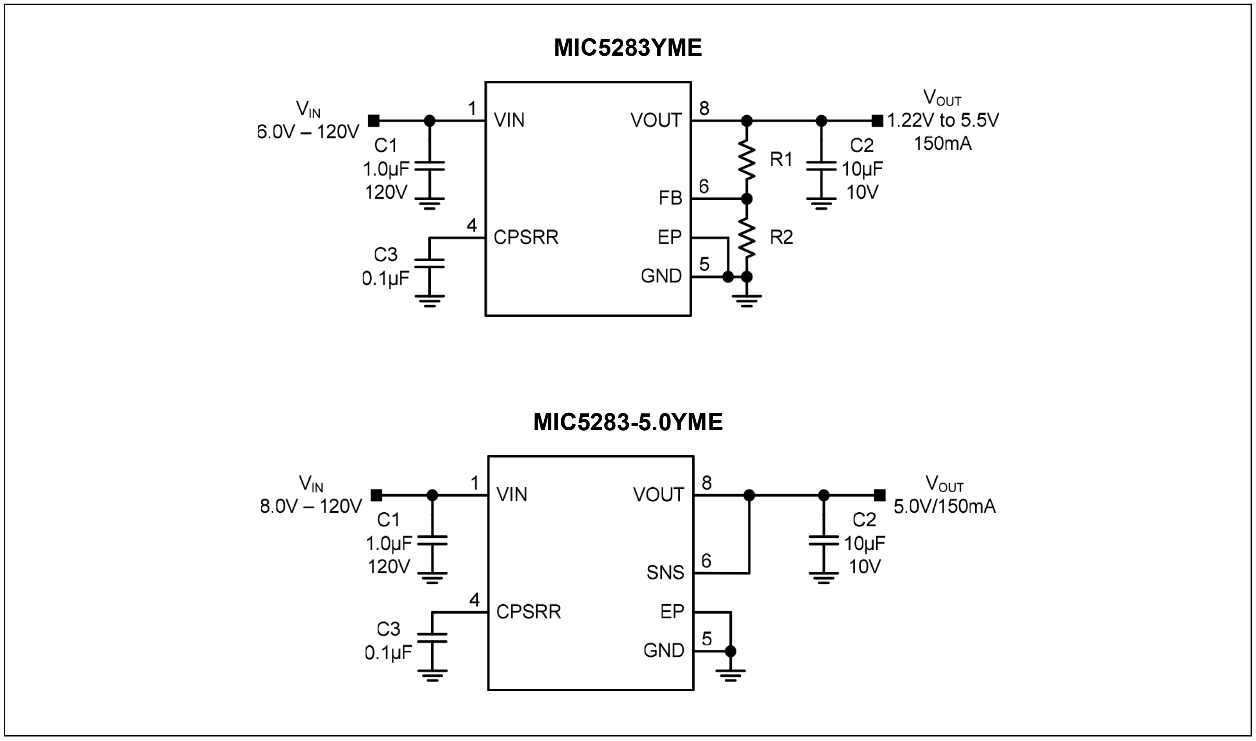


MIC5283-x.xYML

8-Lead VDFN | Adjustable Voltages

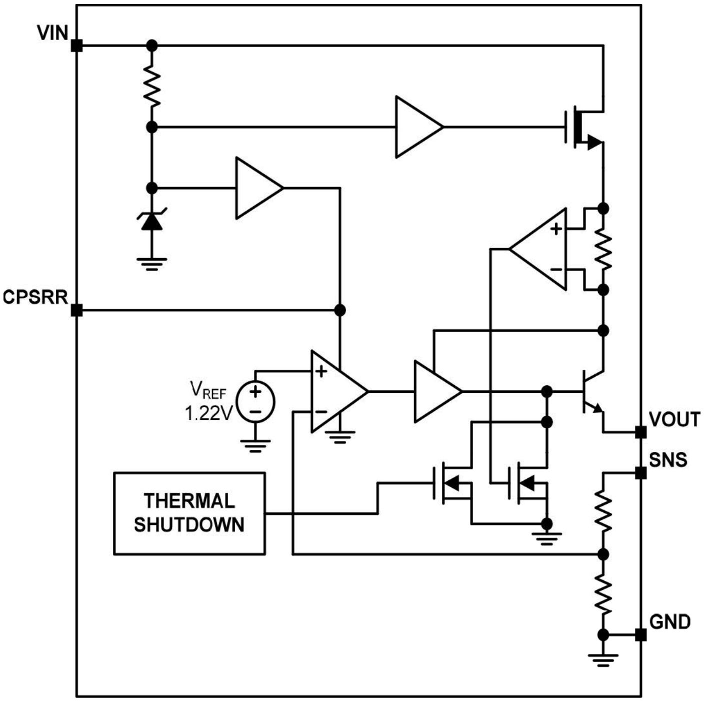


Typical Application Circuits

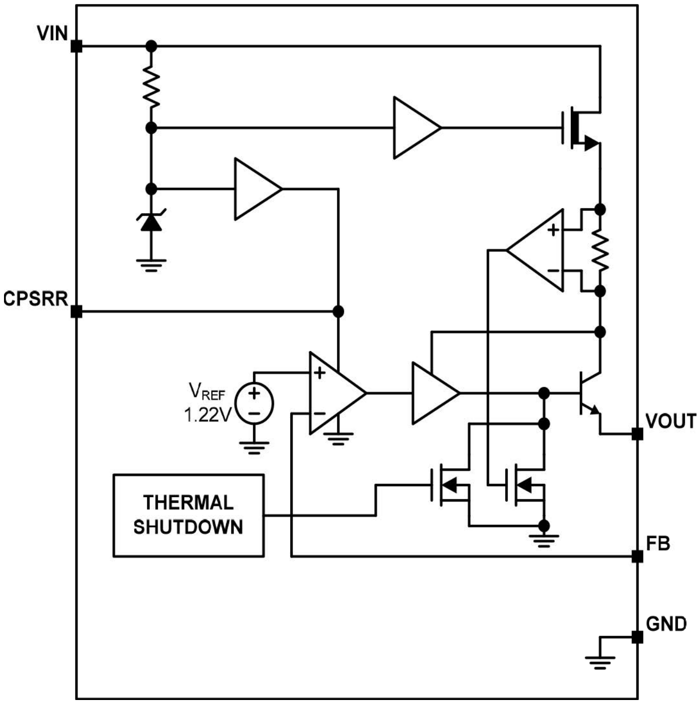


Functional Block Diagram

MIC5283 Fixed Version



MIC5283 Adjustable Version



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

VIN to GND	–0.3V to +125V
VCPSRR to GND	–0.3 to +14V
VFB, VSNS, VOUT to GND	–0.3V to +6V
HBM ESD Ratings (Note 1)	2 kV
MM ESD Ratings (Note 1)	200V

Operating Ratings ‡

V_{IN}	+6V to +120V
V_{OUT} Adjust Range	+1.22V to +5.5V
Power Dissipation (P_D)	Internally Limited (Note 2)

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ Notice: The device is not guaranteed to function outside its operating ratings.

Note 1: Devices are ESD sensitive; use proper handling precautions.

2: The maximum allowable power dissipation at any T_A (ambient temperature) is $P_{D(max)} = (T_{J(max)} – T_A) / \theta_{JA}$. Exceeding the maximum allowable power dissipation results in excessive die temperature, and causes the regulator to enter thermal shutdown.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, C_{IN} = 1.0 µF, C_{PSRR} = 0.1 µF, C_{OUT} = 10 µF, V_{OUT} = 5.0V or 3.3V, I_{OUT} = 100 µA, T_A = 25°C, **bold** values indicate –40°C ≤ T_J ≤ +125°C, unless noted. (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Power Supply Input						
Input Voltage Range	V_{IN}	6	—	120	V	—
Quiescent Supply Current	I_Q	—	8	**14**	µA	I_{OUT} = 0
Output Voltage						
Output Voltage Accuracy	ΔV_{OUT}	–3	—	+3	%	Variation from nominal VOUT 100 µA ≤ I_{OUT} ≤ 150 mA
		–5	—	**+5**	%	
Line Regulation (Note 2)	$\Delta V_{OUT}/V_{OUT}$	**–0.5**	0.04	**+0.5**	%/V	10V ≤ V_{IN} ≤ 120V
Feedback Input (Adjustable)						
Feedback Voltage	V_{FB}	1.183	1.220	1.256	V	100 µA ≤ I_{OUT} ≤ 150 mA
		1.159	1.220	**1.281**	V	
Feedback Current	I_{FB}	—	3.2	—	nA	V_{FB} = 1.22V
Current Limit						
Current Limit	I_{LIMIT}	**180**	300	**500**	mA	V_{OUT} = 0V
Ripple Rejection						
Power Supply Rejection Ratio (I_{OUT} = 50 mA)	PSRR	—	70	—	dB	100 Hz ≤ f ≤ 1 kHz
		—	75	—	dB	1 kHz < f ≤ 30 kHz
		—	65	—	dB	30 kHz < f ≤ 100 kHz

Note 1: Specifications are for packaged products only.

2: Line regulation is a percentage of V_{OUT}.

ELECTRICAL CHARACTERISTICS (CONTINUED)

V_{IN} = 12V, C_{IN} = 1.0 µF, C_{PSRR} = 0.1 µF, C_{OUT} = 10 µF, V_{OUT} = 5.0V or 3.3V, I_{OUT} = 100 µA, T_A = 25°C, **bold** values indicate –40°C ≤ T_J ≤ +125°C, unless noted. (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Power Dropout Voltage						
Dropout Voltage	$V_{IN} – V_{OUT}$	—	1.8	**2.8**	V	I_{OUT} = 150 mA
Thermal Protection						
Thermal-Shutdown Temperature	T_{SHDN}	—	155	—	°C	TJ rising
Thermal-Shutdown Hysteresis	T_{SHDN_HYS}	—	15	—	°C	—

Note 1: Specifications are for packaged products only.

2: Line regulation is a percentage of V_{OUT}.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Operating Junction Temperature Range	T_J	–40	—	+125	°C	—
Storage Temperature Range	T_A	–65	—	+150	°C	—
Lead Temperature	—	—	—	+260	°C	Soldering, 10 seconds
Thermal Resistance 8-Lead VDFN	θ_{JA}	—	60	—	°C/W	Note 1
Thermal Resistance 8-Lead SOIC	θ_{JA}	—	41	—	°C/W	

Note 1: The maximum allowable power dissipation at any T_A (ambient temperature) is $P_{D(max)} = (T_{J(max)} – T_A) / \theta_{JA}$. Exceeding the maximum allowable power dissipation results in excessive die temperature, and causes the regulator to enter thermal shutdown.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

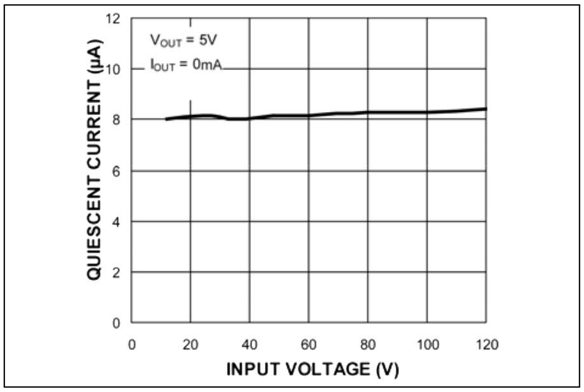


FIGURE 2-1: *Quiescent Supply Current vs. Input Voltage.*

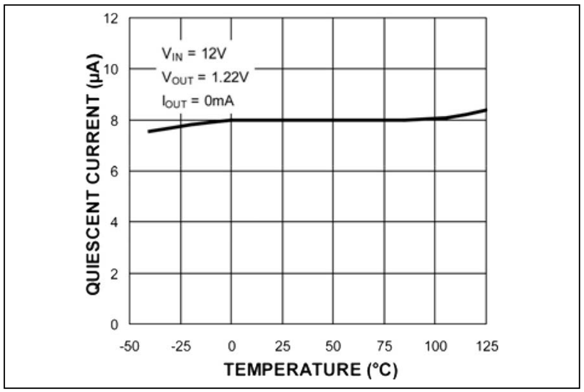


FIGURE 2-2: *Quiescent Supply Current vs. Temperature.*

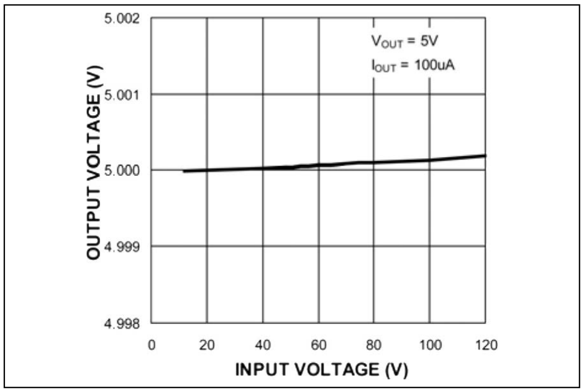


FIGURE 2-3: *.Output Voltage vs. Input Voltage.*

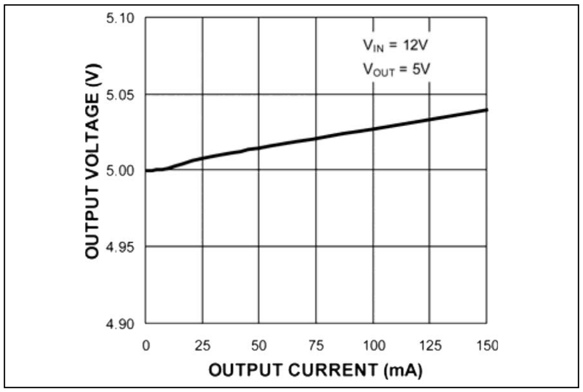


FIGURE 2-4: *Output Voltage vs. Output Current.*

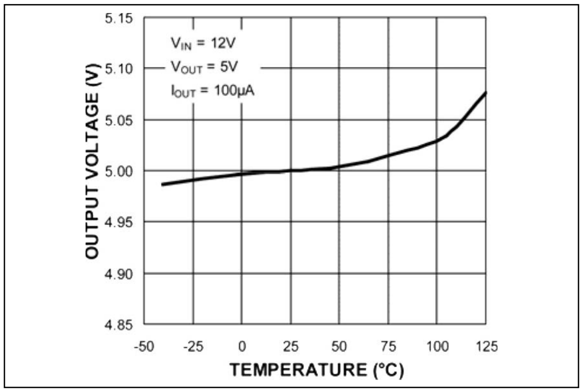


FIGURE 2-5: *Output Voltage vs. Temperature.*

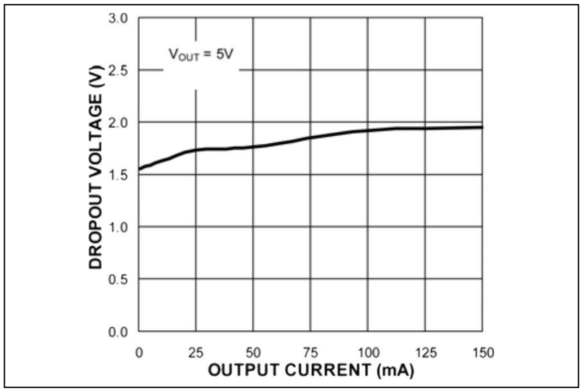


FIGURE 2-6: *Dropout Voltage vs. Output Current.*

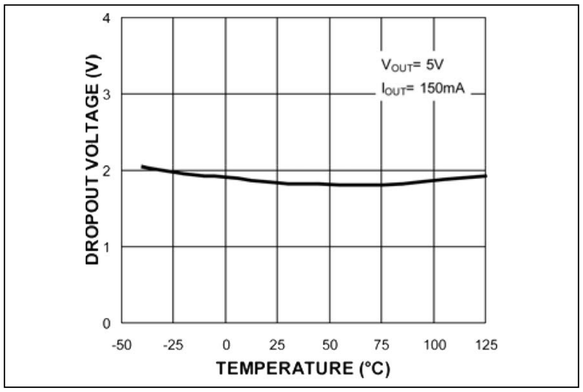


FIGURE 2-7: *Dropout Voltage vs. Temperature.*

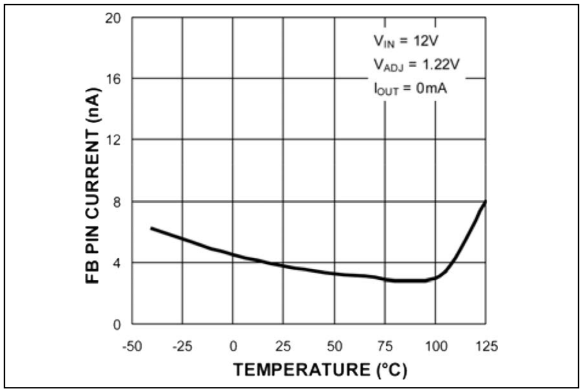


FIGURE 2-8: *Feedback Pin Current vs. Temperature.*

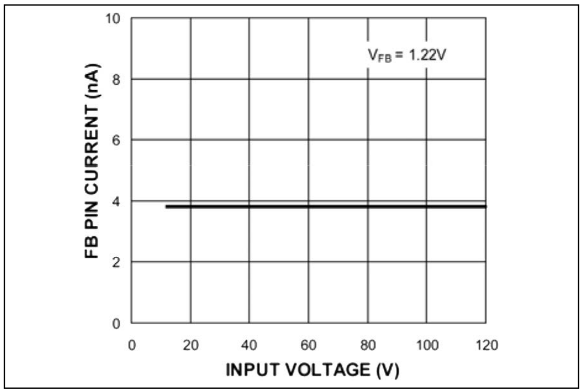


FIGURE 2-9: *Feedback Pin Current vs. Input Voltage.*

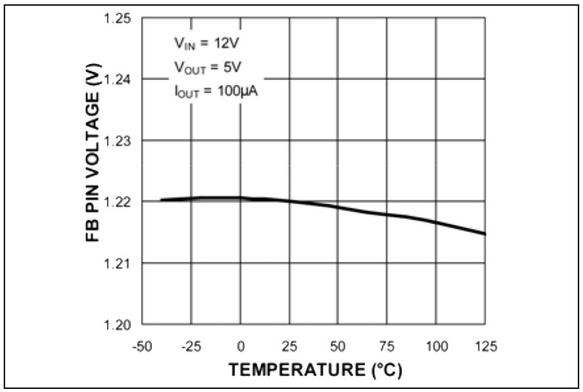


FIGURE 2-10: *Feedback Pin Voltage vs. Temperature.*

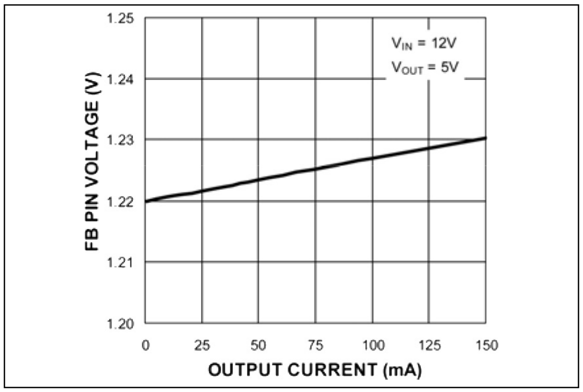


FIGURE 2-11: *Feedback Pin Voltage vs. Output Current.*

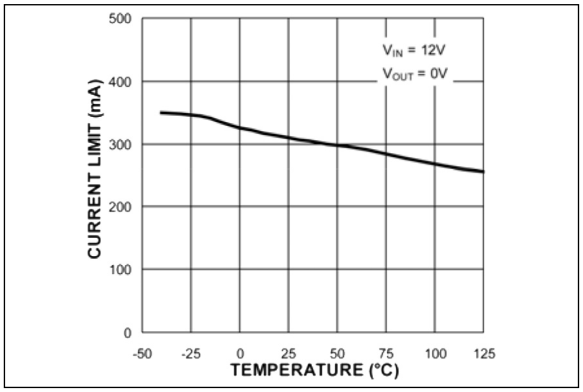


FIGURE 2-12: *Current Limit vs. Temperature.*

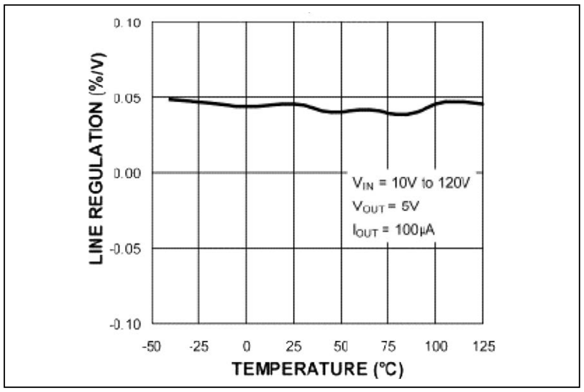


FIGURE 2-13: Line Regulation vs. Temperature.

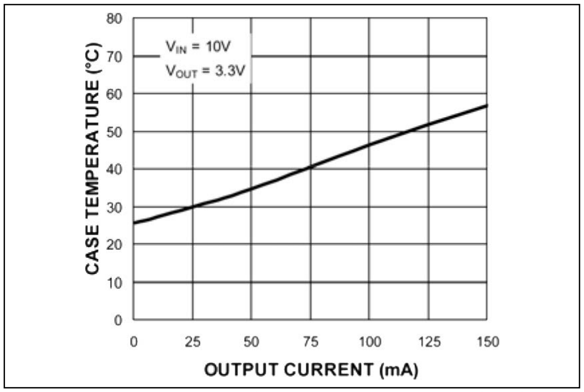


FIGURE 2-14: Case Temperature (ML) vs. Output Current. (Please see Note.)

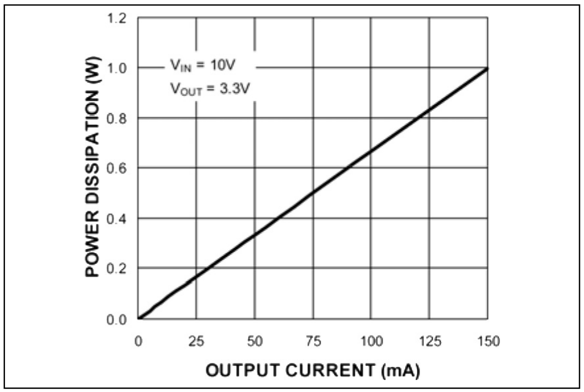


FIGURE 2-15: Power Dissipation (ML) vs. Output Current.

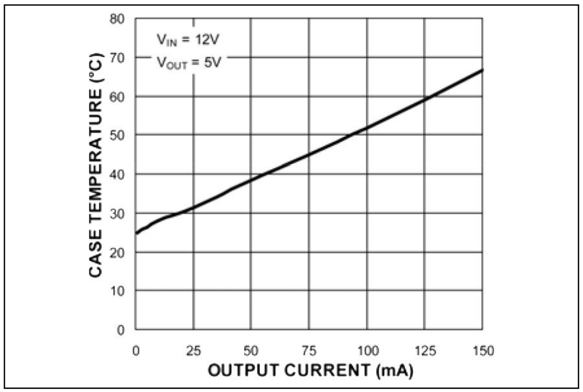


FIGURE 2-16: Case Temperature (ME) vs. Output Current. (Please see Note.)

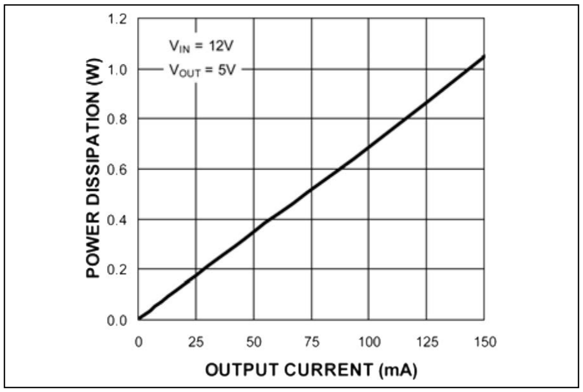


FIGURE 2-17: Power Dissipation (ME) vs. Output Current.

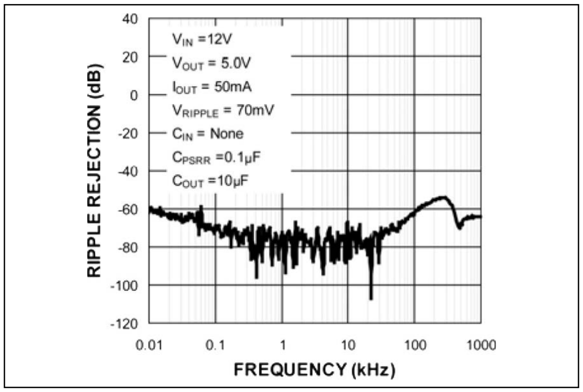


FIGURE 2-18: PSRR vs. Frequency.

Note: The temperature measurement was taken at the hottest point on the MIC5283 case mounte don a 2.25 square-inch PCB at an ambient temperature of 25°C; see “Thermal Measurement” section. Actual results will depend upon the size of the PCB, ambient temperature, and proximity to other heat-emitting components.

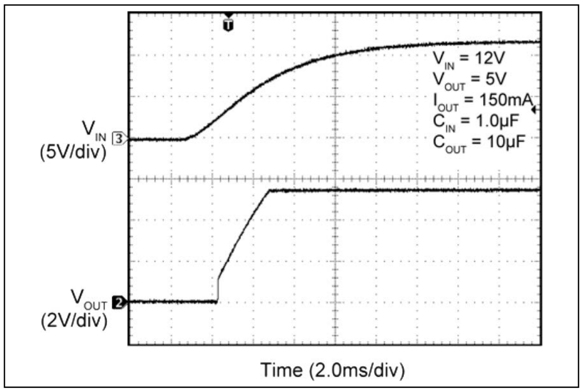


FIGURE 2-19: *Soft Turn-On into Full Load.*

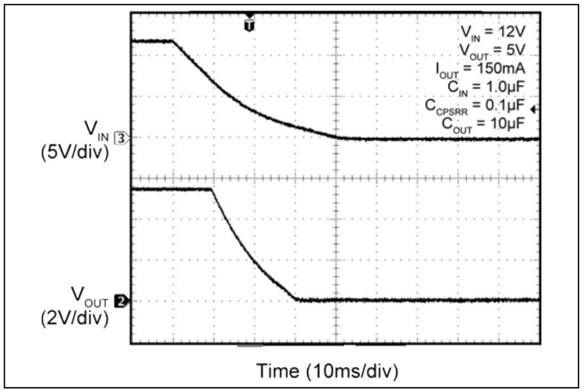


FIGURE 2-20: *Soft Turn-Off.*

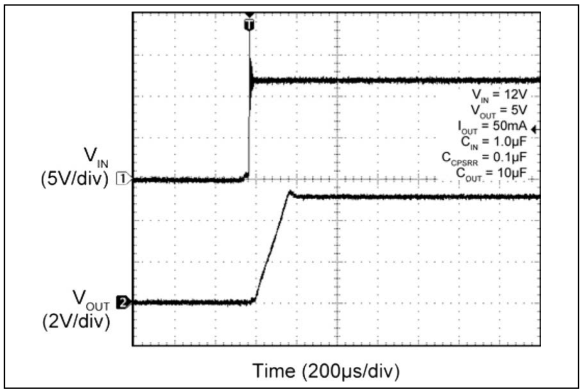


FIGURE 2-21: *Fast Turn-On.*

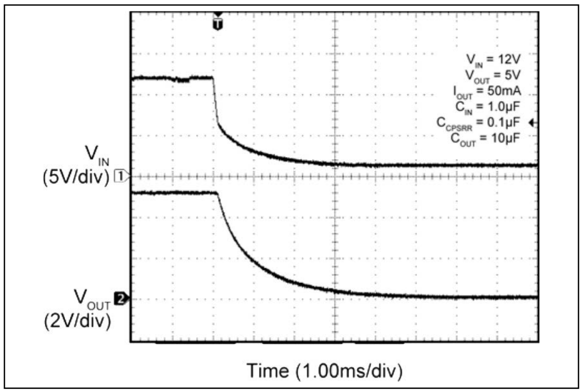


FIGURE 2-22: *Fast Turn-Off.*

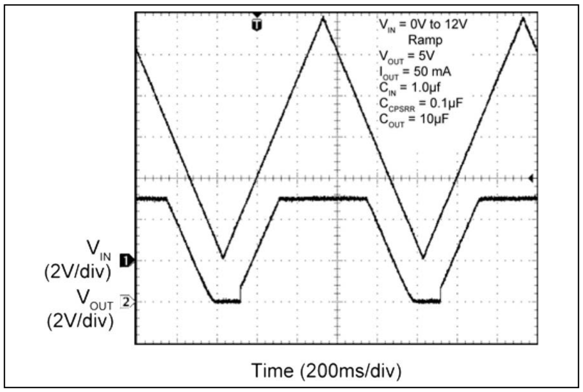


FIGURE 2-23: *V_{IN} ULVO Threshold.*

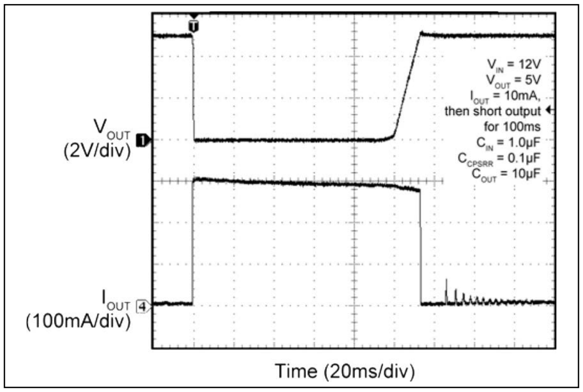


FIGURE 2-24: *Current Limit.*

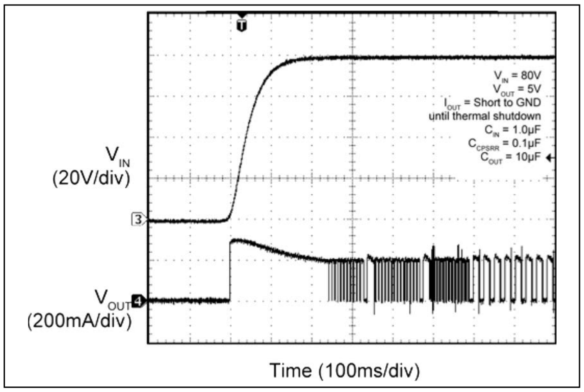


FIGURE 2-25: *Thermal Shutdown Response.*

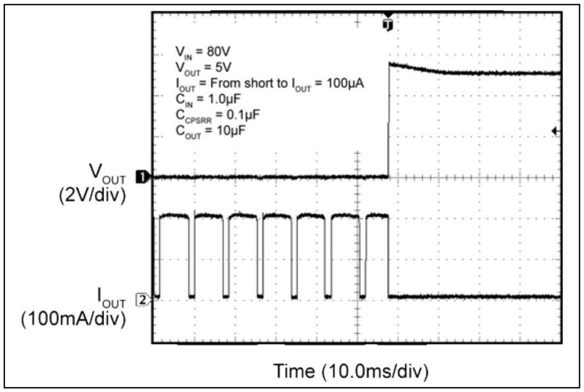


FIGURE 2-26: *V_{OUT} Recovery from Thermal Shutdown.*

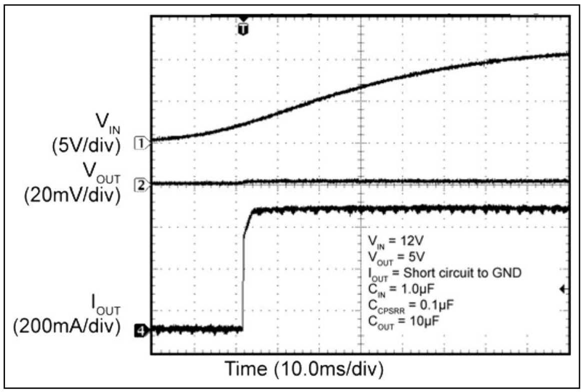


FIGURE 2-27: *Turn-On into Short Circuit.*

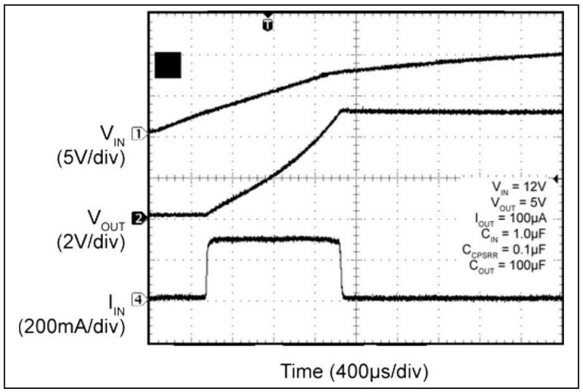


FIGURE 2-28: *Inrush Current Response.*

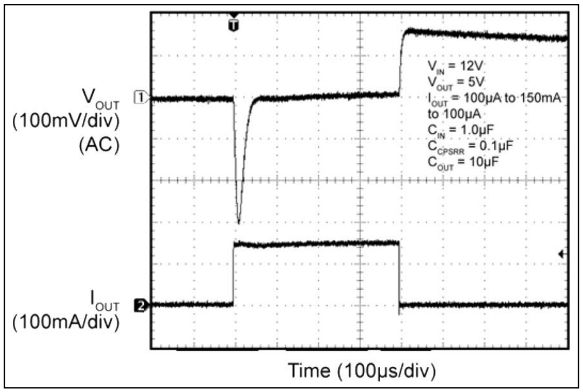


FIGURE 2-29: *Load Transient Response.*

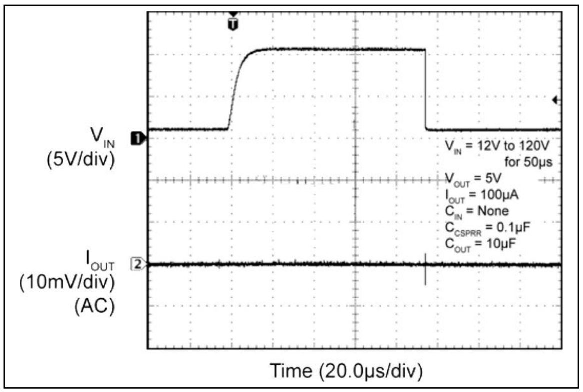


FIGURE 2-30: *Line Transient Response.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number (Fixed)	Pin Number (Adj.)	Pin Name	Description
1	1	VIN	Supply Voltage Input. Connect 1µF capacitor from VIN to GND.
2, 3, 7	2, 3, 7	NC	Not internally connected. Connect NC to GND or leave unconnected.
4	4	CPSRR	Bypass Capacitor Connection. Connect 0.1µF capacitor from CPSRR to GND.
5	5	GND	Ground.
	6	FB	Feedback Connection. For external resistor divider to set V_{OUT}.
6		SNS	Sense input. Connect SNS to VOUT.
8	8	VOUT	Regulator Output. Connect 10µF capacitor from VOUT to GND.
EP	EP	EP	Exposed Pad (ePad) for Thermal Dissipation. Connect EP to GND.

4.0 APPLICATION INFORMATION

The MIC5283 voltage regulator accepts a 6V to 120V input voltage and has an ultra-low 8 µA typical quiescent current while offering an excellent line transient response and PSRR. These features make it ideal for harsh, noisy environments. All options offer 150 mA of output current.

The MIC5283YML and MIC5283YME options offer adjustable output voltage from 1.22V to 5.5V. The MIC5283-3.3YML and MIC5283-3.3YME offer fixed 3.3V outputs and the MIC5283-5.0YML and MIC5283-5.0YME offer fixed 5.0V outputs. The YME packaged devices feature a heat slug to more effectively remove heat from the die.

4.1 Thermal Protection

The MIC5283 has internal thermal shutdown to protect it from excessive heating of the die. When the junction temperature exceeds approximately +155°C, the output is disabled and the device begins to cool down. The device turns back on when the junction temperature cools by 15°C. This will result in a cycled output during continuous thermal-overload conditions.

4.2 Current Limit

The MIC5283 features output current-limit protection. The output sustains a continuous short circuit to GND without damage to the device, but thermal shutdown often results. The typical value for the current limit of the MIC5283 is 300 mA.

4.3 Input Capacitor

Connect a 1.0 µF capacitor from VIN to GND. Microchip recommends the C5750X7R2E105M, 1.0 µF, 250V capacitor made by TDK. When using a different capacitor, assure that the voltage rating of the capacitor has adequate headroom to withstand any potential transient.

4.4 CPSRR Capacitor

To maintain high power supply rejection, connect a 0.1 µF capacitor from CPSRR to GND. The voltage rating of the capacitor must be at least 14V.

4.5 Output Capacitor

Connect a 10 µF capacitor from VOUT to GND. Assure that the voltage rating of the capacitor exceeds the designed output voltage of the MIC5283.

4.6 Output Voltage Setting

For the MIC5283YML and MIC5283YME, VOUT is programmable from 1.22V to 5.5V using an external resistive divider. VOUT is set using the following equation:

EQUATION 4-1:

$$V_{OUT} = V_{REF} \times \left(\frac{R1}{R2} + 1\right)$$

where V_{REF} = 1.22V, and R1 and R2 form the feedback voltage divider from VOUT to GND.

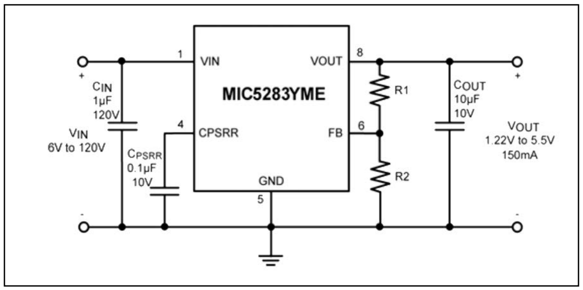


FIGURE 4-1: Output Voltage Setting for the MIC5283YME.

4.7 Thermal Measurements

It is always prudent to measure an IC's case temperature to make sure that it is within operating limits, but it is easy to get erroneous results. The standard thermocouple that comes with many voltage meters uses a large wire gauge that behaves like a heat-sink, resulting in artificially low case temperature measurements.

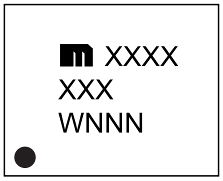
Use a thermocouple of 36-gauge wire or smaller, such as the Omega (5SC-TT-K-36-36), to minimize the heat-sinking effect. Also, apply a thermal compound to maximize heat transfer between the IC and the thermocouple.

One recommended alternative to consider is an infrared thermometer. The IR thermometer from Optris has a 1 mm spot size, ideal for monitoring small surface mount packages. Also, the optional stand makes it easy to keep the beam on the IC for long periods of time.

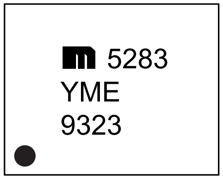
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

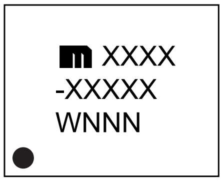
8-Lead SOIC (Fixed)



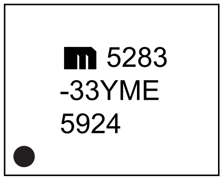
Example



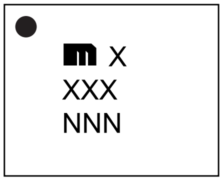
8-Lead SOIC (Adj.)



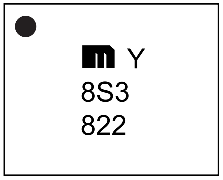
Example



8-Lead VDFN (All)



Example



ORDERING INFORMATION

Part Number	Output Voltage	Top Mark	Temperature Range	Package	Lead Finish
MIC5283YME	Adjustable	5283YME	–40°C to +125°C	8-Lead ePad SOIC	Pb-Free
MIC5283-3.3YME	3.3V	5283-33YME	–40°C to +125°C	8-Lead ePad SOIC	Pb-Free
MIC5283-5.0YME	5.0V	5283-50YME	–40°C to +125°C	8-Lead ePad SOIC	Pb-Free
MIC5283YML	Adjustable	A83	–40°C to +125°C	8-Lead 3 mm × 3 mm VDFN	Pb-Free
MIC5283-3.3YML	3.3V	8S3	–40°C to +125°C	8-Lead 3 mm × 3 mm VDFN	Pb-Free
MIC5283-5.0YML	5.0V	583	–40°C to +125°C	8-Lead 3 mm × 3 mm VDFN	Pb-Free

Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

●, ▲, ▼ Pin one index is identified by a dot, delta up, or delta down (triangle mark).

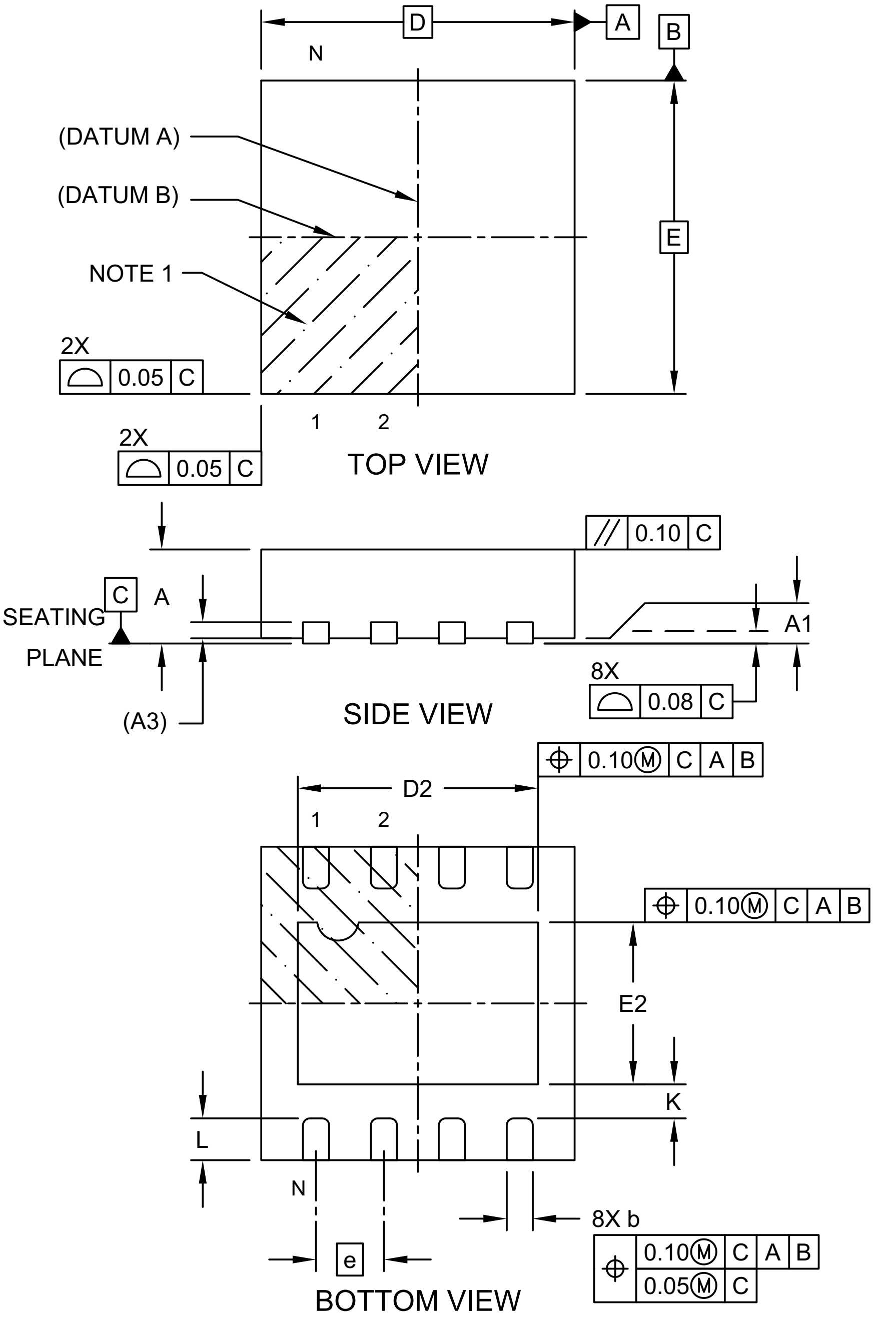
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (‾) symbol may not be to scale.

Note: If the full seven-character YYWWNNN code cannot fit on the package, the following truncated codes are used based on the available marking space:
6 Characters = YWWNNN; 5 Characters = WWNNN; 4 Characters = WNNN; 3 Characters = NNN; 2 Characters = NN; 1 Character = N.

8-Lead 3 mm × 3 mm × 0.9 mm VDFN Package Outline and Recommended Land Pattern

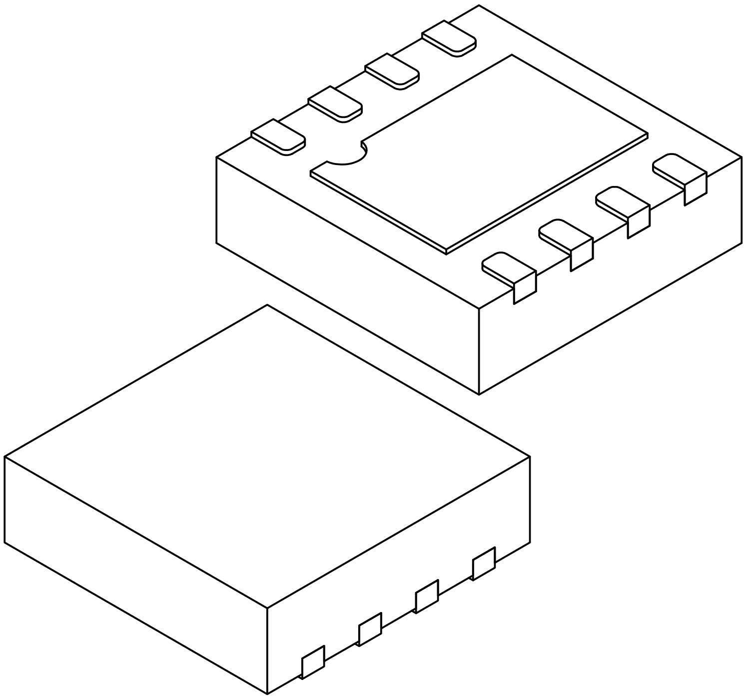
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1021 A Sheet 1 of 2

8-Lead 3 mm × 3 mm × 0.9 mm VDFN Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	8		
Pitch	e	0.65 BSC		
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.203 REF		
Overall Length	D	3.00 BSC		
Exposed Pad Length	D2	2.25	2.30	2.35
Overall Width	E	3.00 BSC		
Exposed Pad Width	E2	1.50	1.55	1.60
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.20	-	-

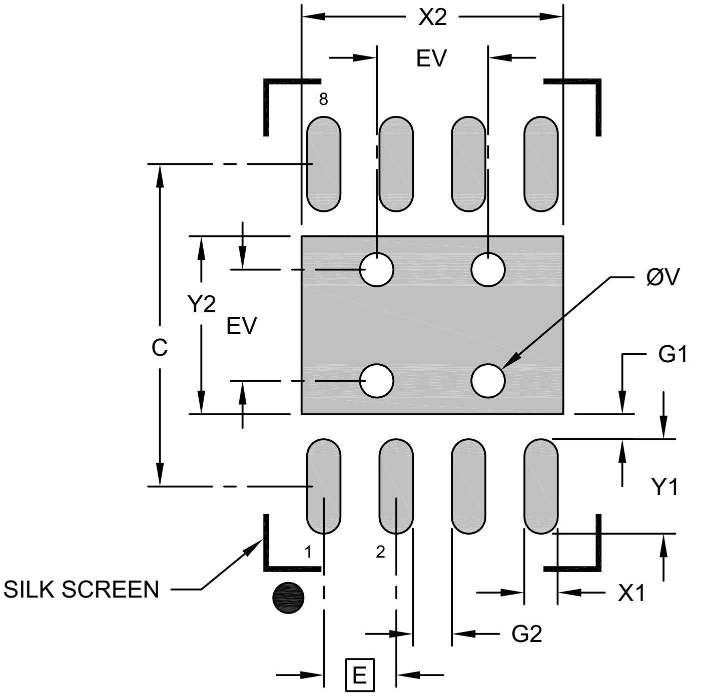
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1021 A Sheet 1 of 2

8-Lead 3 mm × 3 mm × 0.9 mm VDFN Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	X2			2.35
Optional Center Pad Length	Y2			1.60
Contact Pad Spacing	C		2.90	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.85
Contact Pad to Center Pad (X8)	G1	0.23		
Contact Pad to Contact Pad (X6)	G2	0.35		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

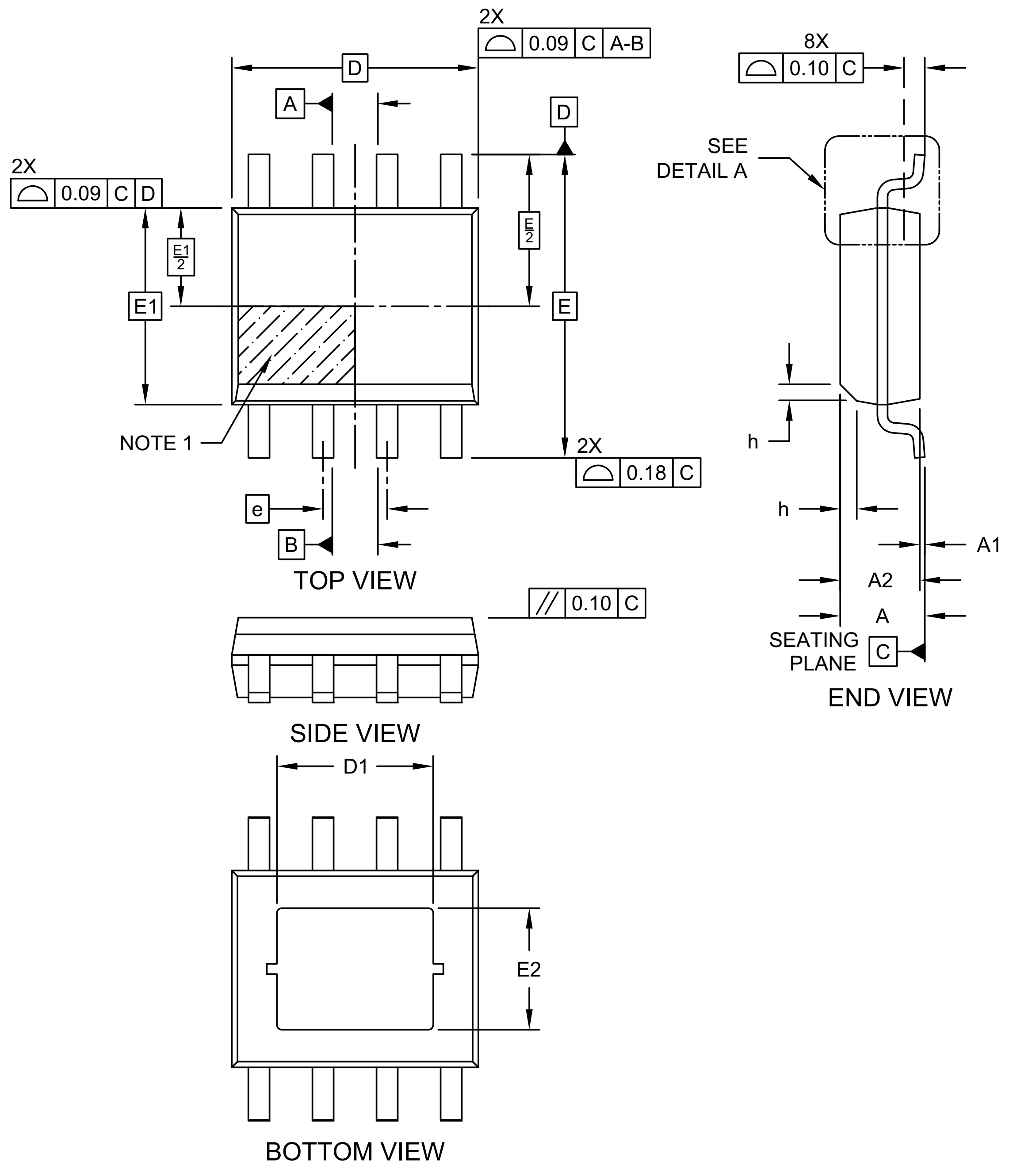
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3021 Rev A

8-Lead 3.9 mm SOIC with 3.1 mm × 2.41 mm ePad Package Outline and Recommended Land Pattern

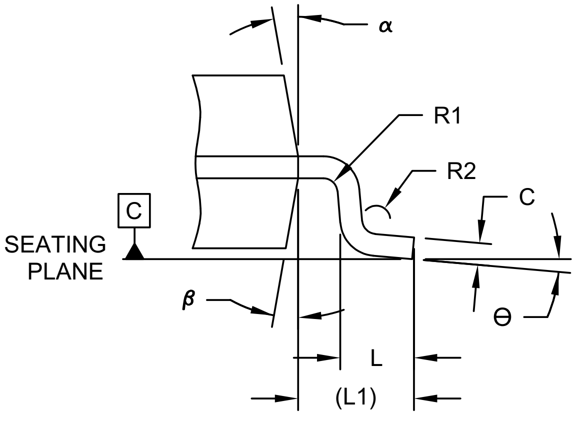
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



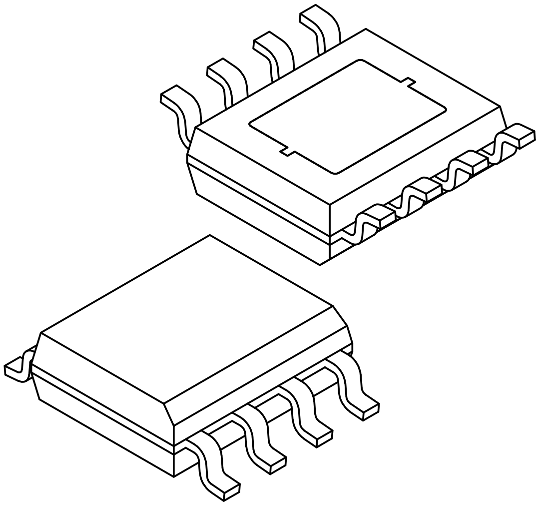
Microchip Technology Drawing C04-1136 Rev B Sheet 1 of 2

8-Lead 3.9 mm SOIC with 3.1 mm × 2.41 mm ePad Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL A



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	1.43	1.55	1.68
Standoff	A1	0.00	0.05	0.10
Molded Package Thickness	A2	1.25	-	-
Overall Length	D		4.89 BSC	
Exposed Pad Length	D1	-	3.10	-
Overall Width	E		6.02 BSC	
Molded Package Width	E1		3.90 BSC	
Exposed Pad Width	E2	-	2.41	-
Terminal Width	b	0.35	0.41	0.49
Lead Thickness	c	0.19	0.20	0.25
Terminal Length	L	0.41	0.64	0.89
Footprint	L1		1.04 REF	
Foot Angle	Θ	0°	5°	8°
Lead Bend Radius	R1	0.07	-	-
Lead Bend Radius	R2	0.07	-	-
Mold Draft Angle	α	5°	-	15°
Mold Draft Angle	β	5°	-	15°

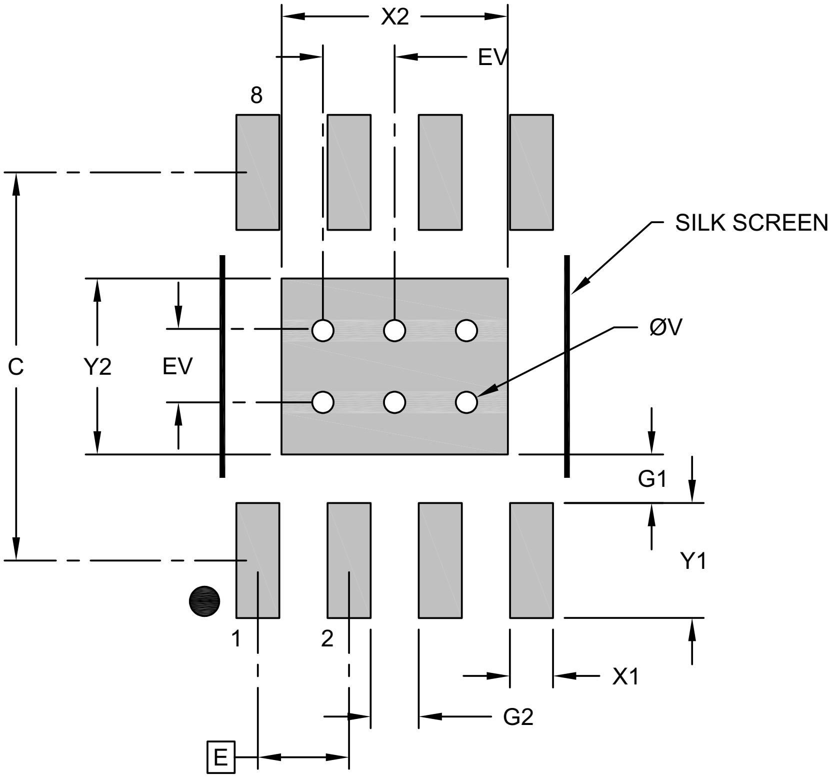
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1136 Rev B Sheet 2 of 2

8-Lead 3.9 mm SOIC with 3.1 mm × 2.41 mm ePad Package Outline and Recommended Land Pattern

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Optional Center Pad Width	X2			3.15
Optional Center Pad Length	Y2			2.45
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.60
Contact Pad to Center Pad (X8)	G1	0.68		
Contact Pad to Contact Pad (X6)	G2	0.67		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-1136 Rev B

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (May 2023)

- Converted Micrel document MIC5283 to Microchip data sheet DS20006761A.
- Minor text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART No.	-X.XX	X	XX	-XX
Device	Output Voltage	Junction Temp. Range	Package	Media Type

Device: MIC5283: 500 mA-Peak Output LDO Regulator

Output Voltage:
<blank>= Adjustable Voltage
-3.3 = 3.3V
-5.0 = 5.0V

Junction Temperature Range: Y = –40°C to +125°C

Package:
ML = 8-Lead VDFN
ME = 8-Lead ePad SOIC

Media Type:
<blank>= 95/Tube (SOIC option only)
-TR = 2500/Reel (SOIC option only)
-TR = 5000/Reel (VDFN option only)
-T5 = 500/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

Examples:

a)	MIC5283YME:	MIC5283, Adjustable Output Voltage, –40°C to +125°C Temp. Range, 8-Lead ePad SOIC, 95/Tube
b)	MIC5283-3.3YME:	MIC5283, 3.3V Output Voltage, –40°C to +125°C Temp. Range, 8-Lead ePad SOIC, 95/Tube
c)	MIC5283-5.0YME-TR:	MIC5283, 5.0V Output Voltage, –40°C to +125°C Temp. Range, 8-Lead ePad SOIC, 2500/Reel
b)	MIC5283YML:	MIC5283, Adjustable Output Voltage, –40°C to +125°C Temp. Range, 8-Lead VDFN, 95/Tube
c)	MIC5283-3.3YML-TR:	MIC5283, 3.3V Output Voltage, –40°C to +125°C Temp. Range, 8-Lead VDFN, 5000/Reel
b)	MIC5283-5.0YML-T5:	MIC5283, 5.0V Output Voltage, –40°C to +125°C Temp. Range, 8-Lead VDFN, 500/Reel

NOTES:

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