MIC7401

Configurable PMIC, Five-Channel Buck Regulator plus One-Boost with HyperLight Load®, I²C Control, and Enable

General Description

The MIC7401 is a powerful, highly-integrated, configurable, power-management IC (PMIC) featuring five synchronous buck regulators, one boost regulator, and high-speed I²C interface with an internal EEPROM.

The device offers two distinct modes of operation "stand-by mode" and "normal mode" intended to provide an energy optimized solution suitable for portable handheld, and infotainment applications.

In normal mode, the programmable switching converters can be configured to support a variety of features, including start-up sequencing, timing, soft-start ramp, output voltage levels, current-limit levels, and output discharge for each channel.

In stand-by mode the PMIC can configured in a low power state by either disabling an output or by changing the output voltage to a lower level. Independent exit from stand-by mode can be achieved either by I²C communication or the external STBY pin.

The device has five synchronous buck regulators with high-speed adaptive on-time control supporting even the challenging ultra-fast transient requirement for core supplies. The one boost regulator provides a flash-memory programming supply that delivers up to 200mA of output current. The boost is equipped with an output disconnect switch that opens if a short-to-ground fault is detected.

An internal EEPROM enables a single-chip solution across many platforms by allowing the designer to customize the PMIC for their design. Modifications can be made without the need to re-approve a new PMIC, saving valuable design resources and time.

All switchers provide light-load efficiency with HyperLight Load® mode for buck and PFM mode for boost. An additional benefit of this proprietary architecture is very-low output ripple voltage throughout the entire load range with the use of small output capacitors. The MIC7401 is designed for use with a small inductors (down to 0.47µH for buck, 1.5µH for boost), and an output capacitor as small as 10µF for buck, enabling a total solution size of 12mm × 8.5mm and less than 1mm height on top layer.

The datasheet and other support documentation can be found on Micrel's web site at: www.micrel.com.

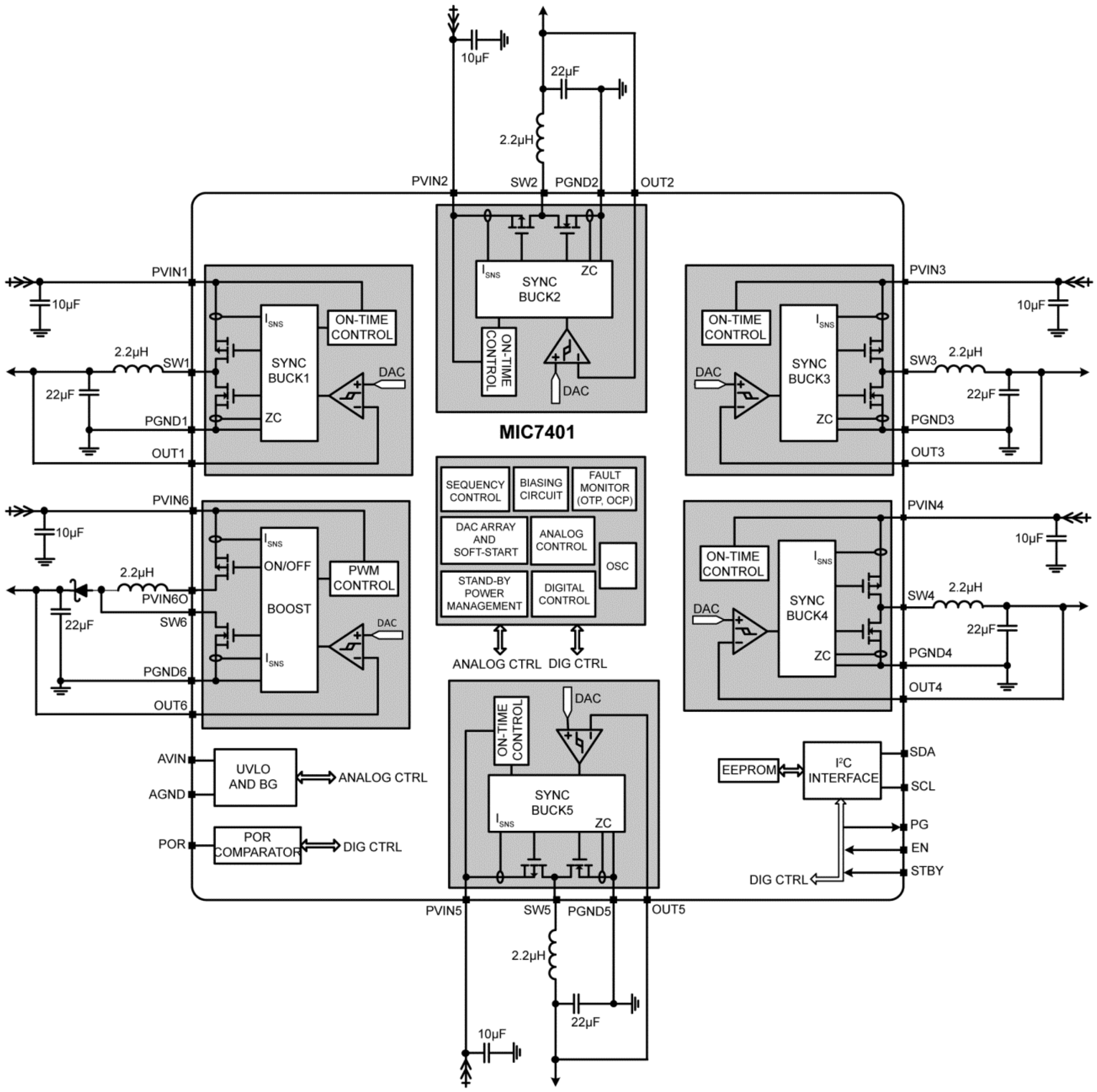
Features

- Input voltage: 2.4V to 5.5V
- Five independent synchronous bucks up to 3A
- One independent non-synchronous boost 200mA
- **200µA quiescent current (all regulators on)**
- **5µA typical shutdown current**
- 93% peak buck efficiency, 85% typical efficiency at 1mA
- **Dual power mode: stand-by and normal mode**
- I²C interface up to 3.4MHz
- **I²C on-the-fly EEPROM programmability, featuring:**
  - Buck and boost output voltage scaling
  - Power-on-Reset (PoR) threshold and delay
  - Power-up sequencing/sequencing delay
  - Buck and boost current limit
  - Buck and boost pull-down when disabled
  - Individual ON, OFF, and standby modes
  - Soft-start and global power-good masking
- 23µA buck typical quiescent current
- 70µA boost typical quiescent current
- 1.5% output accuracy over temperature/line/load
- 2.0MHz boost switching frequency
- 1.3MHz buck operation in continuous mode
- Ultra-fast buck transient response
- **12mm × 8.5mm × 1.25mm solution size (top layer)**
- Thermal-shutdown and current-limit protection
- 36-pin 4.5mm × 4.5mm × 0.85mm FQFN package (0.4mm pitch)
- –40°C to +125°C junction temperature range

Applications

- Client and enterprise solid state drives (SSD)
- Consumer and in-vehicle infotainment devices
- Multimedia devices
- Portable handheld devices
- Security camera
- Gaming machines
- Service provider gateways

Typical Application



Ordering Information

Part Number	Marking	Output Voltages	Features	Package[1]	Lead Finish
MIC7401YFL	7401 YWWS	1.8V, 1.1V, 1.8V 1.05V, 1.25V, 12V	STBY – Active Low Falling Edge (DEFAULT)	36-Pin 4.5mm × 4.5mm FQFN	Pb-Free
MIC7401-XXXXYFL [2]	X X 7401 X YYWW X	Configurable	Configurable	36-Pin 4.5mm × 4.5mm FQFN	Pb-Free

Notes:

1. GREEN, RoHs-compliant package. Lead finish is Matte Tin. Mold compound is Halogen Free.
2. Configurable options available upon request. Contact Marketing.

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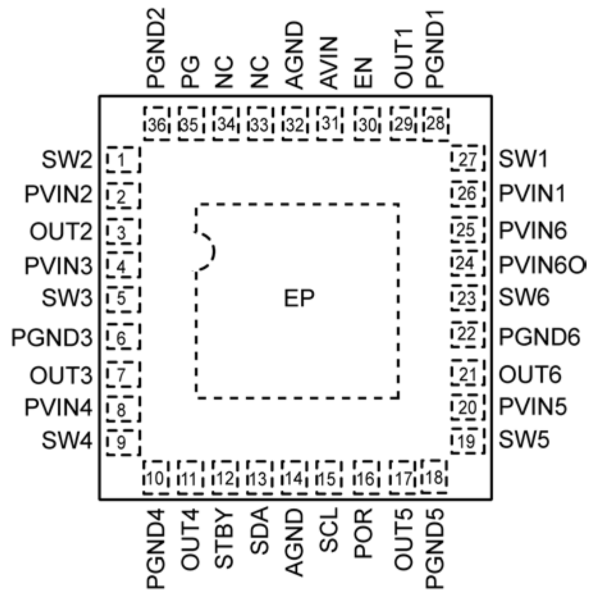
Pin Configuration



36-Pin 4.5mm × 4.5mm FQFN (FL)
(Top View)

Pin Description

Pin Number	Pin Name	Description
1	SW2	Switch Pin 2 (Output): Inductor connection for the synchronous step-down regulator. Connect the inductor between the output capacitor and the SW2 pin.
2	PVIN2	Power Supply Voltage 2 (Input): Input supply to the source of the internal high-side P-channel MOSFET. An input capacitor between PVIN2 and the power ground PGND2 pin is required and to be placed as close as possible to the IC.
3	OUT2	Output Voltage Sense 2 (Input): This pin is used to sense the output voltage. Connect OUT2 as close to the output capacitor as possible to sense output voltage. Also provides the path to discharge the output through an internal 90Ω resistor when disabled. This pull-down feature is programmed through the PULLD[x] register.
4	PVIN3	Power Supply Voltage 3 (Input): Input supply to the source of the internal high-side P-channel MOSFET. An input capacitor between PVIN3 and the power ground PGND3 pin is required and to be placed as close as possible to the IC.
5	SW3	Switch Pin 3 (Output): Inductor connection for the synchronous step-down regulator. Connect the inductor between the output capacitor and the SW3 pin.
6	PGND3	Power Ground 3: The power ground for the synchronous buck converter power stage. The PGND pin connects to the sources of the internal low-side N-Channel MOSFET, the negative terminals of input capacitors, and the negative terminals of output capacitors.
7	OUT3	Output Voltage Sense 3 (Input): This pin is used to sense the output voltage. Connect OUT3 as close to the output capacitor as possible to sense output voltage. Also provides the path to discharge the output through an internal 90Ω resistor when disabled. This pull-down feature is programmed through the PULLD[x] register.
8	PVIN4	Power Supply Voltage 4 (Input): Input supply to the source of the internal high-side P-channel MOSFET. An input capacitor between PVIN4 and the power ground PGND4 pin is required and to be placed as close as possible to the IC.

Pin Description (Continued)

Pin Number	Pin Name	Description
9	SW4	Switch Pin 4 (Output): Inductor connection for the synchronous step-down regulator. Connect the inductor between the output capacitor and the SW4 pin.
10	PGND4	Power Ground 4: The power ground for the synchronous buck converter power stage. The PGND pin connects to the source of the internal low-side N-Channel MOSFET, the negative terminals of input capacitors, and the negative terminals of output capacitors.
11	OUT4	Output Voltage Sense 4 (Input): This pin is used to sense the output voltage. Connect the OUT4 as close to the output capacitor as possible to sense output voltage. Also provides the path to discharge the output through an internal 90Ω resistor when disabled. This pull-down feature is programmed through the PULLD[x] register.
12	STBY	Standby Reset (Input): Standby mode allows the total power consumption to be reduced by either lowering a supply voltage or turning it off. The IC can be placed in standby mode while operating in normal mode by a high-to-low transition (DEFAULT) on the STBY input. When this occurs, the STBY_MODEB bit will be set to logic "0". Either a low-to-high transition on the STBY pin or an I²C write command to the STBY_MODEB bit sets all of the regulators to their normal mode default settings. This pin can be driven with either a digital signal or open collector output. Do not let this pin float. Connect to ground or V_{IN}. A pull-down resistor of 100kΩ or less can also be used. There are both a high-to-low (DEFAULT) and low-to-high normal to standby trigger options available.
13	SDA	High-Speed Mode 3.4MHz I²C Data (Input/Output): This is an open drain, bidirectional data pin. Data is read on the rising edge of the SCL and data is clocked out on the falling edge of the SCL. External pull-up resistors are required.
14	AGND	Analog Ground: Internal signal ground for all low power circuits. Connect to ground plane for best operation.
15	SCL	High-Speed Mode 3.4MHz I²C Clock (Input): I²C serial clock line open drain input. External pull-up resistors are required.
16	POR	Power-on-Reset (Output): This is an open drain output that goes high after the POR delay time elapses. The POR delay time starts as soon as the AVIN pin voltage rises above the upper threshold set by the PORUP register. The POR output goes low without delay when AVIN falls below the lower threshold set by the PORDN register.
17	OUT5	Output Voltage Sense 5 (Input): This pin is used to sense the output voltage. Connect OUT5 as close to the output capacitor as possible to sense output voltage. Also provides the path to discharge the output through an internal 90Ω resistor when disabled. This pull-down feature is programmed through the PULLD[x] register.
18	PGND5	Power Ground 5: The power ground for the synchronous buck converter power stage. The PGND pin connects to the source of the internal low-side N-Channel MOSFET, the negative terminals of input capacitors, and the negative terminals of output capacitors.
19	SW5	Switch Pin 5 (Output): Inductor connection for the synchronous step-down regulator. Connect the inductor between the output capacitor and the SW5 pin.
20	PVIN5	Power Supply Voltage 5 (Input): Input supply to the source of the internal high-side P-channel MOSFET. An input capacitor between PVIN5 and the power ground PGND5 pin is required and to be placed as close as possible to the IC.
21	OUT6	Output Voltage 6 Sense (Input): This pin is used to sense the output voltage. Connect OUT6 as close to the output capacitor as possible to sense output voltage. Also provides the path to discharge the output through an internal programmable current source when disabled. This pull-down feature is programmed through the PULLD[x] register.
22	PGND6	Power Ground 6: The power ground for the boost converter power stage. The PGND pin connects to the source of the internal low-side N-Channel MOSFET, the negative terminals of input capacitors, and the negative terminals of output capacitors.
23	SW6	Switch Pin 6 (Input): Inductor connection for the boost regulator. Connect the inductor between the PVIN6O and SW6 pin.

Pin Description (Continued)

Pin Number	Pin Name	Description
24	PVIN6O	Power Supply Voltage 6 (Output): This pin is the output of the power disconnect switch for the boost regulator. When the boost regulator is on, an internal switch provides a current path for the boost inductor. In shutdown, an internal P-channel MOSFET is turned off and disconnects the boost output from the input supply. This feature eliminates current draw from the input supply during shutdown. An input capacitor between PVIN6O and the power ground PGND6 pin is required and place as close as possible to the IC.
25	PVIN6	Power Supply Voltage 6 (Input): Input supply to the internal disconnect switch.
26	PVIN1	Power Supply Voltage 1 (Input): Input supply to the source of the internal high-side P-channel MOSFET. An input capacitor between PVIN1 and the power ground PGND1 pin is required and to be placed as close as possible to the IC.
27	SW1	Switch Pin 1 (Output): Inductor connection for the synchronous step-down regulator. Connect the inductor between the output capacitor and the SW1 pin.
28	PGND1	Power Ground 1: The power ground for the synchronous buck converter power stage. The PGND pin connects to the source of the internal low-side N-Channel MOSFET, the negative terminals of input capacitors, and the negative terminals of output capacitors.
29	OUT1	Output Voltage Sense 1(Input): This pin is used to sense the output voltage remotely. Connect OUT1 as close to output capacitor as possible to sense output voltage. This feature also provides the path to discharge the output through an internal 90Ω resistor when disabled. The pull-down feature is programmed through the PULLD[x] register.
30	EN	Enable (input): A logic level control of both outputs. The EN pin is CMOS-compatible. Logic high = enable, logic low = shutdown. In the off state, supply current of the device is greatly reduced (typically 1µA). When the EN pin goes high, the start-up sequence is initiated. When EN goes low, all outputs are immediately turned off and the boost output (V_{OUT6}) is completely disconnected from the input voltage. The EN pin must be high for the I2C to communicate with the IC; otherwise, the IC cannot be programmed. Do not let this pin float. Connect to ground or V_{IN}. A pull-up resistor of 500kΩ can also be used
31	AVIN	Analog Voltage Supply (Input): The start-up sequence begins as soon as the AVIN pin voltage rises above the IC's UVLO upper threshold. The outputs do not turn off until AVIN pin voltage falls below the lower threshold limit. A 2.2µF ceramic capacitor from the AVIN pin to AGND pin must be placed next to the IC.
32	AGND	Analog Ground: Internal signal ground for all low power circuits. Connect directly to the layer 2 ground plane. Layer 2 is the point where all the PGNDs and AGND are connected. Do not connect PGND and AGND together on the top layer.
33	NC	No Connect. Must be left floating.
34	NC	No Connect. Must be left floating.
35	PG	Global Power Good (Output): This is an open drain output that is pulled high when all the regulator power good flags are high. If an output falls below the power good threshold or a thermal fault occurs, the global power good flag is pulled low. There is a falling edge de-glitch time of 50µs to prevent false triggering on output voltage transients. A power good mask feature programmed through the PGOOD_MASK[x] registers can be used to ignore a power good fault. When masked an individual power good fault will not cause the global power good output to de-assert. Do not connect the power good pull-up resistor to a voltage higher than AV_{IN}.
36	PGND2	Power Ground 2: The power ground for the synchronous buck converter power stage. The PGND pin connects to the source of the internal low-side N-Channel MOSFET, the negative terminals of input capacitors, and the negative terminals of output capacitors.
EP	ePad	Exposed Pad: Must be connected to the GND plane for full output power to be realized.

Absolute Maximum Ratings[3]

Supply Voltages ($PV_{IN[1-6]}$) .... -0.3V to 6V
Analog Supply Voltage (AV_{IN}) .... -0.3V to 6V
Buck Output Voltages ($V_{OUT[1-5]}$) .... -0.3V to 6V
Boost Output Voltage (V_{OUT6}) .... -0.3V to 20V
Buck Switch Voltages ($V_{SW[1-5]}$). .... -0.3V to 6V
Boost Switch Voltage (V_{SW6}). .... -0.3V to 20V
Power Good Voltage (V_{PG}) .... -0.3V to AV_{IN}
Power-On Reset Output (V_{POR}) .... -0.3V to 6V
Enable Voltage (V_{EN}) .... -0.3V to 6V
Standby Voltage (V_{STBY}) .... -0.3V to 6V
I²C IO (V_{SDA}, V_{SCL}) .... -0.3V to AV_{IN}
AGND to PGND[1-6] .... -0.3V to 0.3V
Ambient Storage Temperature (Ts) ....-65°C to +150°C
ESD HBM Rating[6] 2kV
ESD MM Rating.................................. 200V

Operating Ratings[4]

Input Voltage ($PV_{IN[1-6]}$).................................. 2.4V to 5.5V
Analog Input Voltage (AV_{IN}) .... 2.4V to 5.5V
Buck Output Voltage Range ($V_{OUT[1-5]}$) .... 0.8V to 3.3V
Boost Output Voltage Range (V_{OUT6}) .... 7V to 14V
Power Good Voltage (V_{PG})..................................0V to AV_{IN}
Power-On Reset Output (V_{POR})..................................0V to AV_{IN}
Enable Voltage (V_{EN})..................................0V to AV_{IN}
Standby Voltage (V_{STBY})..................................0V to AV_{IN}
I²C IO (V_{SDA}, V_{SCL}) ....0V to AV_{IN}
Junction Temperature (T_J)[5] ....-40°C to +125°C
Junction Thermal Resistance
4.5mm × 4.5mm FQFN-36 (θ_{JA}) ....30°C/W

Electrical Characteristics[7]

$V_{IN} = AV_{IN} = PV_{IN(1-6)} = 5.0V$; $V_{OUT1} = 1.8V$; $V_{OUT2} = 1.1V$; $V_{OUT3} = 1.8V$; $V_{OUT4} = 1.05V$; $V_{OUT5} = 1.25V$; $V_{OUT6} = 12V$ (refer to the *Evaluation Board Schematic* for component values). T_A = 25°C, unless otherwise noted. **Bold** values indicate –40°C ≤ TJ ≤ +125°C.

Parameter	Conditions	Min.	Typ.	Max.	Unit
Input Supply (VIN)					
Input Voltage Range (AV_{IN}, $PV_{IN[1-6]}$)		**2.4**		**5.5**	V
Operating Quiescent Current into AV_{IN} [8, 9]	V_{IN} = 5.0V; I_{OUT} = 0A		200	240	µA
Operating Quiescent Current into PV_{IN} [8]	V_{IN} = 5.0V; I_{OUT} = 0A		0.3	1	µA
Shutdown Current into (PV_{IN} + AV_{IN})	V_{IN} = 5.0V; V_{EN} = 0V		5		µA
Undervoltage Lockout Threshold	AV_{IN} Rising	**2.15**	2.25	**2.35**	V
Undervoltage Lockout Hysteresis			150		mV
Standby Input (STBY)					
Logic Level High		**1.2**			V
Logic Level Low				**0.4**	V
Bias Current into Pin	$V_{STBY} = V_{IN}$			200	nA
Bias Current out of Pin	V_{STBY} = 0V			200	nA
Rising/Falling Edge Reset Deglitch			100		µs

Notes:

3. Absolute maximum ratings indicate limits beyond which damage to the component may occur.
4. The device is not guaranteed to function outside its operating rating.
5. The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(Max)}$, the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown.
6. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5kΩ in series with 100pF.
7. Specification for packaged product only.
8. Tested in a non-switching configuration.
9. When all outputs are configured to the minimum programmable voltage.

Electrical Characteristics[7] (Continued)

$V_{IN} = AV_{IN} = PV_{IN(1-6)} = 5.0V$; $V_{OUT1} = 1.8V$; $V_{OUT2} = 1.1V$; $V_{OUT3} = 1.8V$; $V_{OUT4} = 1.05V$; $V_{OUT5} = 1.25V$; $V_{OUT6} = 12V$ (refer to the *Evaluation Board Schematic* for component values). $T_A = 25°C$, unless otherwise noted. **Bold** values indicate –40°C ≤ TJ ≤ +125°C.

Parameter	Conditions	Min.	Typ.	Max.	Unit
Enable Input (EN)					
Logic Level High	V_{EN} Rising, Regulator Enabled	**1.2**			V
Logic Level Low	V_{EN} Falling, Regulator Shutdown			**0.4**	V
Bias Current Into Pin	$V_{EN} = V_{IN}$			200	nA
Bias Current Out of Pin	$V_{EN} = 0V$			200	nA
Power-On-Reset (POR) Comparator					
POR Upper Comparator Range	AV_{IN} Rising	2.646	2.7	2.754	V
POR Lower Comparator Range	AV_{IN} Falling	2.548	2.6	2.652	V
Power Reset Output (POR) and Timer					
POR Delay		18	20	22	ms
POR Deglitch Delay	AV_{IN} Falling		50		µs
POR Output Low Voltage	$I_{POR} = 10mA$ (sinking)		75	400	mV
POR Leakage Current	$V_{POR} = 5.5V$			200	nA
Global Power Good Output (PG)					
Buck Power Good Threshold Voltage	$V_{OUT[1-5]}$ Rising	87	91	95	$\%V_{OUT}$
Buck Hysteresis [10]	$V_{OUT[1-5]}$ Falling		4		$\%V_{OUT}$
Boost Power Good Threshold Voltage	$V_{OUT[6]}$ Rising	87	91	95	$\%V_{OUT}$
Boost Hysteresis [10]	$V_{OUT[6]}$ Falling		380		mV
Power Good Output Low Voltage	$I_{PG} = 10mA$ (sinking)		75	400	mV
Power Good Leakage Current	$V_{PG} = 5.5V$		0.01	200	nA
Power Good De-Glitch Delay	$V_{OUT[1-6]}$ Falling		100		µs
Output Sequencing Delay [10]		0.96	1	1.04	ms
Thermal Protection					
Thermal Shutdown	T_J Rising		160		°C
Thermal Hysteresis			20		°C

Note:

10. Guaranteed by design.

Electrical Characteristics[7] (Continued)

V_{IN} = AV_{IN} = $PV_{IN(1-6)}$ = 5.0V; V_{OUT1} = 1.8V; V_{OUT2} = 1.1V; V_{OUT3} = 1.8V; V_{OUT4} = 1.05V; V_{OUT5} = 1.25V; V_{OUT6} = 12V (refer to the *Evaluation Board Schematic* for component values). T_A = 25°C, unless otherwise noted. **Bold** values indicate –40°C ≤ TJ ≤ +125°C.

Parameter	Conditions	Min.	Typ.	Max.	Unit
Synchronous Buck (V_{OUT1} - V_{OUT5})					
Buck Output Voltage Accuracy (OUT[1-5])					
Typical Output Voltage 1 Accuracy [11]	Includes Load, Line and Reference	**–1.5%**		**1.5%**	%
Typical Output Voltage 2 Accuracy [11]	Includes Load, Line and Reference	**–1.5%**		**1.5%**	%
Typical Output Voltage 3 Accuracy [11]	Includes Load, Line and Reference	**–1.5%**		**1.5%**	%
Typical Output Voltage 4 Accuracy [11]	Includes Load, Line and Reference	**–1.5%**		**1.5%**	%
Typical Output Voltage 5 Accuracy [11]	Includes Load, Line and Reference	**–1.5%**		**1.5%**	%
Output Voltage 1 Accuracy [11]		**–1%**		**1%**	%
Output Voltage 2 Accuracy [11]		**–1%**		**1%**	%
Output Voltage 3 Accuracy [11]		**–1%**		**1%**	%
Output Voltage 4 Accuracy [11]		**–1%**		**1%**	%
Output Voltage 5 Accuracy [11]		**–1%**		**1%**	%
Load Regulation	I_{OUT} = 10mA to $I_{OUT(MAX)}$		0.1		%
Line Regulation	V_{IN} = 3.3V to 5.0V		0.05		%
Buck Soft-Start					
Soft-Start (1-5) LSB [10, 12]		3.84	4	4.16	µs/step
Buck Internal MOSFETs					
High-Side On-Resistance	V_{IN} = 3.3V; $I_{SW[1-5]}$ = 200mA		54		mΩ
High-Side On-Resistance	V_{IN} = 5.0V; $I_{SW[1-5]}$ = 200mA		40		mΩ
Low-Side On-Resistance	V_{IN} = 3.3V; $I_{SW[1-5]}$ = -200mA		37		mΩ
Low-Side On-Resistance	V_{IN} = 5.0V; $I_{SW[1-5]}$ = -200mA		30		mΩ
Output Pull-Down Resistance	$V_{SW[1-5]}$ = 0V	75	90	200	Ω
Buck Controller Timing					
Fixed On-Time [13]	V_{IN} = 3.3; V_{OUT} = 1.0V; I_{OUT} = 1.0A		220		ns
Minimum OFF-Time			80		ns

Note:

11. Not tested in a closed loop configuration.
12. The soft-start time is calculated using the following equation: $t_{softstart} = [(V_{OUT\_PROGRAM} – 0.15)/0.05 +1) \times t_{RAMP}$.
13. Buck frequency is calculated using the following equation $f_{SW} = (V_{OUT}/V_{IN}) \times (1/t_{ON})$.

Electrical Characteristics[7] (Continued)

V_{IN} = AV_{IN} = $PV_{IN(1-6)}$ = 5.0V; V_{OUT1} = 1.8V; V_{OUT2} = 1.1V; V_{OUT3} = 1.8V; V_{OUT4} = 1.05V; V_{OUT5} = 1.25V; V_{OUT6} = 12V (refer to the *Evaluation Board Schematic* for component values). T_A = 25°C, unless otherwise noted. **Bold** values indicate –40°C ≤ TJ ≤ +125°C.

Parameter	Conditions	Min.	Typ.	Max.	Unit
Buck Current Limit (OUT1-OUT5)					
Buck 1 Current Limit Threshold	See Table 25 for I_{PROG} Settings	3.075	4.1	5.125	A
Buck 2 Current Limit Threshold	See Table 25 for I_{PROG} Settings	3.075	4.1	5.125	A
Buck 3 Current Limit Threshold	See Table 26 for I_{PROG} Settings	3.075	4.1	5.125	A
Buck 4 Current Limit Threshold	See Table 26 for I_{PROG} Settings	4.88	6.1	7.32	A
Buck 5 Current Limit Threshold	See Table 27 for I_{PROG} Settings	3.075	4.1	5.125	A
Gross High-Side Current Limit [1-5]	With Respect to Buck [x] Current Limit		150		%
Zero Cross Threshold	Zero crossing detector		0		mV
Boost (V_{OUT6})					
Boost Output Voltage (V_{OUT6})					
Typical Output Voltage Accuracy [11]	Includes Load, Line, and Reference	**-1.5%**		**1.5%**	%
Output Voltage Accuracy [11]		**-1%**		**1%**	%
Load Regulation	I_{OUT6} = 1.0mA to 200mA		0.2		%
Line Regulation	V_{IN} = 2.4V to 5.5V; I_{OUT6} = 10mA		0.2		%
V_{OUT6} Discharge Current	V_{IN} = 3.3V; V_{OUT6} = 12V	111	148	185	mA
Boost Soft-Start Step Duration					
Soft-Start 6 LSB [10, 12]		3.84	4	4.16	µs/step
Boost Internal MOSFETs					
Low-Side On-Resistance	V_{IN} = 3.3V; I_{SW1} = –100mA		160		mΩ
Low-Side On-Resistance	V_{IN} = 5.0V; I_{SW1} = –100mA		140		mΩ
Boost Disconnect MOSFETs					
Disconnect Switch On-Resistance	I_{PVIN6O} = 100mA; V_{IN} = 3.3V		90		mΩ
Disconnect Switch Current Limit			5		A
Boost Switching Frequency					
Switching Frequency (PWM Mode)		1.92	2	2.08	MHz
Minimum Duty Cycle		35	40	45	%
Maximum Duty Cycle		80	85	90	%
Boost Current Limit					
NMOS Current-Limit Threshold			2.24		A

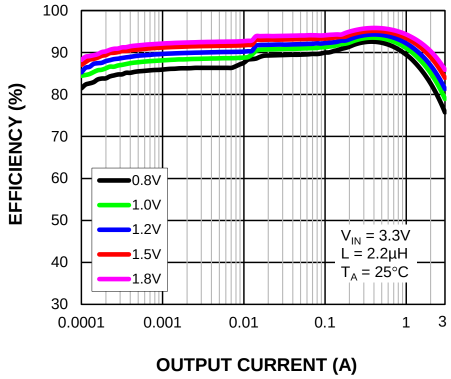
Electrical Characteristics[7] (Continued)

V_{IN} = AV_{IN} = $PV_{IN(1-6)}$ = 5.0V; V_{OUT1} = 1.8V; V_{OUT2} = 1.1V; V_{OUT3} = 1.8V; V_{OUT4} = 1.05V; V_{OUT5} = 1.25V; V_{OUT6} = 12V (refer to the *Evaluation Board Schematic* for component values). T_A = 25°C, unless otherwise noted. **Bold** values indicate –40°C ≤ TJ ≤ +125°C.

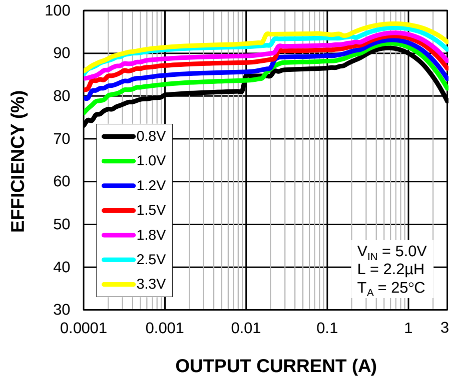
Parameter	Conditions	Min.	Typ.	Max.	Unit
I²C Interface					
I²C Interface (SCL, SDA)					
Low Level Input Voltage				**0.4**	V
High Level Input Voltage		**1.2**			V
High Level Input Current		–200	0.01	200	nA
Low Level Input Current		–200	0.01	200	nA
SDA Pull-Down Resistance			20		Ω
SDA Logic 0 Output Voltage	I_{SDA} = 3mA			**0.4**	V
CLK, DATA Pin Capacitance			0.7		pF
I²C Interface Timing[10]					
SCL Clock Frequency	Standard Mode			**100**	kHz
	Fast Mode			**400**	kHz
	High-Speed Mode[10]			**3.4**	MHz

Typical Characteristics

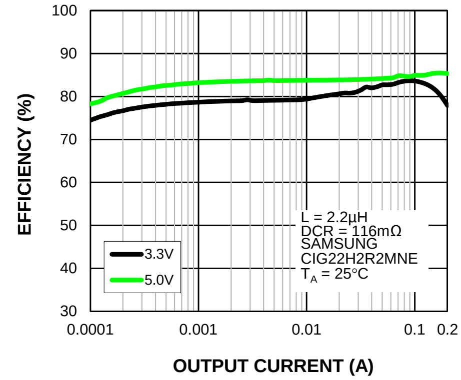
Buck Efficiency (LDCR = 0mΩ) vs. Output Current



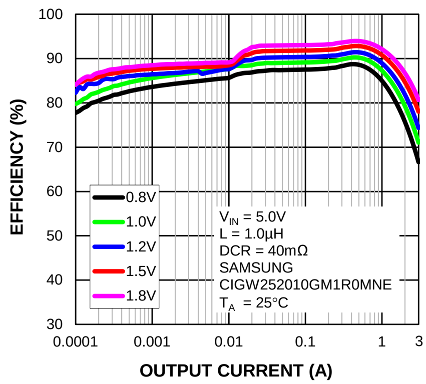
Buck Efficiency (LDCR = 0mΩ) vs. Output Current



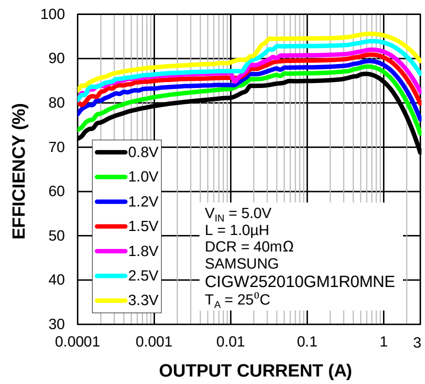
Boost Efficiency (12V) vs. Output Current



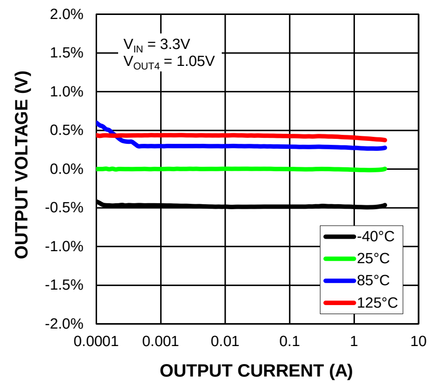
Buck Efficiency (LDCR = 40mΩ) vs. Output Current



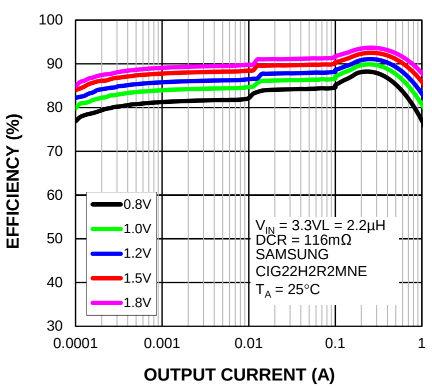
Buck Efficiency (LDCR = 40mΩ) vs. Output Current



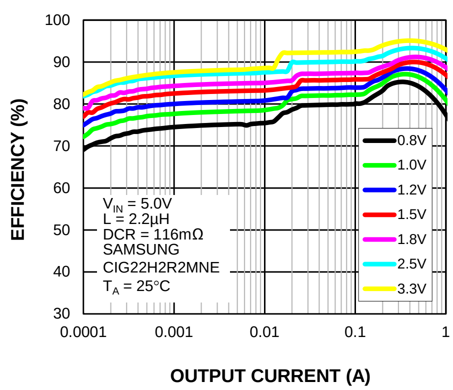
Output Voltage vs. Output Current



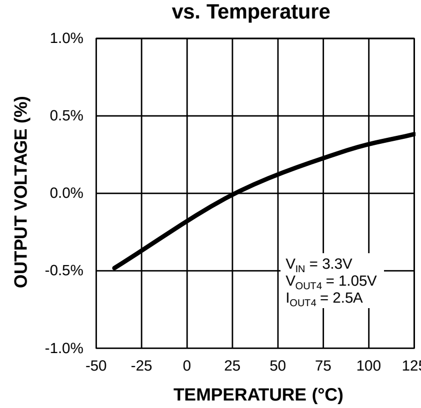
Buck Efficiency (LDCR = 116mΩ) vs. Output Current



Buck Efficiency (LDCR = 116mΩ) vs. Output Current

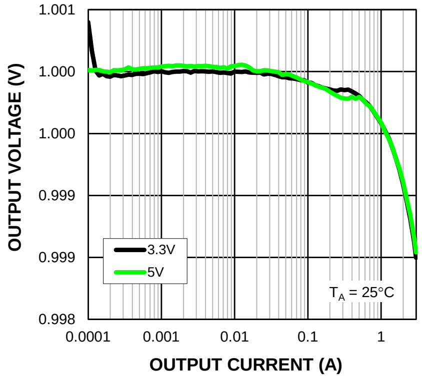


Output Voltage vs. Temperature

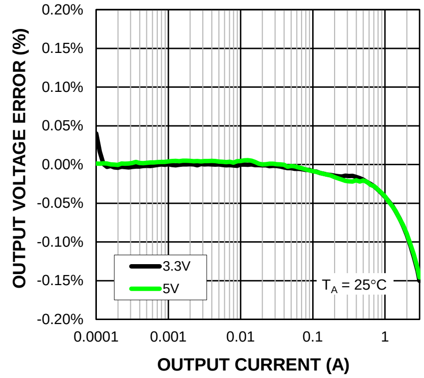


Typical Characteristics (Continued)

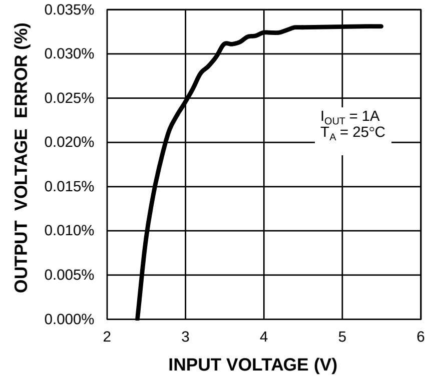
Buck Output Voltage (1.0V) vs. Output Current



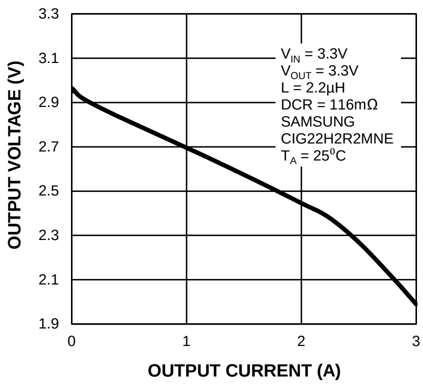
Buck Output Voltage Regulation vs. Output Current



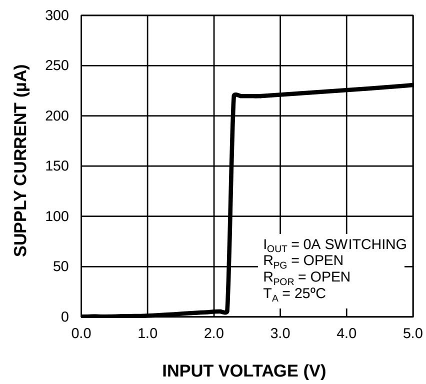
Buck Line Regulation vs. Input Voltage



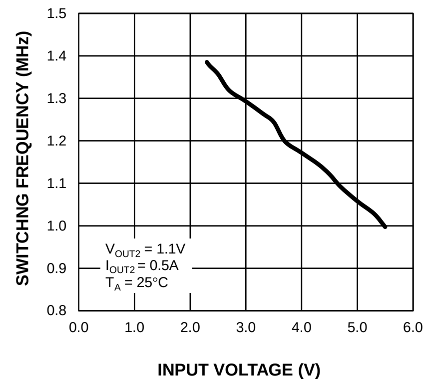
Dropout Output Voltage vs. Output Current



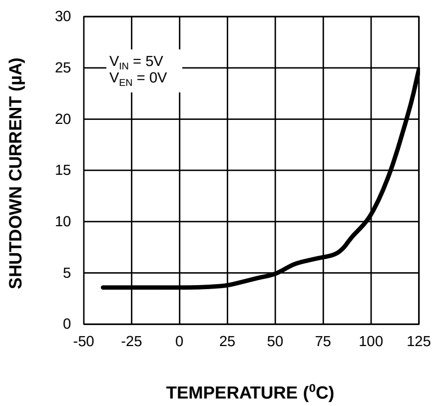
V_{IN} Operating Supply Current vs. Input Voltage



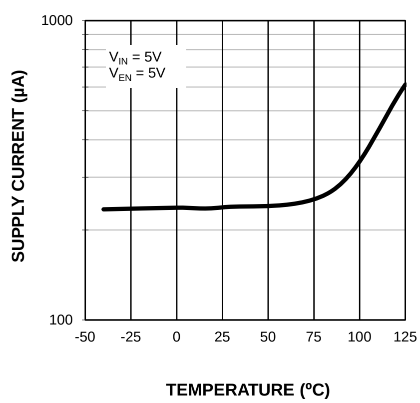
Buck 2 Switching Frequency vs. Input Voltage



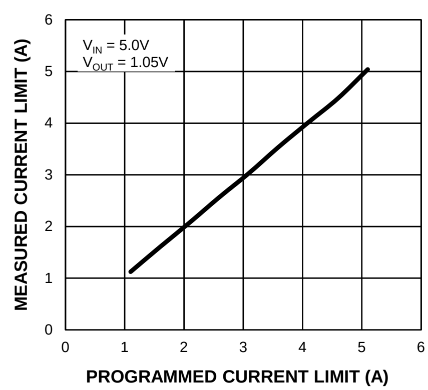
V_{IN} Shutdown Supply Current vs. Temperature



V_{IN} Supply Current vs. Temperature

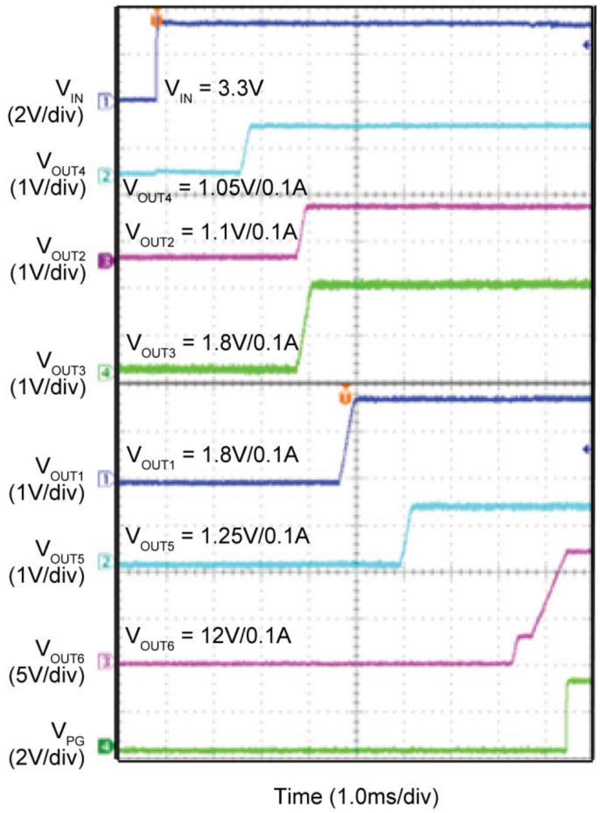


Programmed Current Limit vs. Measured Current Limit

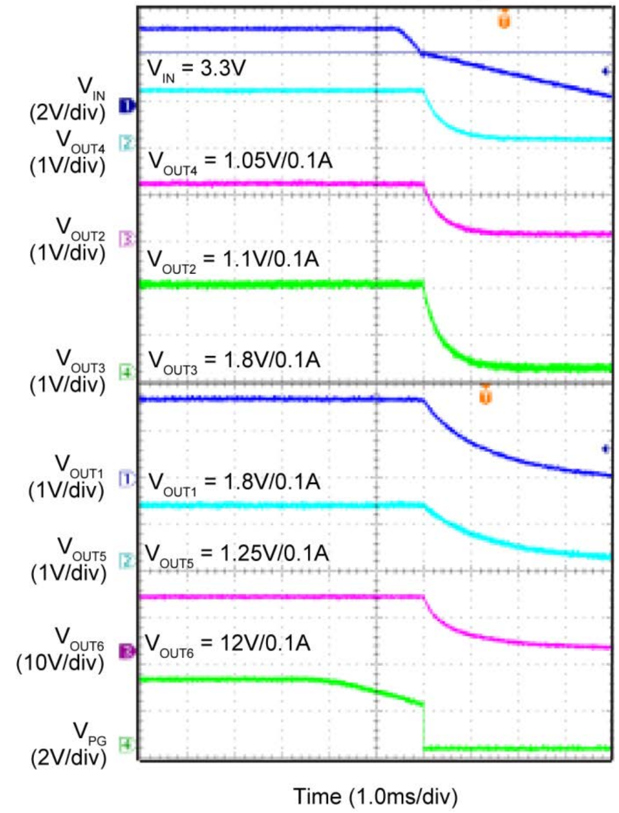


Functional Characteristics

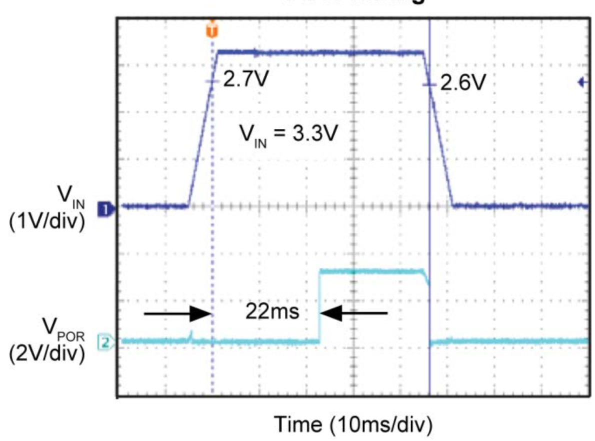
Hot Plug – Rising V_{IN}



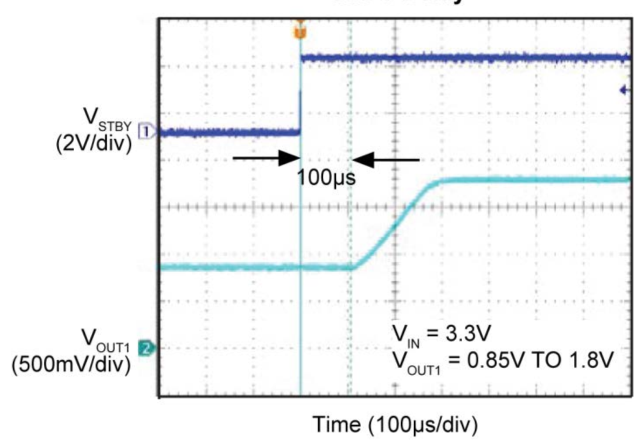
Unplug – Falling V_{IN}



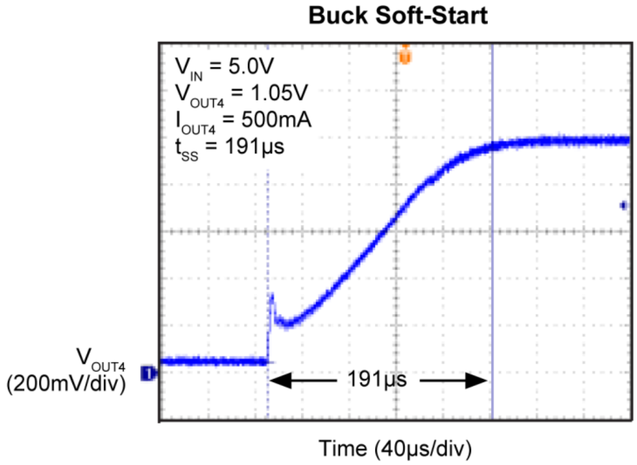
POR Timing

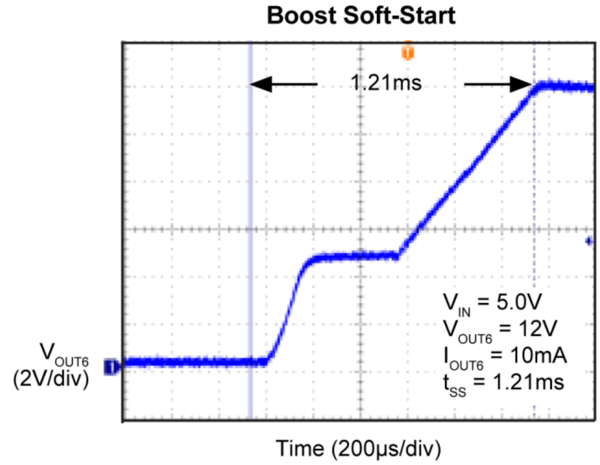


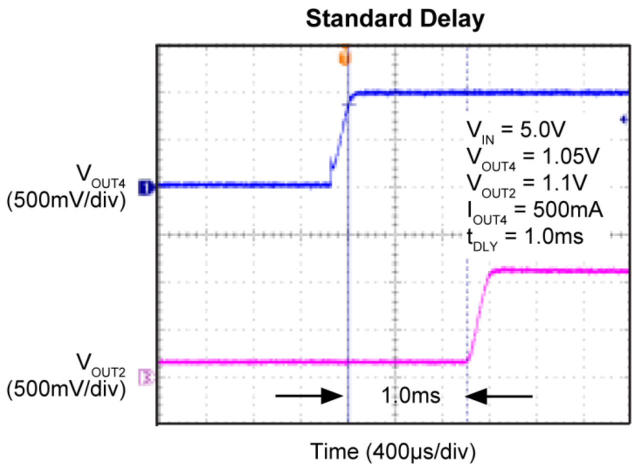
STBY Delay

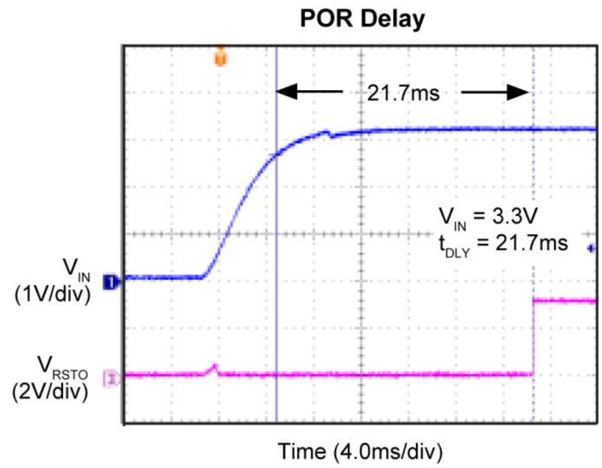


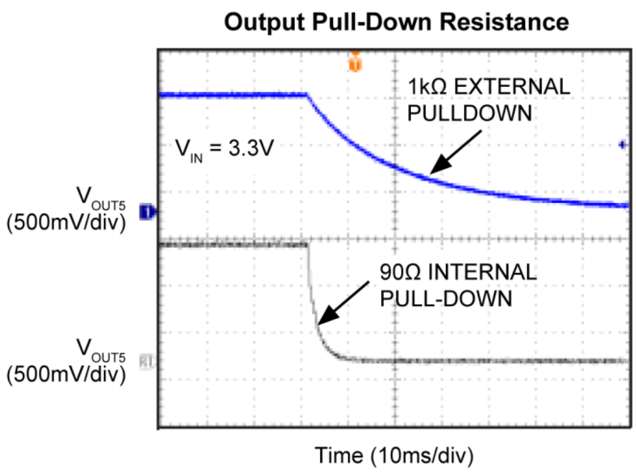
Functional Characteristics (Continued)





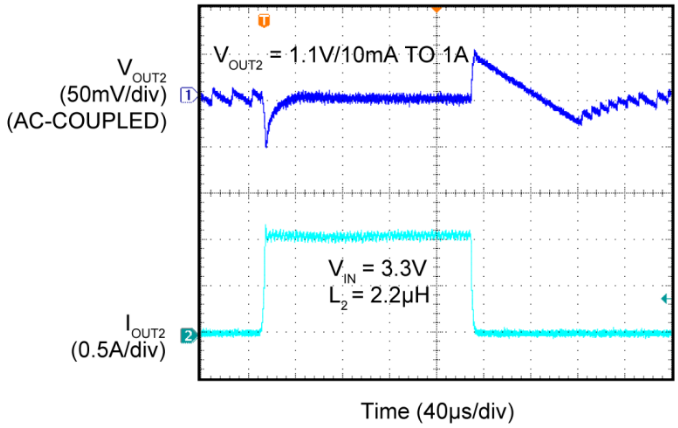




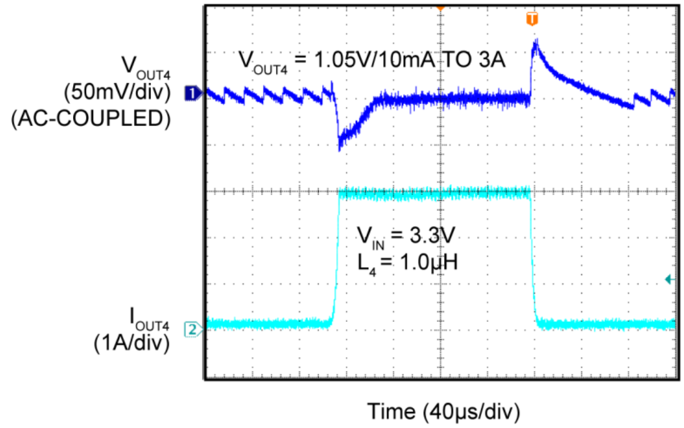


Functional Characteristics (Continued)

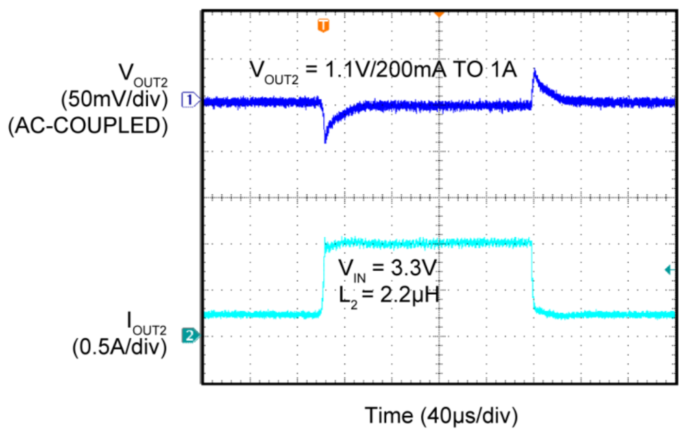
Buck 2 Load Transient – 10mA to 1A



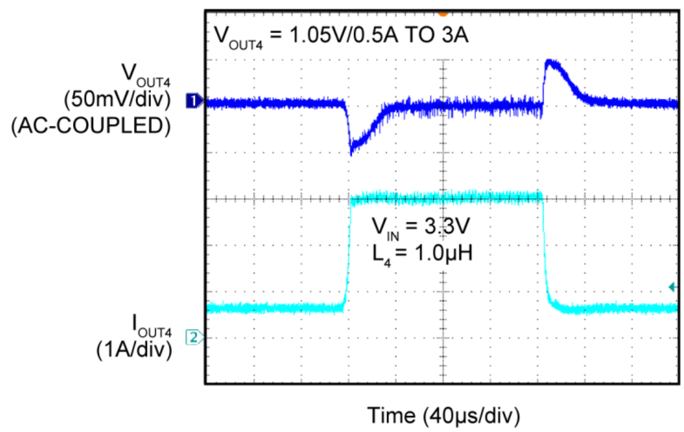
Buck 4 Load Transient – 10mA to 3A



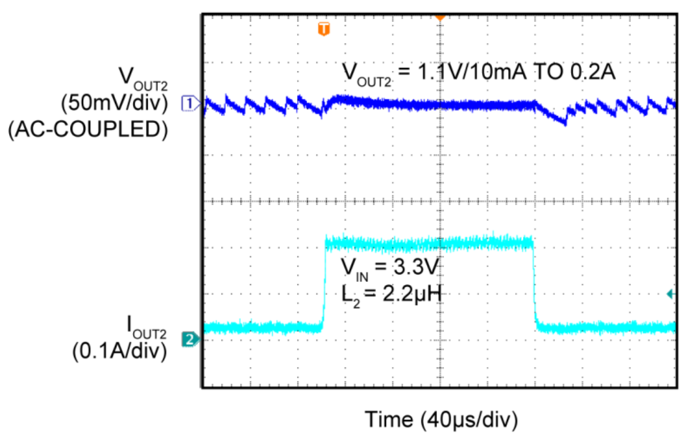
Buck 2 Load Transient – 200mA to 1A



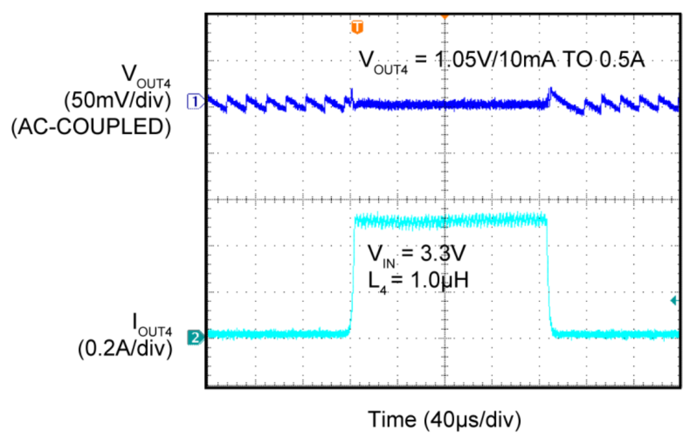
Buck 4 Load Transient – 0.5A to 3A



Buck 2 Load Transient – 10mA to 0.2A

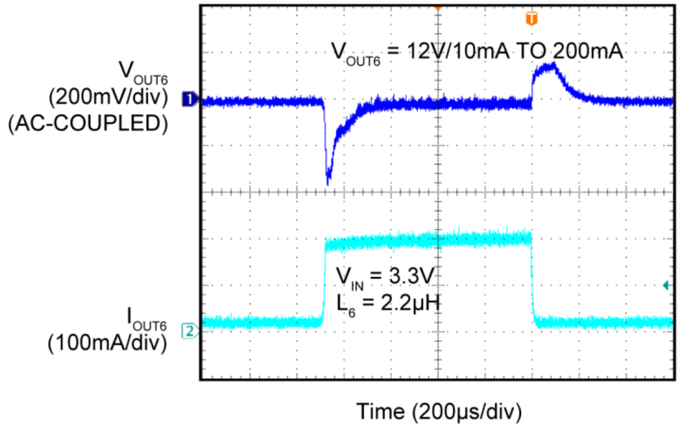


Buck 4 Load Transient – 10mA to 0.5A

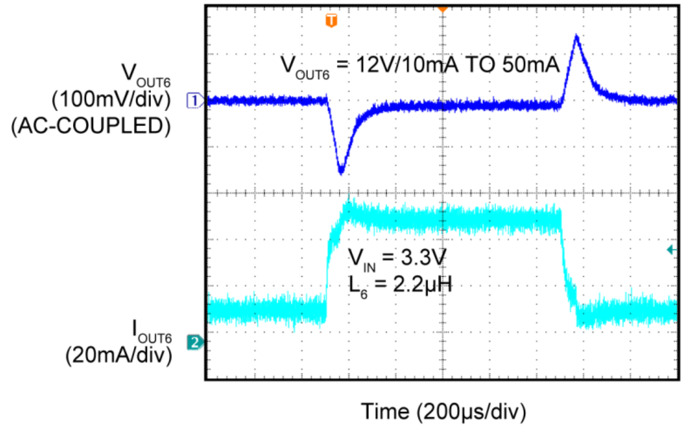


Functional Characteristics (Continued)

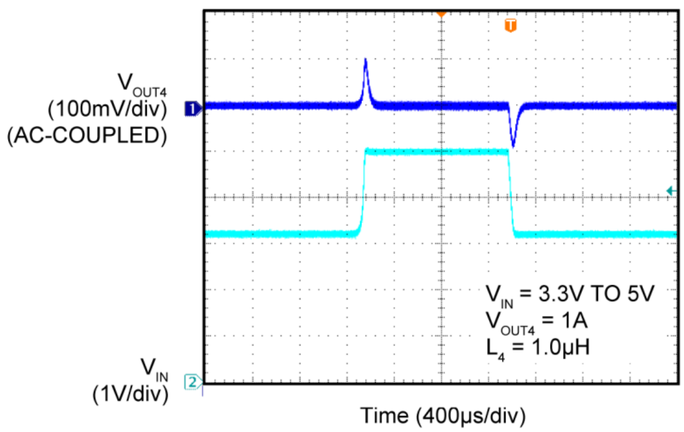
Boost 6 Load Transient – 10mA to 200mA



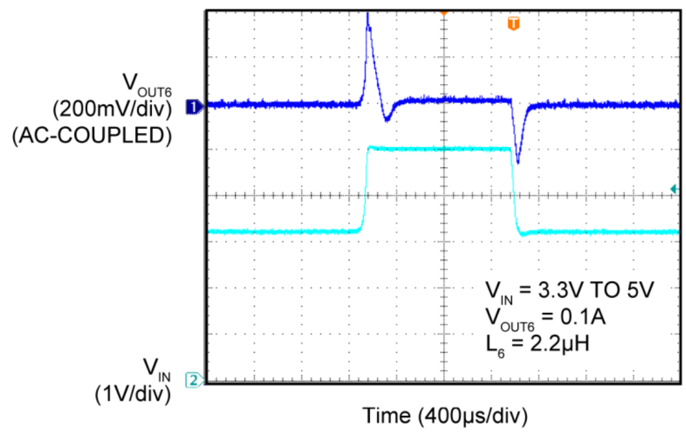
Boost 6 Load Transient – 10mA to 50mA



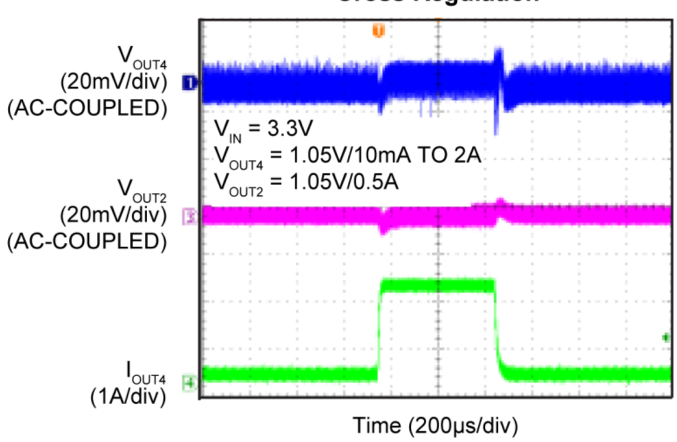
Buck 4 Line Transient – 3.3V to 5.0V



Boost 6 Line Transient – 3.3V to 5.0V

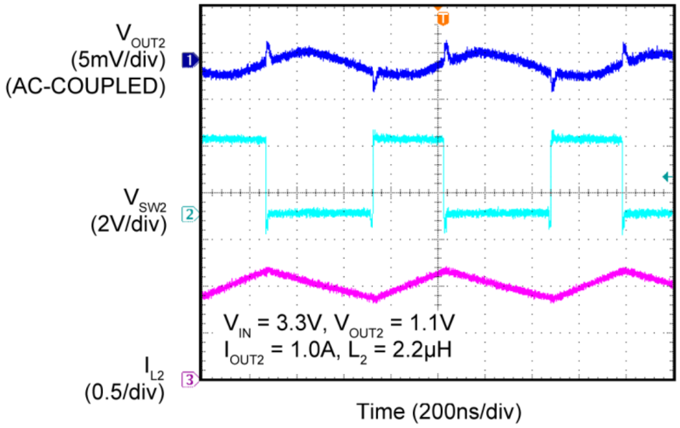


Cross Regulation

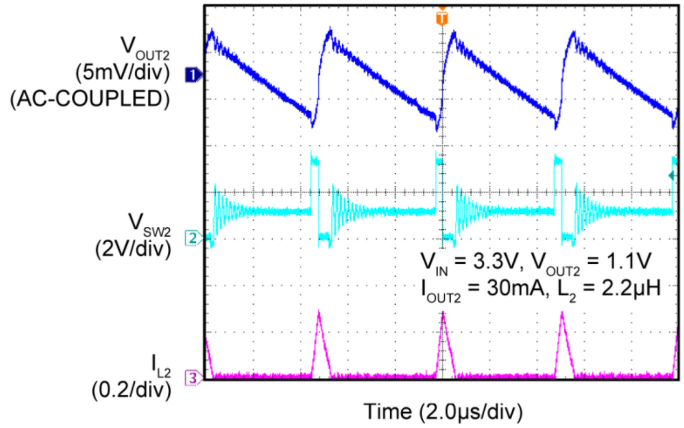


Functional Characteristics (Continued)

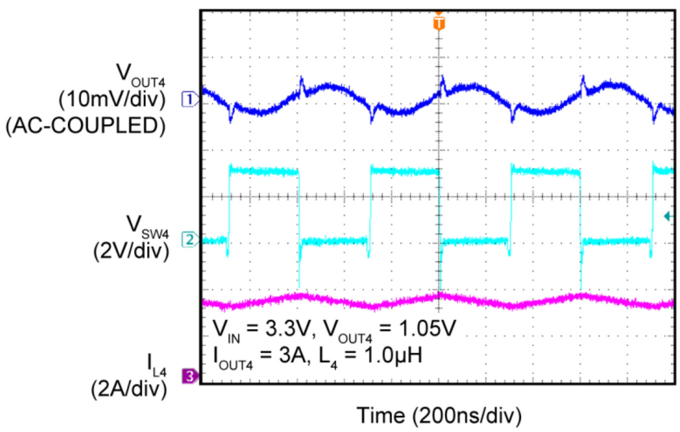
Buck 2 PWM Switching Waveforms



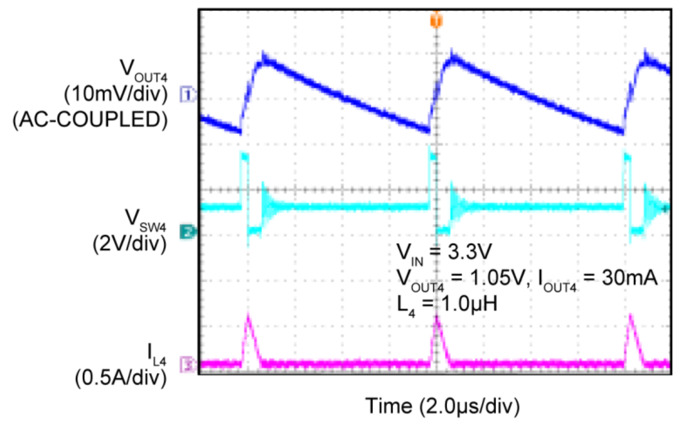
Buck 2 PFM Switching Waveforms



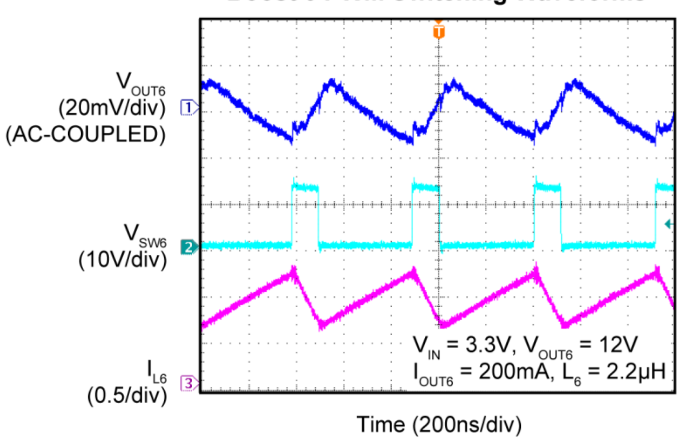
Buck 4 PWM Switching Waveforms



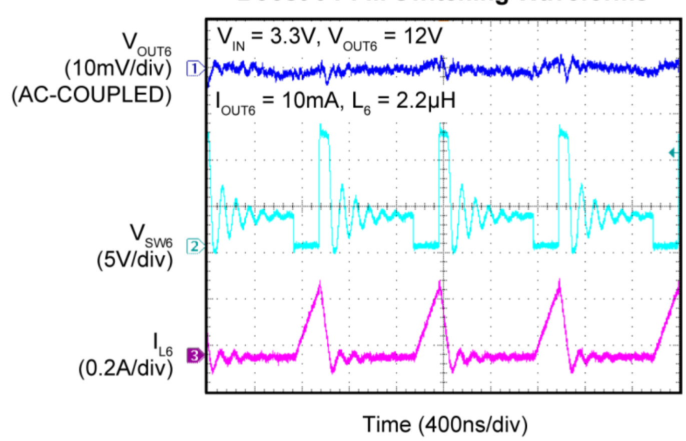
Buck 4 PFM Switching Waveforms



Boost 6 PWM Switching Waveforms

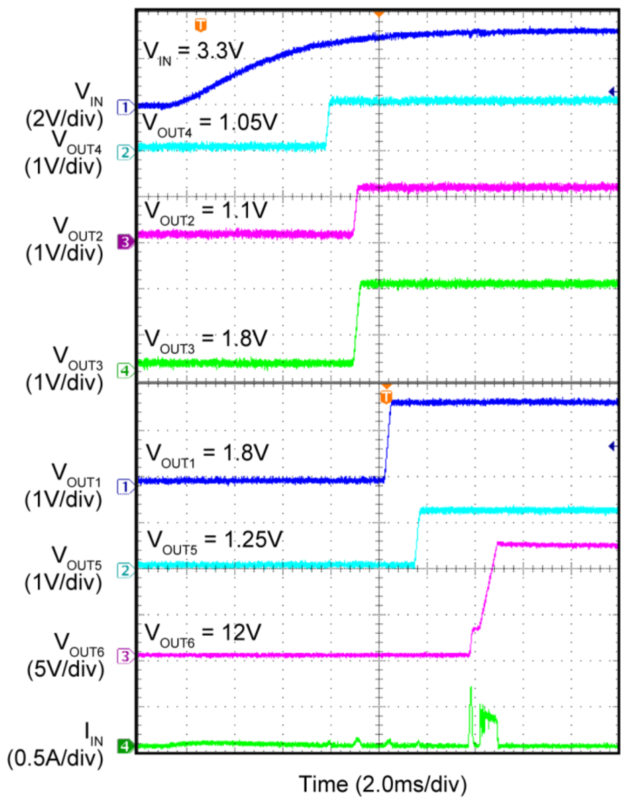


Boost 6 PFM Switching Waveforms

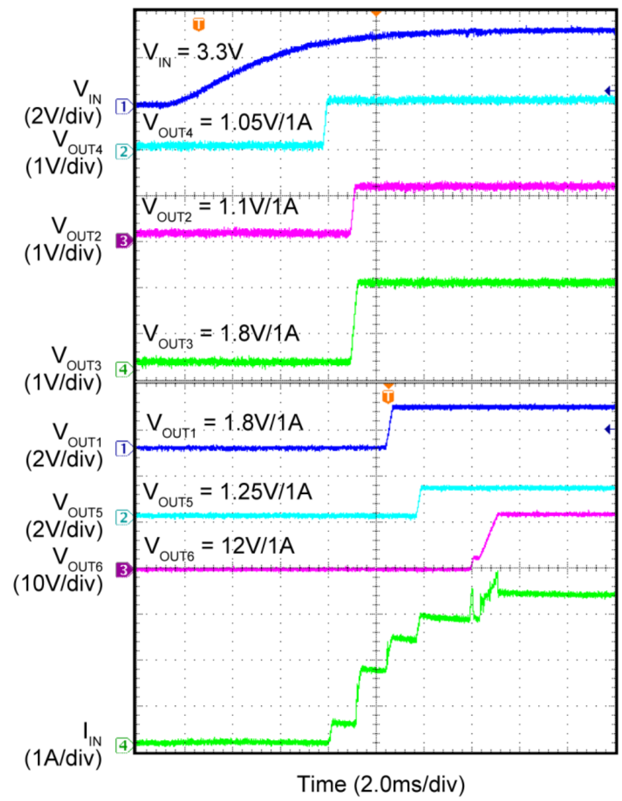


Functional Characteristics (Continued)

Input Supply Inrush Current – No Load

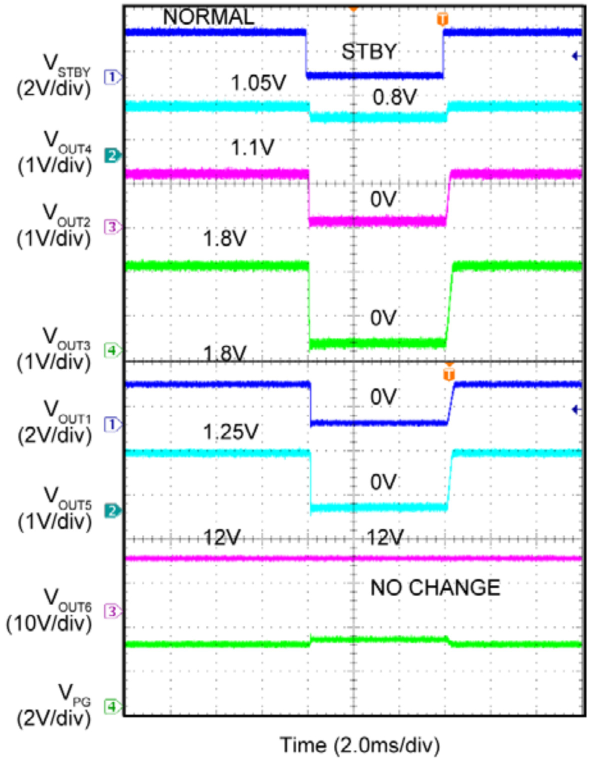


Input Supply Inrush Current – Loaded

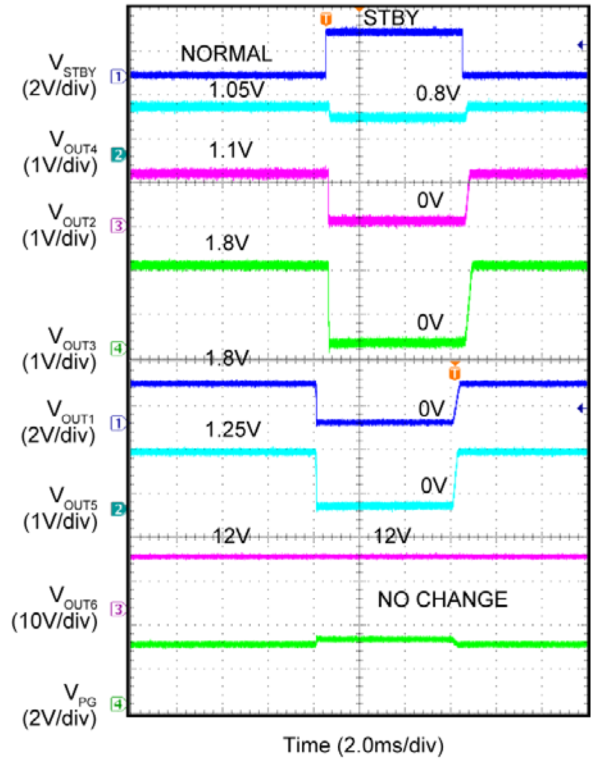


Functional Characteristics (Continued)

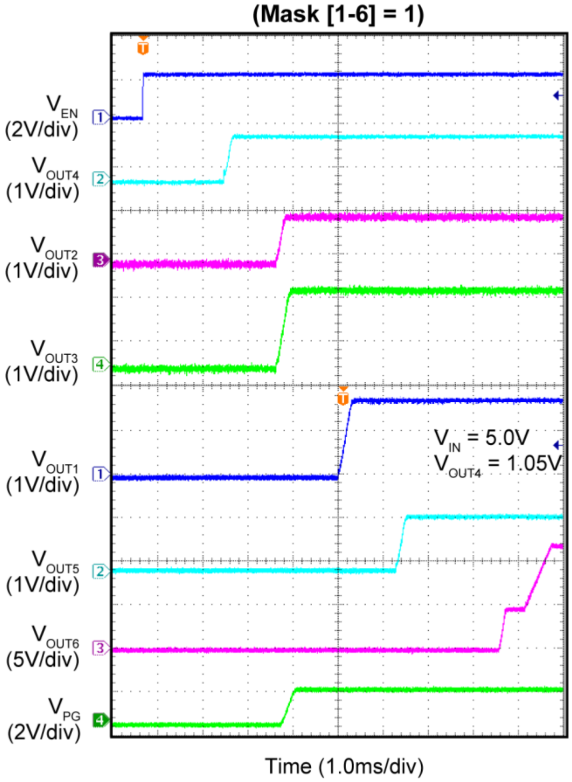
Falling Edge Trigger Standby (DEFAULT)



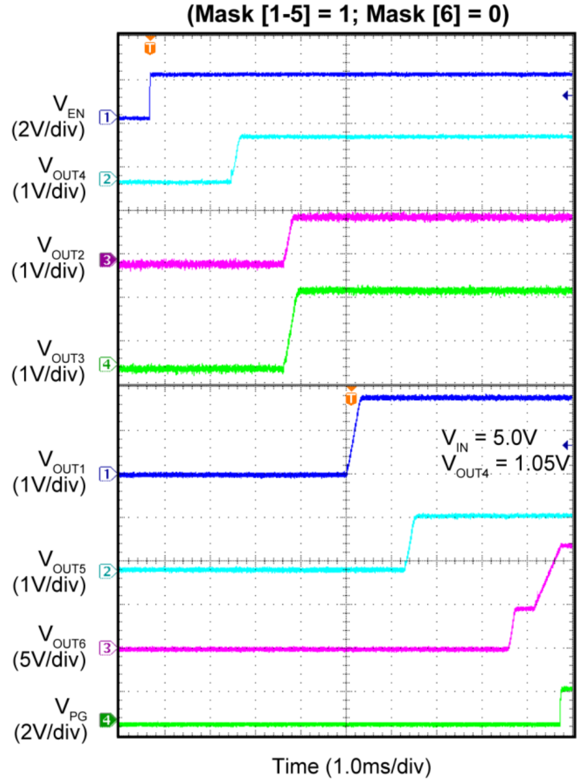
Rising Edge Trigger Standby



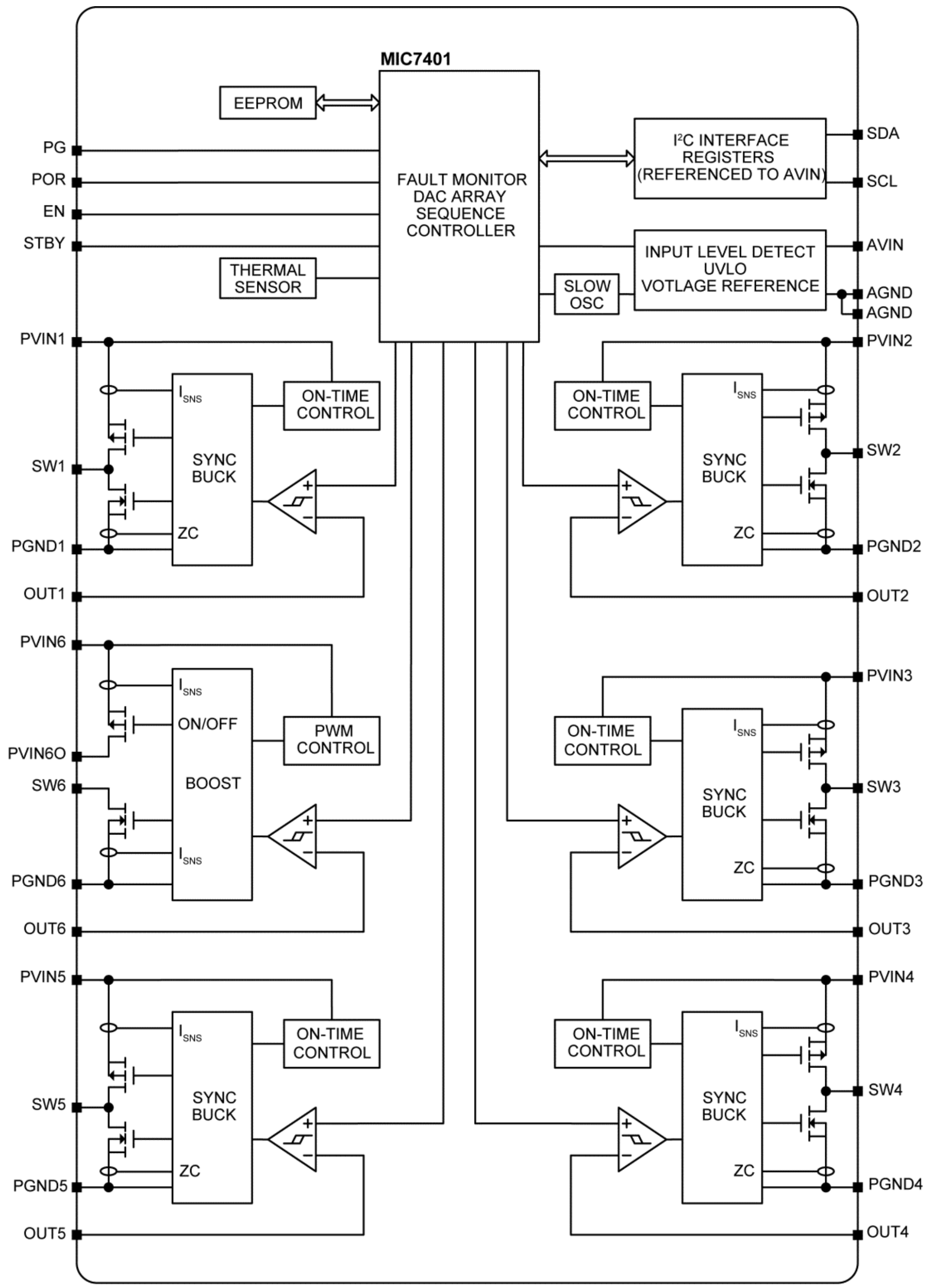
Power Good with All Outputs Masked (Mask [1-6] = 1)



Power Good with All Outputs Masked except V_{OUT6} (Mask [1-5] = 1; Mask [6] = 0)



MIC7401 Block Diagram



Functional Description

The MIC7401 is one of the industry's most-advanced PMIC designed for solid state drives (SSD) on the market today. It is a multi-channel solution which offers software configurable soft-start, sequencing, and digital voltage control (DVC) that minimizes PC board area. These features usually require a pin for programming. However, this approach makes the IC larger by increasing pin count, and also increases BOM cost due to the external components.

The following is a complete list of programmable features:

- Buck output voltage (0.8V – 3.3V/50mV steps)
- Boost output voltage (7.0V – 14V/ 200mV steps)
- Power-on-reset (2.25V – 4.25V/50mV steps)
- Power-on-reset delay (5ms – 160ms/5ms steps)
- Power-up sequencing (6 time slots)
- Power-up sequencing delay (0ms – 7ms/1ms steps)
- Soft-start (4µs – 1024µs per step)
- Buck current limit threshold
  - (1.1A to 6.1A/0.5A steps)
- Boost current limit threshold
  - (1.76A to 2.6A/0.12A steps)
- Boost pull-down (37mA to 148mA/37mA steps)
- Buck pull-down (90Ω)
- Buck standby output voltage programmable
- Boost standby output voltage programmable
- Global power good masking

These features give the system designer the flexibility to customize the MIC7401 for their application. For example, V_{OUT1} current limit can be programmed to 4.1A and V_{OUT2} can be set to 1.1A. These outputs can be programmed to come up at the same time or 2.0ms apart. In addition, in power-saving standby mode, the outputs can either be turned off or programmed to a lower voltage. With this programmability the MIC7401 can be used in multiple platforms.

The MIC7401 buck regulators are adaptive on-time synchronous step-down DC-to-DC regulators. They are designed to operate over a wide input voltage range from 2.4V to 5.5V and provide a regulated output voltage at up to 3.0A of output current. An adaptive on-time control scheme is employed to obtain a constant switching frequency and to simplify the control compensation. The device includes an internal soft-start function which reduces the power supply input surge current at start-up by controlling the output voltage rise time.

The MIC7401 has a current-mode boost regulator that can deliver up to 200mA of output current and only consumes 70µA of quiescent current. The 2.0MHz switching frequency allows small chip inductors to be used. Programmable overcurrent sensing protects the boost from overloads and an output disconnect switch opens to protect against a short-circuit condition. Soft-start is also programmable and controls both the rising and falling output.

Programmable Buck Soft-Start Control

The MIC7401 soft-start feature forces the output voltage to rise gradually, which limits the inrush current during start-up. A slower output rise time will draw a lower input surge current. The soft-start time is based on the least significant bit (LSB) of an internal DAC and the speed of the ramp rate, as shown in Figure 1. This illustrates the soft-start waveform for all five synchronous buck converters. The initial step starts at 150mV and each subsequent step is 50mV.

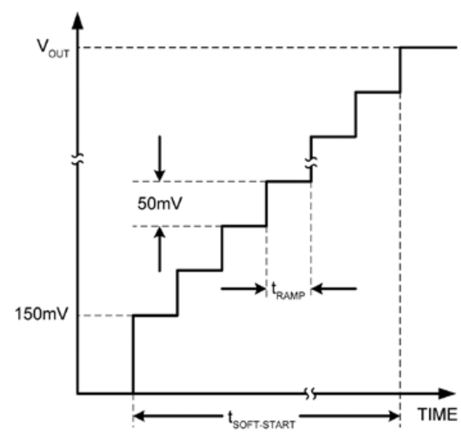


Figure 1. Buck Soft-Start

The output ramp rate (t_{RAMP}) is set by the soft-start registers. Each output ramp rate can be individually set from 4µs to 1024µs, see Table 1 for details.

The soft-start time t_{SS} can be calculated by Equation 1:

$$t_{SS} = \left(\frac{V_{OUT} - 0.15V}{50mV}\right) \times t_{RAMP} \qquad \text{Eq. 1}$$

Where:

t_{SS} = Output rise time

V_{OUT} = Output voltage

t_{RAMP} = Output dwell time

For example:

$$t_{SS} = \left(\frac{1.8V - 0.15V}{50mV}\right) \times 8\mu s$$

$$t_{SS} = 264\mu s$$

Where:

V_{OUT} = 1.8V

t_{RAMP} = 8.0µs

Table 1. Buck Outputs Default Soft-Start Time (DEFAULT)

	V_{OUT} (V)	t_{RAMP} (µs)	t_{SS} (µs)
V_{OUT1}	1.8	8	264
V_{OUT2}	1.1	8	152
V_{OUT3}	1.8	8	264
V_{OUT4}	1.05	8	144
V_{OUT5}	1.25	8	176

Figure 2 shows the output of Buck 1 ramping up cleanly, starting from 0.15V to its final 1.1V value.

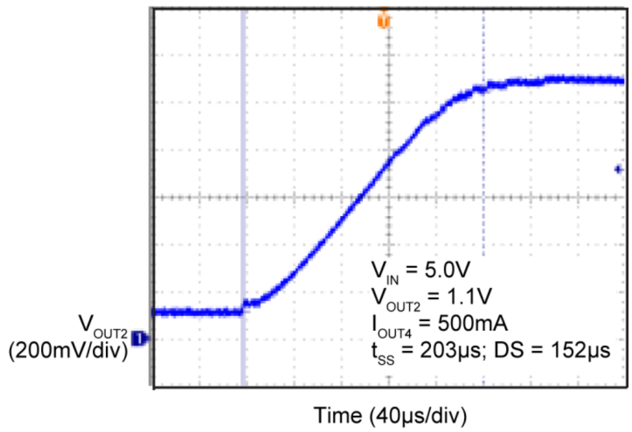


Figure 2. Buck Soft-Start

Buck Digital Voltage Control (DVC)

The output voltage has a 6-bit control DAC that can be programmed from 0.8V to 3.3V in 50mV increments. If the output is programmed to a higher voltage, then the output ramps up, as shown in Figure 3.

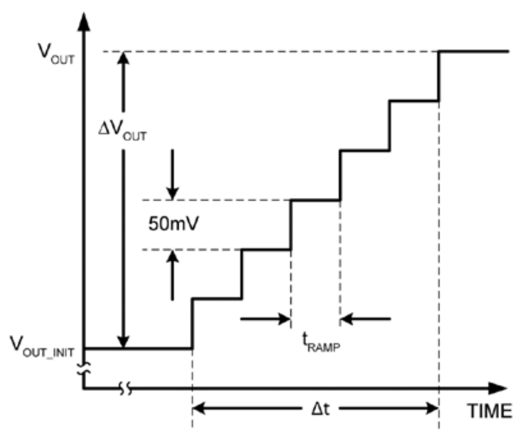


Figure 3. Buck DVC Control Ramp

The ramp time is determined by Equation 2:

$$\Delta t = \left(\frac{V_{OUT} - V_{OUT\_INIT}}{50mV} \right) \times t_{RAMP} \qquad \text{Eq. 2}$$

Where:

V_{OUT_INIT} = Initial output voltage

V_{OUT} = Final output voltage

t_{RAMP} = Output dwell time

When the regulator is set in stand-by mode or programmed to a lower voltage, then the output voltage ramps down at a rate determined by the output ramp rate (t_{RAMP}), the output capacitance and the external load. Small loads result in slow output voltage decay and heavy loads cause the decay to be controlled by the DAC ramp rate.

In Figure 4, V_{OUT1} is switched to stand-by mode with an I²C command and then switched back to normal mode either by an I²C command or a low-to-high transition of the STBY pin. In this case, the rise and fall times are the same due to a 1A load on V_{OUT1}.

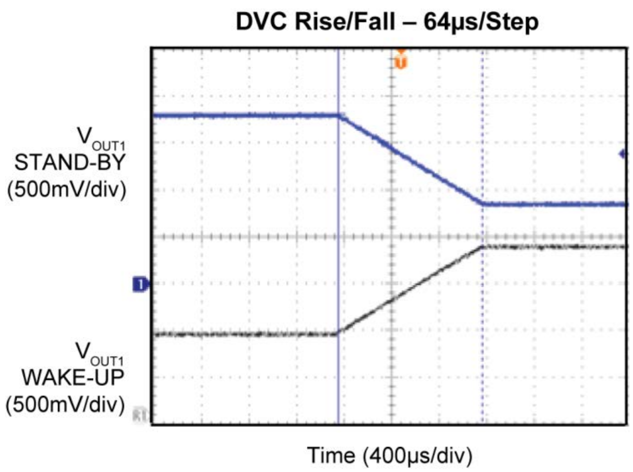


Figure 4. Buck DVC Control Ramp

Programmable Boost Soft-Start Control

The boost soft-start time is divided into two parts as shown in Figure 5. T1 is a fixed 367µs delay starting from when the internal enable goes high. This delay gives enough time for the disconnect switch to turn on and bring the inductor voltage to V_{IN} before the boost is turned on. There is a 50µs delay which is controlled by the parasitic capacitance (Cgd) of the disconnect switch before the output starts to rise.

After the T1 period, the DAC output ramp starts, T2. The total soft-start time, t_{SS}, is the sum of both periods. Figure 6 displays the actual boost soft-start waveform.

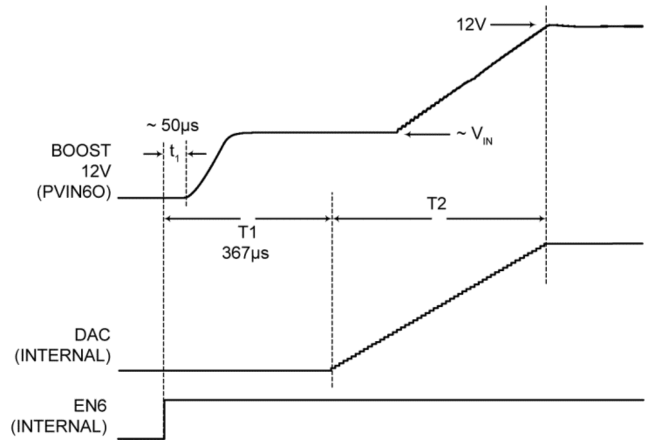


Figure 5. Boost Soft-Start Ramp

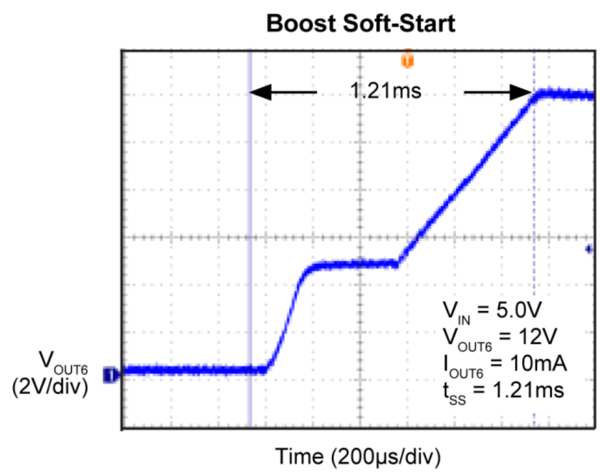


Figure 6. Boost Soft-Start

$$t_{SS} = T1 + T2$$

$$T2 = \left(\frac{(V_{OUT} - 1.4V)}{0.2V}\right) \times t_{RAMP} \qquad \text{Eq. 2}$$

$$T2 = \left(\frac{(12V - 1.4V)}{0.2V}\right) \times 16\mu s$$

Where:

T1 = 367µs

T2 = 848µs

t_{SS} = 367µs + 848µs = 1.215ms

V_{OUT} = Output voltage

t_{RAMP} = Output dwell time = 16µs

Boost Digital Voltage Control (DVC)

The boost output control works the same way as the buck, except that the voltage steps are 200mV, see Figure 7. When the boost is programmed to a lower voltage the output ramps down at a rate determined by the output ramp rate (t_{RAMP}), the output capacitance and the external load. During both the ramp up and down time, the power good output is blanked and will not imitate a fault flag if the power good mask bit is set to "1".

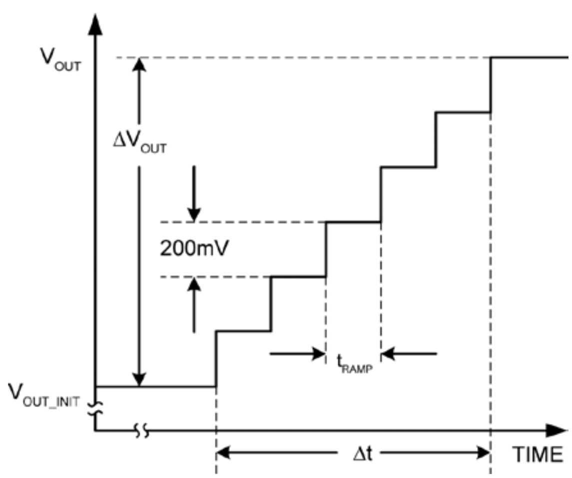


Figure 7. Boost DVC Control Ramp

The ramp time can be computed using Equation 3:

$$\Delta t = \left(\frac{V_{OUT} - V_{OUT\_INIT}}{0.2V}\right) \times t_{RAMP} \qquad \text{Eq. 3}$$

Where:

V_{OUT_INIT} = Initial output voltage

Table 2. Boost Output Default Soft-Start Time

	V_{OUT} (V)	t_{RAMP} (µs)	t_{SS} (ms)
V_{OUT6}	12	16	1.215

Buck Current Limit

The MIC7401 buck regulators have high-side current limiting that can be varied by a 4-bit code. If the regulator remains in current limit for more than seven consecutive PWM cycles, the output is latched off, the over-current status register bit is set to 1, the power-good status register bit is set to 0 and the global power good (PG) output pin is pulled low. An over-current fault on one output will not disable the remaining outputs. Table 3 shows the current limit register settings verses output current. The current limit register setting is set at twice the maximum output current.

Table 3. Buck Current Limit Register Settings

$I_{OUT(MAX)}$	I_{PROG}	BINARY	HEX
0.5A	1.1A	1111	F'h
1.0A	2.1A	1101	D'h
1.5A	3.1A	1011	B'h
2.0A	4.1A	1001	9'h
2.5A	5.1A	0111	7'h
3.0A	6.1A	0101	5'h

The output can be turned back on by recycling the input power or by software control. To clear the overcurrent fault by software control, set the enable register bit to "0" then clear the overcurrent fault by setting the fault register bit to "0". This will clear the over-current and power good status registers. Now the output can be re-enabled by setting the enable register bit to "1".

During start-up sequencing if Output 1 is still shorted, Outputs 2 through 4 will come up normally. Once an overcurrent condition is sensed, then the fault register is set to "1" and the start-up sequence will stop and no further outputs will be enabled. See Figure 9 for default start-up sequence.

Boost Current Limit

The boost current limit features cycle-by-cycle protection. The duty cycle is cut immediately once the current limit is hit. When the boost current limit is hit for five consecutive cycles, the FAULT signal is asserted and remains asserted with the boost converter keeping on running until the boost is powered off.

This protects the boost in normal overload conditions, but not in a short-to-ground case. For a short circuit to ground, the boost current limit will not be able to limit the inductor current. This short-circuit condition is sensed by the current in the disconnect switch. When the disconnect switch current limit is hit for four consecutive master clock cycles (2MHz), regardless if the boost is switching or not, both the disconnect switch and boost are latched off automatically and the FAULT signal is asserted.

The output can be turned back on by recycling the input power or by software control. To clear the overcurrent fault by software control, set the enable register bit to "0" then clear the overcurrent fault by setting the fault register bit to "0".

Global Power Good Pin

The global power-good output indicates that all the outputs are above the 91% limit after the power-up sequence is completed. Once the power-up sequence is complete, the global power good output stays high unless an output falls below its power-good limit, a thermal fault occurs, the input voltage drops below the lower UVLO threshold or an output is turned OFF by setting the enable register bit to "0" unless the PGOOD_MASK[x] bit is set to "1" (Default).

A power-good mask bit can be used to control the global power good output. The power-good mask feature is programmed through the PGOOD_MASK[x] registers and is used to ignore an individual power-good fault. When masked, PGOOD_MASK[x] bit is set to "1", an individual power good fault will not cause the global power good output to de-assert.

If all the PGOOD_MASK[x] bit are set to "1", then the power good output de-asserts as soon as the first output starts to rise. The PGOOD_MASK[x] bit of the last output must be set to "0" to have the PG output stay low until the last output reaches 91% of its final value.

The global power-good output is an open-drain output. A pull-up resistor can be connected to V_{IN} or V_{OUT}. Do not connect the pull-up resistor to a voltage higher than AV_{IN}.

Standard Delay

There is a programmable timer that is used to set the standard delay time between each time slot. The timer starts as soon as the previous time slot's output power good goes high. When the delay completes, the regulators assigned to that time slot are enabled, see Figure 8.

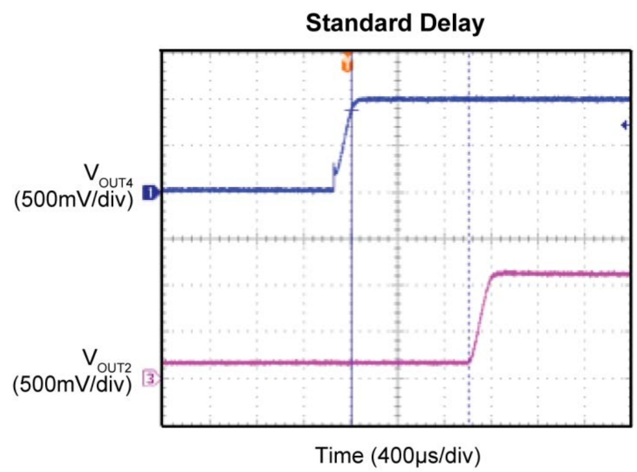


Figure 8. Standard Delay Time

Power-Up Sequencing

When power is first applied to the MIC7401, all I²C registers are loaded with their default values from the EEPROM. There is about a 1.5ms delay before the first regulator is enabled while the MIC7401 goes through the initialization process. The DELAY register's STDEL bits set the delay between powering up each regulator at initial power up.

The sequencing registers allow the outputs to come up in any order. There are six time slots that an output can be configured to power up in. Each time slot can be programmed for up to six regulators to be turned on at once or none at all.

Figure 9 shows an example of this feature. V_{OUT4} is enabled in time slot 1. After a 1ms delay, V_{OUT2} and V_{OUT3} are enable at the same time in time slot 2. The 1ms is the standard delay for all of the outputs and can be programmed from 0ms to 7ms in 1ms. Next, V_{OUT1} is powered up in time slot 3 and V_{OUT5} in time slot 4. There are no regulators programmed for time slot 5. Finally, V_{OUT6} is powered up in time slot 6. The global power good output, V_{PG}, goes high as soon as the last output reaches 91% of its final value. Here the PGOOD_MASK[6] bit is set to "0".

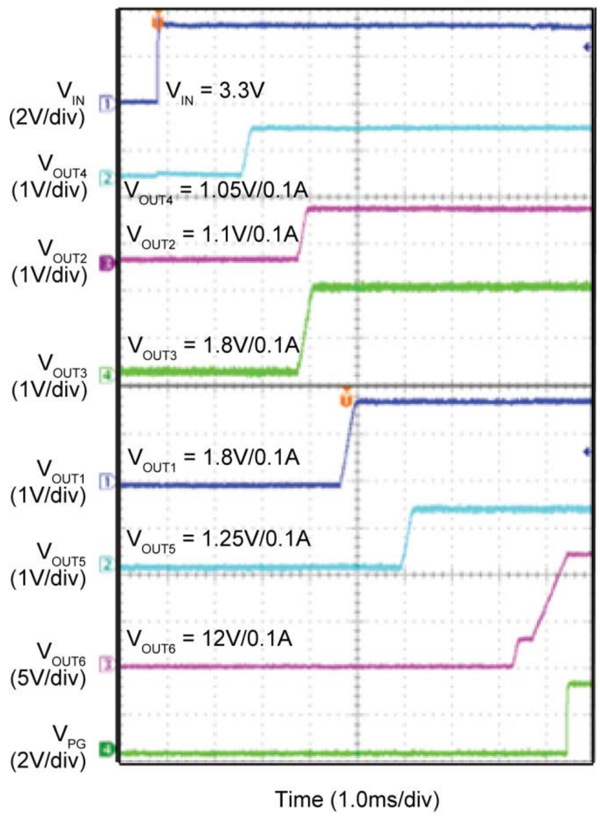


Figure 9. Hot Plug – V_{IN} Rising

Global Enable Pin

When the enable pin rises above the enable threshold voltage, the MIC7401 enters its start-up sequence.

Programmable Power-on-Reset (POR) Delay

The POR output pin provides the user with a way to let the SOC know that the input power is failing. If the input voltage falls below the power-on reset lower threshold level, the POR output immediately goes low. The lower threshold is set in the PORDN register and the upper threshold uses PORUP register.

The low-to-high POR transition can be delayed from 5ms to 160ms in 5ms increments. This feature can be used to signal the SOC that the power supplies are stable. The PORDEL register sets the delay of the POR pin. The POR delay starts as soon as the AVIN pin voltage rises above the power-on reset upper threshold limit. Figure 10 shows the POR operation.

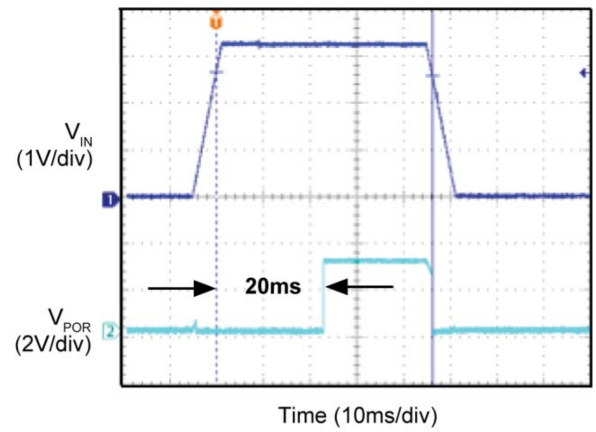


Figure 10. POR

Power-Down Sequencing

When power is removed from V_{IN}, all the regulators try to maintain the output voltage until the input voltage falls below the UVLO limit of 2.35V as shown in Figure 11.

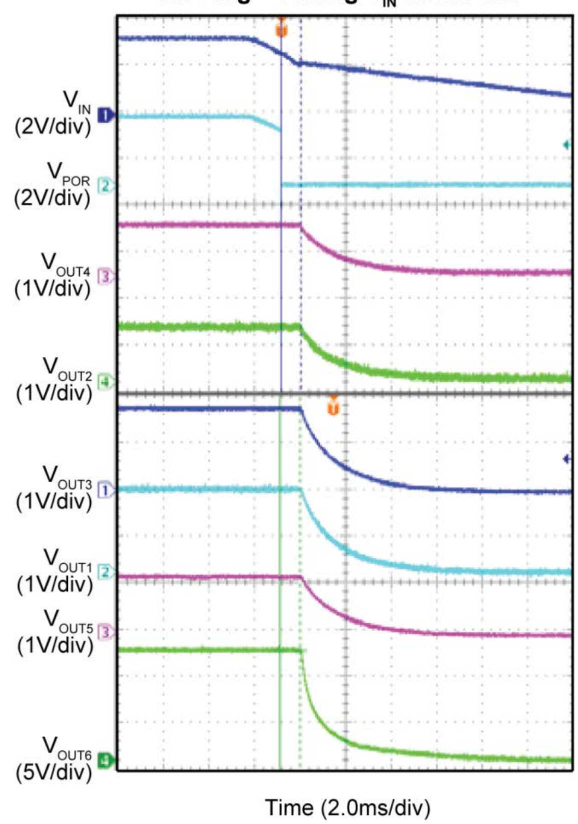


Figure 11. Hot Un-Plug – V_{IN} Falling

Stand-By Mode

In stand-by mode, efficiency can be improved by lowering the output voltage to the standby mode value or turning an output off completely. There are two registers used for setting the output voltage, normal-mode register and stand-by mode register. The default power-up voltages are set in the normal-mode registers.

An I²C write command to the STBY_CTRL_REG register or the STBY pin can be used to set the MIC7401 into stand-by mode. Figure 12 shows an I²C write command implementation. In stand-by mode, the output can be programmed to a lower voltage or turned completely off. When disabled, the output will be soft-discharged to zero if the PULLD[1-6] register are set to 1. If PULLD[x] = 0 the output drifts to PGND at a rate determined by the load current and output capacitance.

In stand-by, if an output is disabled, the global power good output is not affected when the PGOOD_MASK[x] is set to logic 1. If the PGOOD_MASK[x] is set to logic 0, then the global power good flag is pulled low. In Figure 12, all the PGOOD_MASK[x] bits are set to logic 1.

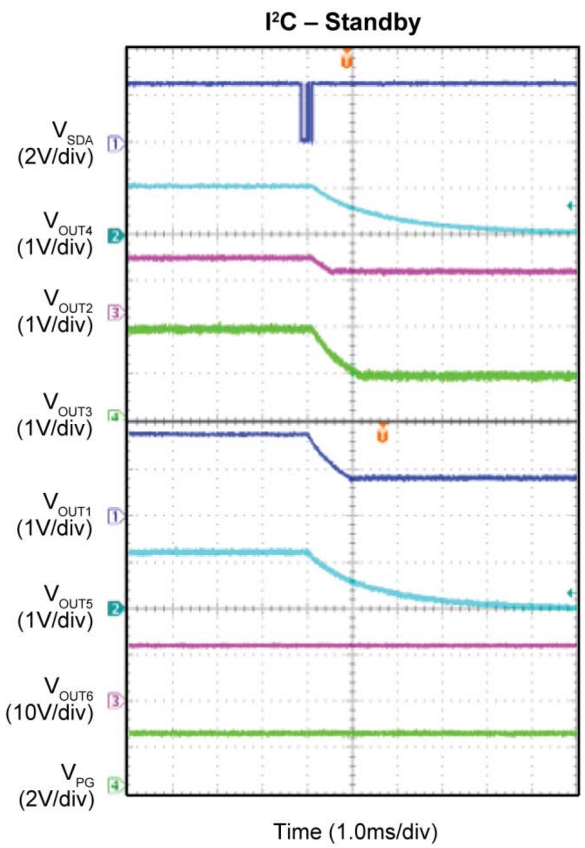


Figure 12. I²C Stand-By Mode

Resistive Discharge

To ensure a known output condition in stand-by mode, the output is actively discharged to ground if the output is disabled. Setting the buck pull down register field PULLD[1-5] = 1 connects a 90Ω pull down resistor from OUT[x] to PGND[x] when the MIC7401 is disabled. If PULLD[x] = 0 the output drifts to PGND at a rate determined by the load current and the output capacitance value. The boost has a programmable pull-down current level from 37mA to 148mA. In Figure 13, the top trace shows the normal pull down and the bottom trace is with the 90Ω pull-down.

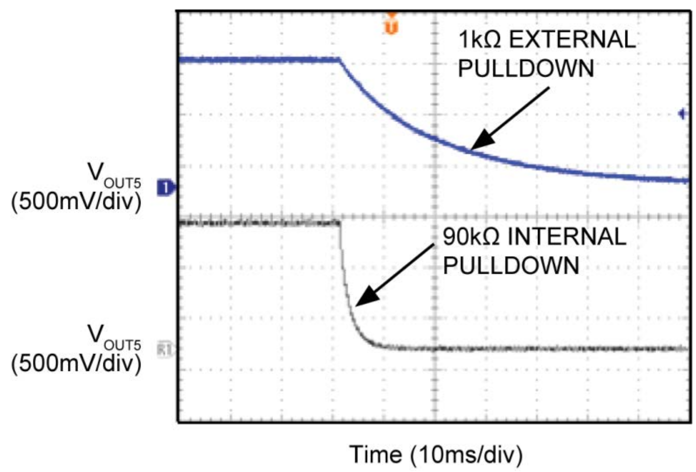


Figure 13. Output Pull-Down Resistance

STBY Pin

A pin-selectable STBY input allows the MIC7401 to be placed into standby or normal mode. In standby mode, the individual regulator can be turned on or off or the output voltage can be set to a different value. If the regulators are turned off, standby mode cuts the quiescent current by 23µA for each buck regulator and 70µA for the boost.

Figure 14 illustrates the STBY pin operation. A low-to-high transition on the STBY pin switches the output from standby mode to normal mode. There is a 100µs STBY deglitch time to eliminate nuisance tripping then all the regulators are enabled at the same time and ramp up with their programmed ramp rates. A high-to-low transition on the STBY pin switches the output from normal mode to standby mode.

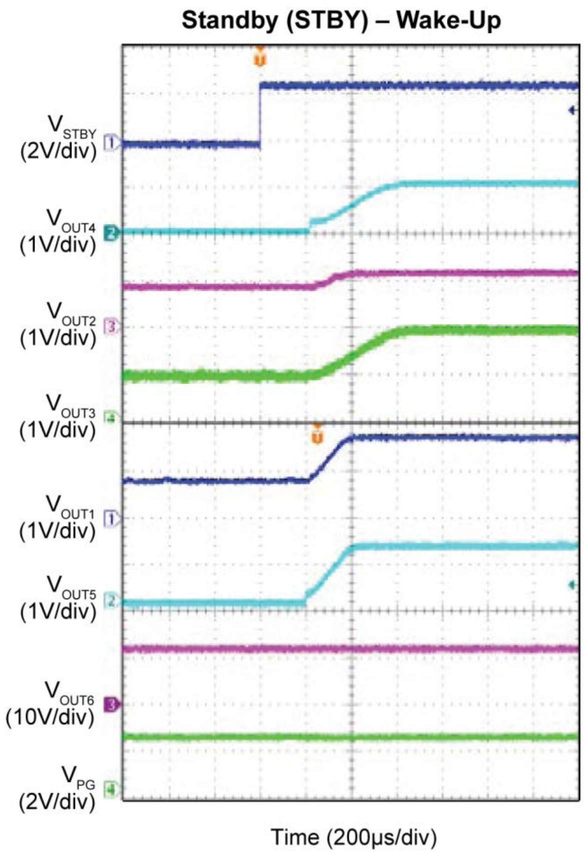


Figure 14. STBY-to-NORMAL Transition (DEFAULT)

Safe Start-Up into a Pre-Biased Output

The MIC7401 is designed for safe start-up into a pre-biased output. This prevents large negative inductor currents which can cause the output voltage to dip and excessive output voltage oscillations. A zero crossing comparator is used to detect a negative inductor current. If a negative inductor current is detected, the low-side synchronous MOSFET functions as a diode and is immediately turned off.

Figure 15 shows a 1V output pre-bias at 0.5V at start-up, see V_{OUT4} trace. The inductor current, Trace I_{L4}, is not allowed to go negative by more than 0.5A before the low-side switch is turned off. This feature prevents high negative inductor current flow in a pre-bias condition which can damage the IC.

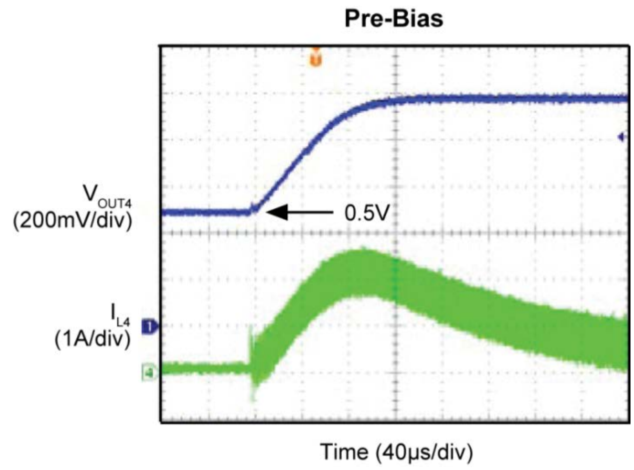


Figure 15. Pre-Biased Output Voltage

Buck Regulator Power Dissipation

The total power dissipation in a MIC7401 is a combination of the five buck regulators and the boost dissipation. The buck regulators (OUT1 to OUT5) dissipation is approximately the switcher's input power minus the switcher's output power and minus the power loss in the inductor:

$$P_{D\_BUCK} \approx V_{IN} \times I_{IN} - V_{OUT} \times I_{OUT} - P_{L\_LOSS} \qquad \text{Eq. 4}$$

While the boost power dissipation is estimated by Equation 5:

$$P_{D\_BOOST} \approx V_{IN} \times I_{IN} - V_{OUT} \text{ x } I_{OUT} - P_{L\_LOSS} - V_f \times I_{OUT} \qquad \text{Eq. 5}$$

Although the maximum output current for a single buck regulator can be as much as 3A, the MIC7401 will thermal limit and will not support this high output current on all outputs at the same time.

Total Power Dissipation

The total power dissipation in the MIC7401 package is equal to the sum of the power loss of each regulator:

$$P_{D\_TOTAL} \approx \text{SUM } (P_{D\_SWITCHERS}) \qquad \text{Eq. 6}$$

Once the total power dissipation is calculated, the IC junction temperature can be estimated using Equation 7:

$$T_{J(MAX)} \approx T_A + P_{D\_TOTAL} \times \theta_{JA} \qquad \text{Eq. 7}$$

Where:

$T_{J(MAX)}$ = The maximum junction temperature

T_A = The ambient temperature

θ_{JA} = The junction-to-ambient thermal resistance of the package (30°C/W)

Figure 16 shows the measured junction temperature versus power dissipation of the MIC7401 evaluation board. The actual junction temperature of the IC depends upon many factors. The significant factors influencing the die temperature rise are copper thickness in the PCB, the surface area available for convection heat transfer, air flow and power dissipation from other components, including inductors, SOCs and processor ICs. It is good engineering practice to measure all power components temperature during the final design review using a thermal couple or IR thermometer, see the "Thermal Measurements" sub-section for details.

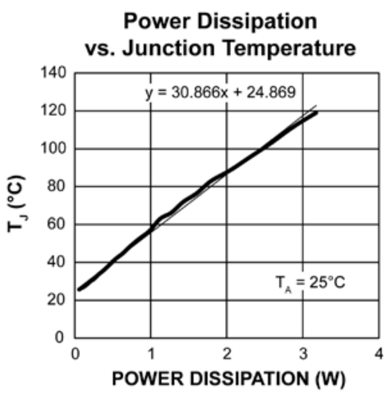


Figure 16. Power Dissipation

Power Derating

The MIC7401 package has a 2W power dissipation limit. To keep the IC junction temperature below a 125°C design limit, the output power has to be limited above an ambient temperature of 65°C. Figure 17 shows the power dissipation derating curve.

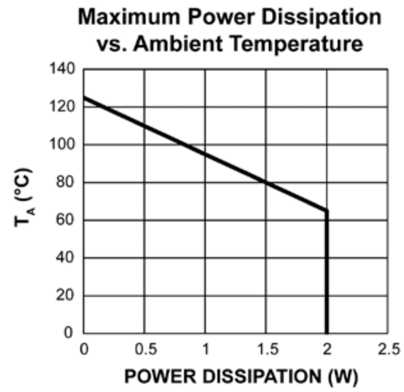


Figure 17. Power Derating Curve

The maximum power dissipation of the package can be calculated by Equation 8:

$$P_{D(MAX)} \approx \left(\frac{T_{J(MAX)} - T_A}{\theta_{JA}}\right) \qquad \text{Eq. 8}$$

Where:

$T_{J(MAX)}$ = Maximum junction temperature (125°C)

T_A = Ambient temperature

θ_{JA} = Junction-to-ambient thermal resistance of the package (30°C/W).

Overtemperature Fault

An overtemperature fault is triggered when the IC junction temperature reaches 160°C. When this occurs, both the over temperature fault flag is set to 1, the global power good output is pulled low and all the outputs are turned off. During the fault condition the I^2C interface remains active and all registers values are maintained.

When the die temperature decreases by 20°C the overtemperature fault bit can be cleared. To clear the fault, either recycle power or write a logic "0" to the over temperature fault register. Once the fault bit is cleared, the outputs power up to their default values and are sequenced according to the time slot settings.

Input Voltage "Hot-Plug"

High-voltage spikes twice the input voltage can appear on the MIC7401 PVIN pins if a battery pack is hot-plugged to the input supply voltage connection as shown in Figure 18 (Trace 1). These spikes are due to the inductance of the wires to the battery and the very low inductance and ESR of the ceramic input capacitors. This problem can be solved by placing a 150µF POS capacitor across the input terminals. Figure 18 (Trace 2) shows that the high-voltage spike is greatly reduced to a value below the maximum allowable input voltage rating.

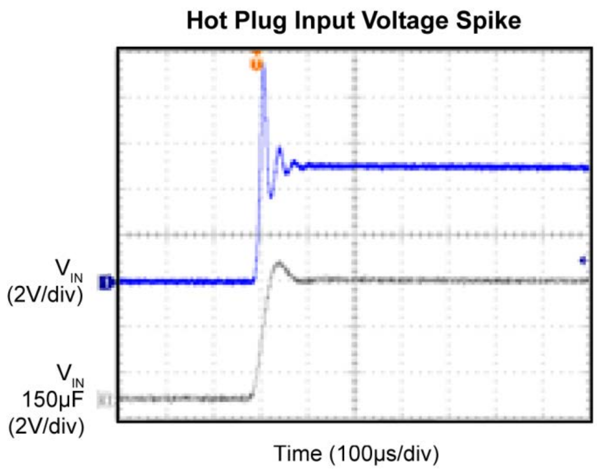


Figure 18. Hot-Plug Input Voltage Spike

Thermal Measurements

Measuring the IC's case temperature is recommended to ensure it is within its operating limits. Although this might seem like a very elementary task, it is easy to get erroneous results. The most common mistake is to use the standard thermal couple that comes with a thermal meter. This thermal couple wire gauge is large (typically 22 gauge) and behaves like a heatsink, resulting in a lower case measurement.

Two reliable methods of temperature measurement are a smaller thermal couple wire or an infrared thermometer. If a thermal couple wire is used, it must be constructed of 36 gauge wire or higher (smaller wire size) to minimize the wire heat-sinking effect. In addition, the thermal couple tip must be covered in either thermal grease or thermal glue to make sure that the thermal couple junction is making good contact with the case of the IC. Omega brand thermal couple (5SC-TT-K-36-36) is adequate for most applications.

Whenever possible, an infrared thermometer is recommended. The measurement spot size of most infrared thermometers is too large for an accurate reading on a small form factor ICs. However, an IR thermometer from Optris has a 1mm spot size, which makes it a good choice for measuring the hottest point on the case. An optional stand makes it easy to hold the beam on the IC for long periods of time.

Timing Diagrams

Normal Power-Up Sequence for Outputs

The STDEL register sets the delay between powering up of each regulator at initial power-up (see power up sequencing in Figure 19). Once all the internal power good registers PGOOD[1-6] are all 1, then the global PG pin goes high without delay.

The PORDEL register sets the delay for the POR flag pin. The POR delay time starts as soon as AVIN pin voltage rises above the system UVLO upper threshold set by the PORUP register. The POR output goes low without delay if AVIN falls below the lower UVLO threshold set by the PORDN register.

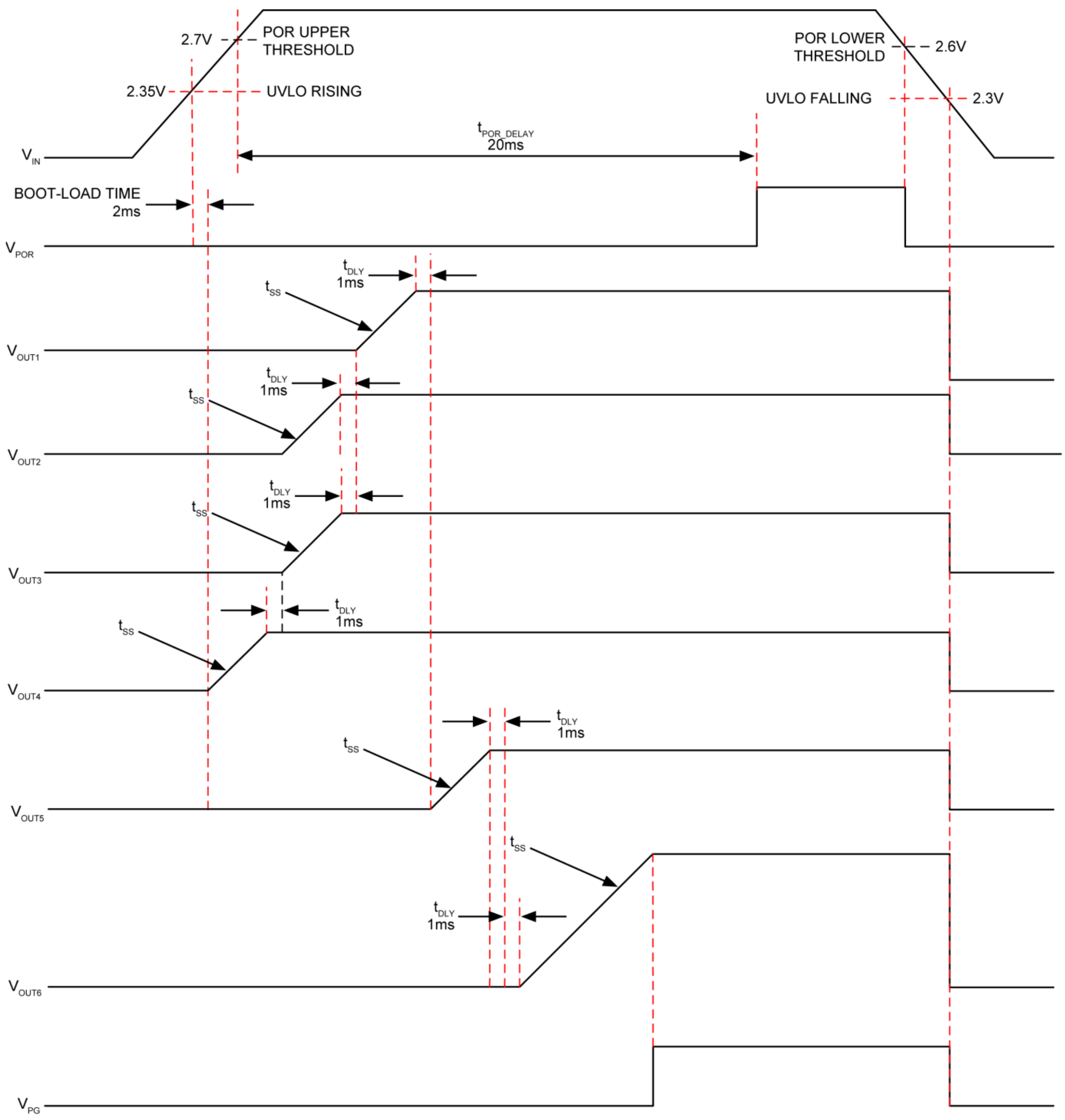


Figure 19. MIC7401 Power-Up/-Down

Standby (STBY) Pin (Wake-Up)

An I²C write command to the STBY_CTRL_REG register or the STBY pin can be used to set the MIC7401 into stand-by mode. The standby (STBY) pin provides a hardware-specific manner in which to wake-up from stand-by mode and go into normal mode. Figure 20 shows the STBY pin operation. A low-to-high transition on the STBY pin switches the output from stand-by mode to normal mode.

There is a 100µs STBY deglitch time to eliminate nuisance tripping then all the regulators are enabled at the same time and ramp up with their programmed ramp rates.

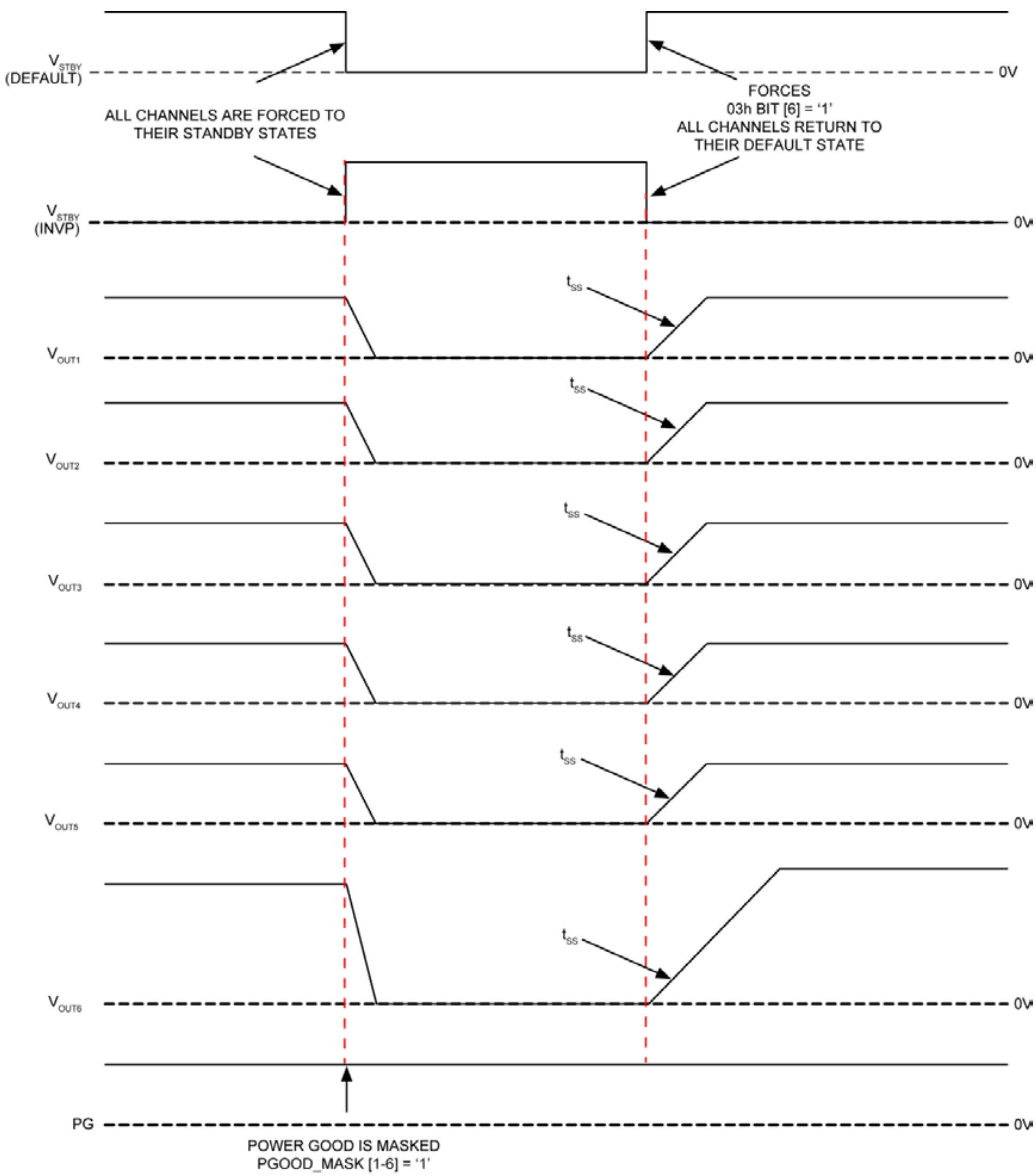
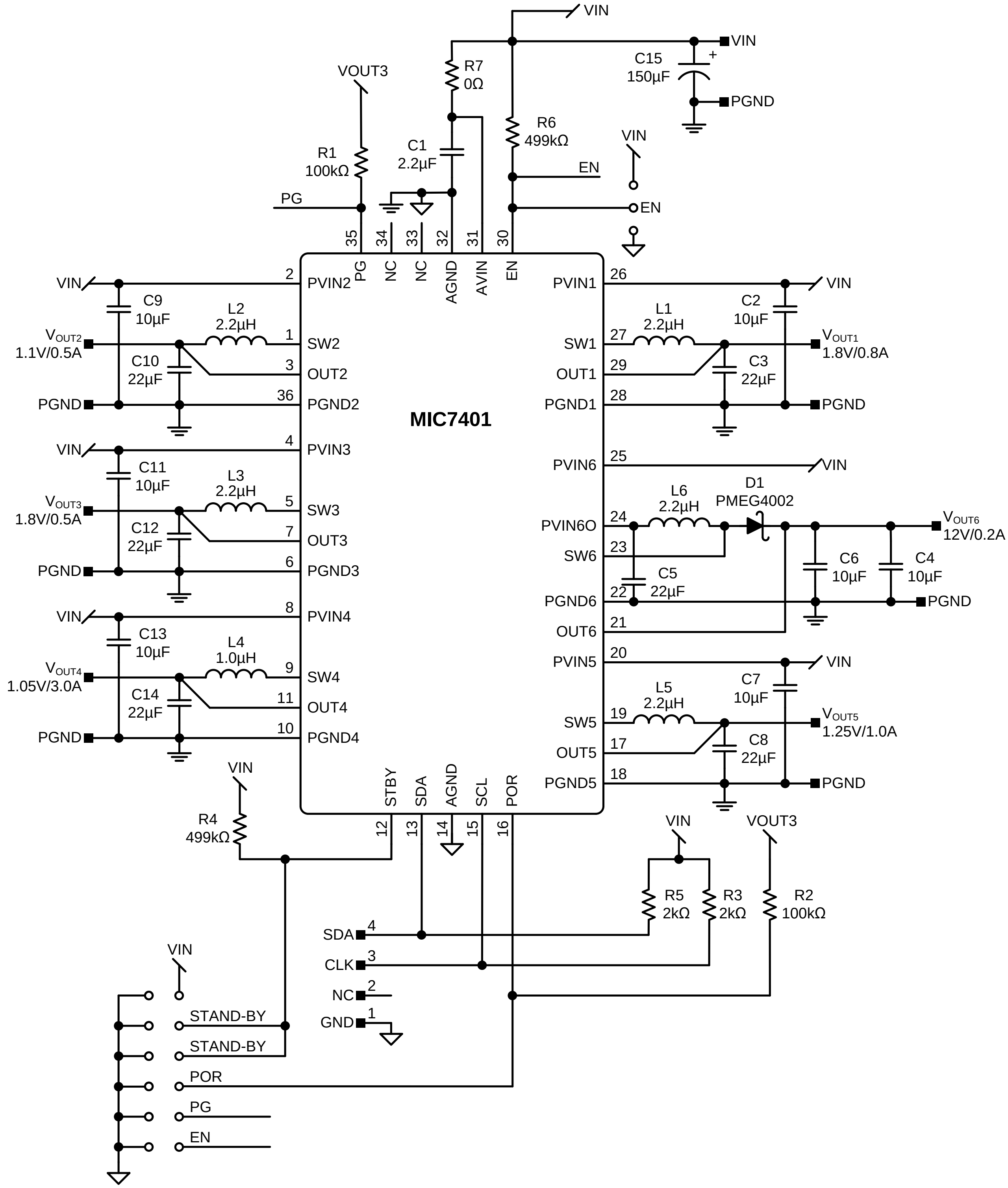


Figure 20. MIC7401 STBY Function (DEFAULT)

Evaluation Board Schematic



Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C1	CL05A225KO5NQNC	Samsung[14]	2.2µF/16V, Ceramic, X5R, 0402, 0.8mm, ±10%	1
C2, C7, C9, C11, C13	CL10A106MO8NQNC	Samsung	10µF/16V, Ceramic, X5R, 0603, 0.8mm, ±20%	5
C4, C6	CL21A106KAYNNNE	Samsung	10µF/25V, Ceramic, X5R, 0805, 1.25mm, ±20%	2
C3, C5, C8, C10, C12, C14	CL10A226MQ8NUNE	Samsung	22µF/6.3V, Ceramic, X5R, 0603, 0.8mm, ±20%	6
C15	EEF-CX0J151XR	Panasonic	150µF/6.3V, POS Capacitor, SP, ±20%	1
D1	PMEG4002EL	NXP[15]	0.2A/40V, Schottky, SOD-882	1
R1, R2	RC1005F104CS	Samsung	100kΩ, Resistor, 0402, 1%	3
R3, R5	RC1005F202CS	Samsung	2.0kΩ, Resistor, 0402, 1%	2
R4, R6	RC1005F4993CS	Samsung	499kΩ, Resistor, 0402, 1%	1
R7	RC1005J000CS	Samsung	0.00Ω, Resistor, 0402, Jumper	1
L1, L2, L3, L5, L6	CIG22H2R2MNE	Samsung	2.2µH, 1.6A Inductor, 116mΩ, 2520 × 1.2mm (maximum)	5
L4	CIGW252010GM1R0MNE	Samsung	1.0µH, 3.3A Inductor' 40mΩ, 2520 × 1.0mm (maximum)	1
U1	**MIC7401YFL**	**Micrel**[16]	**Five-Channel Buck Regulator Plus One Boost with HyperLight Load and I^{2}C Control**	**1**

Notes:

14. Samsung: www.samsung.com.
15. NXP: www.nxp.com.
16. **Micrel, Inc.:** www.micrel.com.

PCB Layout Guidelines

Warning!!! To minimize EMI and output noise, follow these layout recommendations.

PCB Layout is critical to achieve reliable, stable and efficient performance. A ground plane is required to control EMI and minimize the inductance in power, signal and return paths.

The following guidelines should be followed to insure proper operation:

General

- Most of the heat removed from the IC is due to the exposed pad (EP) on the bottom of the IC conducting heat into the internal ground planes and the ground plane on the bottom side of the board. Use at least 16 vias for the EP to ground plane connection.
- Do not connect the PGND and AGND traces together on the top layer. The single point connection is made on the layer 2 ground plane.
- Do not put a via directly in front of a high current pin, SW, PGND, or PVIN. This will increase the trace resistance and parasitic inductance.
- Do not place a via in between the input and output capacitor ground connection. Put it to the inside of the output capacitor and in the way of the high di/dt current path.
- Route all power traces on the top layer, as shown in the example layout.
- Place the input capacitors first and put them as close as possible to the IC.

IC

- The 2.2µF ceramic capacitor, which is connected to the AVIN pin, must be located right at the IC. The AVIN pin is very noise sensitive and placement of the capacitor is very critical. Use wide traces to connect to the AVIN and AGND pins.
- The analog ground pin (AGND) must be connected directly to the ground planes. Do not route the SGND pin to the PGND Pad on the top layer.
- Use fat traces to route the input and output power lines.
- Use Layer 5 as an input voltage power plane.
- Layer 2 and the bottom layer (Layer 6) are ground planes.

Input Capacitor

- A 10µF X5R or X7R dielectrics ceramic capacitor is recommended on each of the PVIN pins for bypassing.
- Place the input capacitors on the same side of the board and as close to the IC as possible.
- Keep both the PVIN pin and PGND connections short.
- If possible, place vias to the ground plane close to the each input capacitor ground terminal, but not in the way of the high di/dit current path.
- Use either X7R or X5R dielectric input capacitors. Do not use Y5V or Z5U type capacitors.
- Do not replace the ceramic input capacitor with any other type of capacitor. Any type of capacitor can be placed in parallel with the input capacitor.
- In “Hot-Plug” applications, a Tantalum or Electrolytic bypass capacitor must be used to limit the over-voltage spike seen on the input supply when power is suddenly applied.

Inductor

- Keep the inductor connection to the switch node (SW) short.
- Do not route any digital lines underneath or close to the inductor.
- To minimize noise, place a ground plane underneath the inductor.

Output Capacitor

- Use a wide trace to connect the output capacitor ground terminal to the input capacitor ground terminal. In the example layout, all input and output capacitor ground connections are place back-to-back.
- The OUT[1-6] trace should be separate from the power trace and connected as close as possible to the output capacitor. Sensing a long high-current load trace can degrade the DC load regulation.

Proper Termination of Unused Pins

Many designs will not require all six DC-to-DC output voltages. In these cases, the unused pin must be connected to either V_{IN} or GND.

The schematic in Figure 21 shows where to tie the unused pins and Table 4 summarizes the connections.

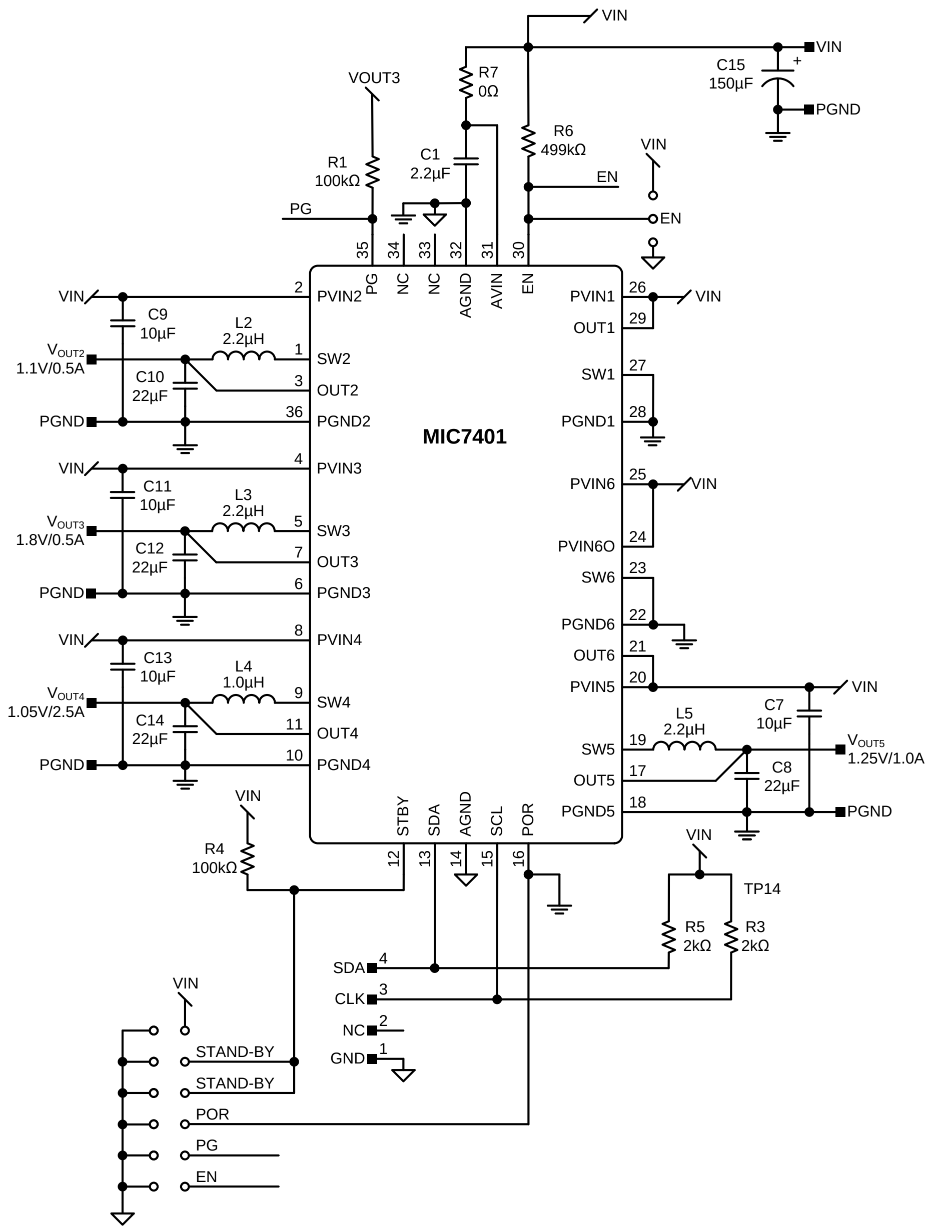
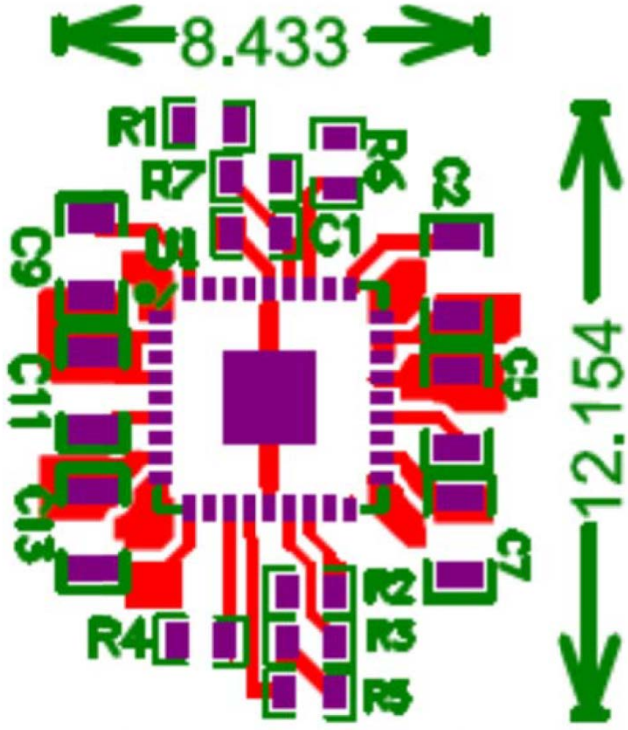


Figure 21. Connections for Unused Pins

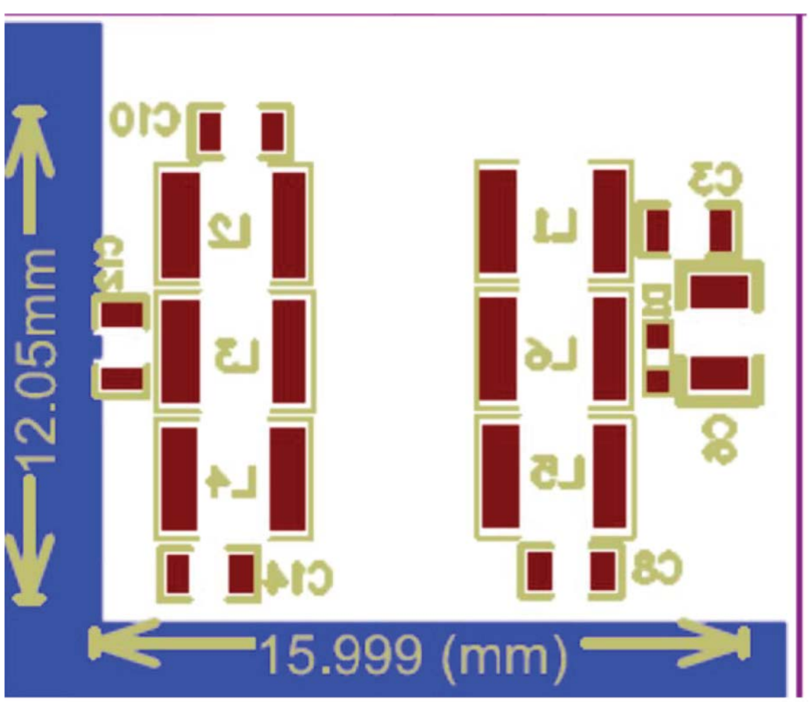
Table 4. Summarization of Unused Pin Connections

Unused	VIN	PGND
Boost	PVIN6, PGIN6O, VOUT6	PGND6, SW6
Buck	PVIN[x], VOUT[x]	PGND[6], SW[x]
POR		POR

PCB Layout Recommendations

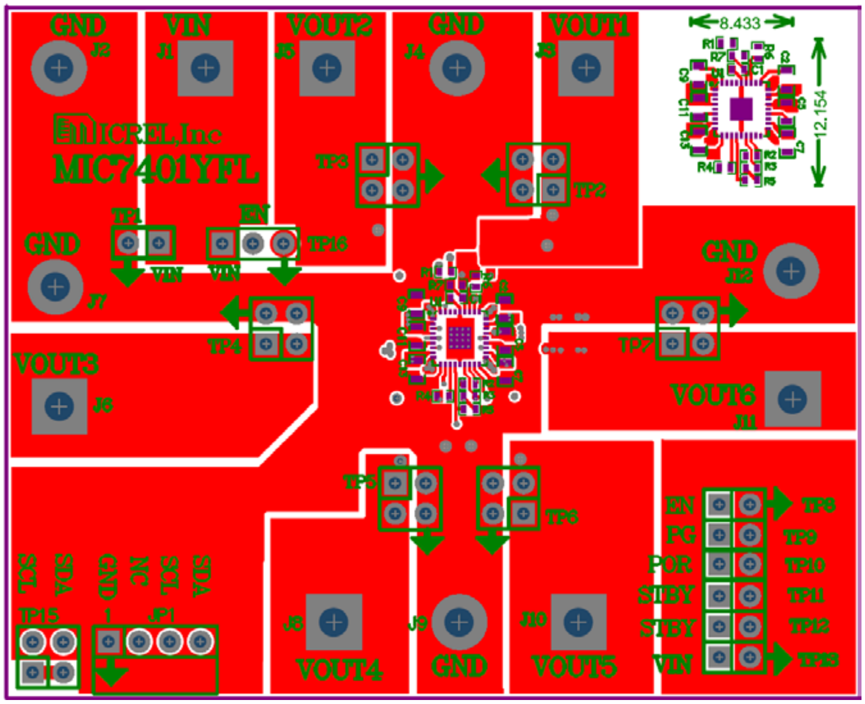


Evaluation Board Top Layer – Power Component Placement

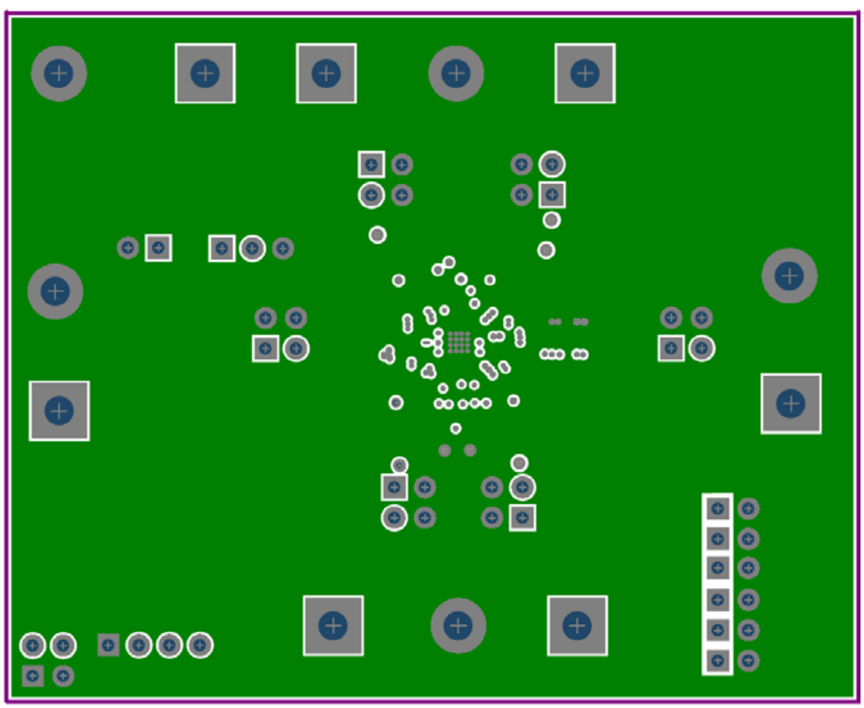


Evaluation Board Bottom Layer – Layer 6 (Power Routing Layer)

PCB Layout Recommendations (Continued)

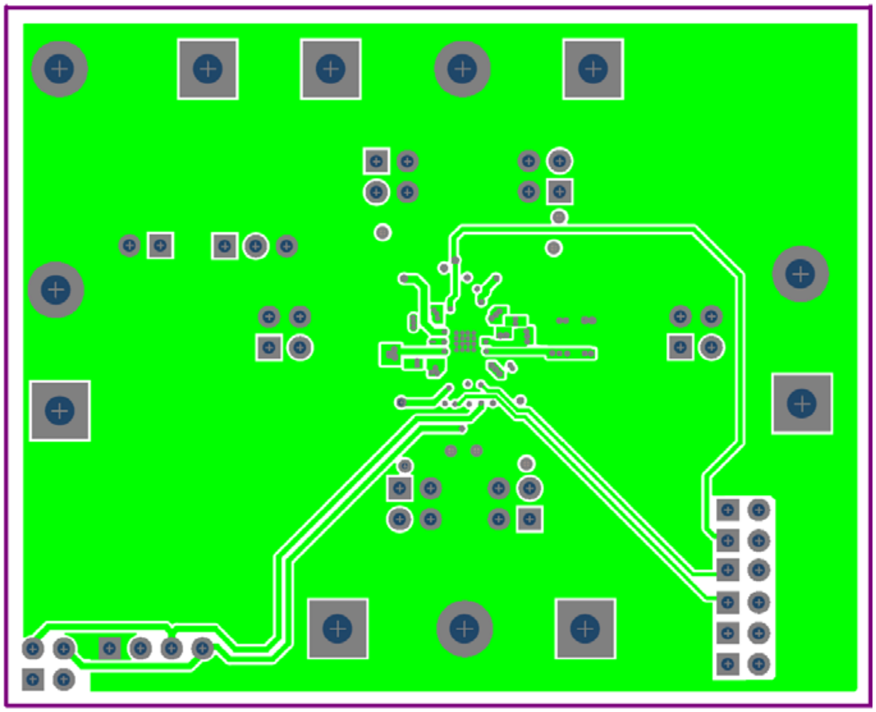


Evaluation Board Top Layer – Layer 1 (Power Routing Layer)

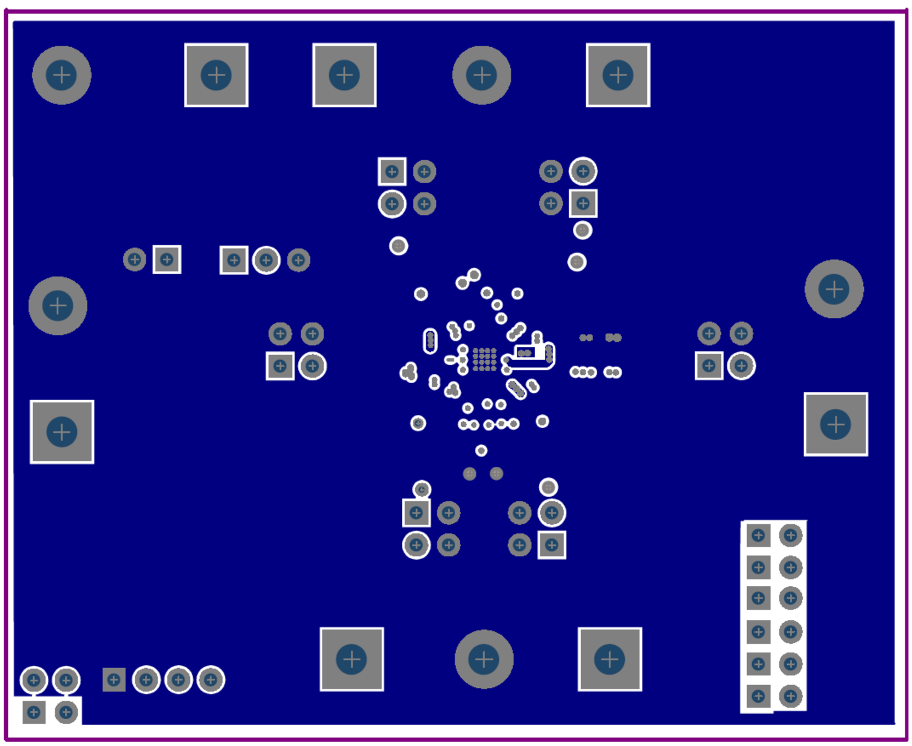


Evaluation Board Layer 2 (Ground Plane)

PCB Layout Recommendations (Continued)

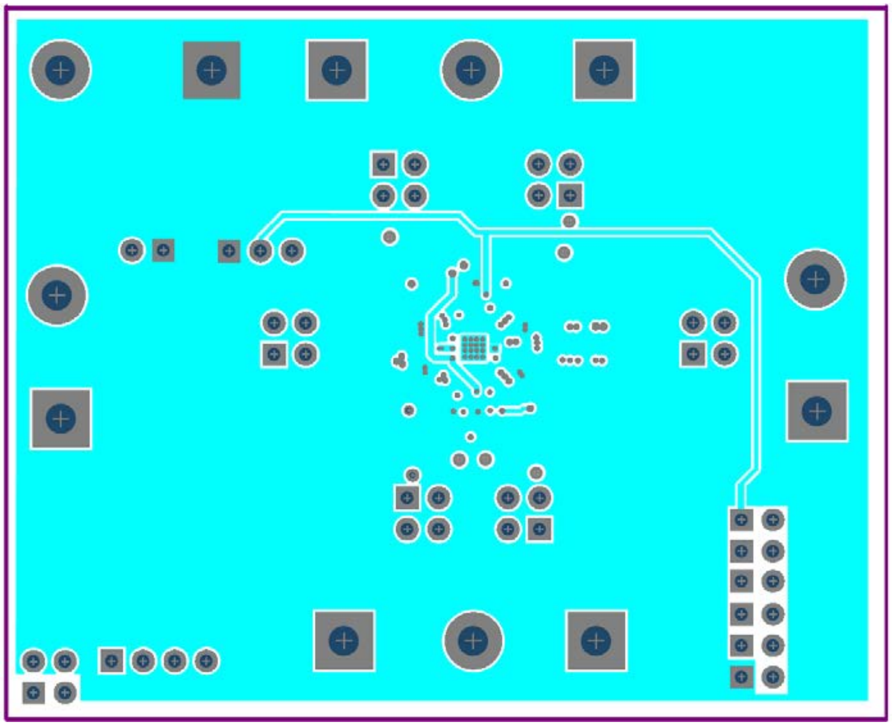


Evaluation Board Top Layer – Layer 3 (Signal Routing Layer)

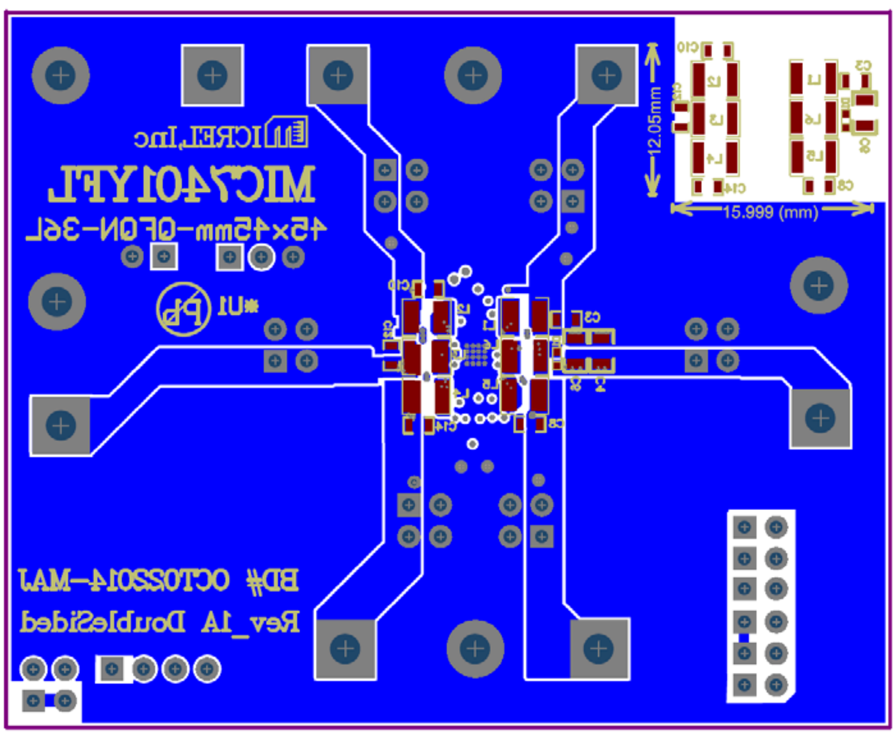


Evaluation Board Layer 4 (Ground Plane)

PCB Layout Recommendations (Continued)

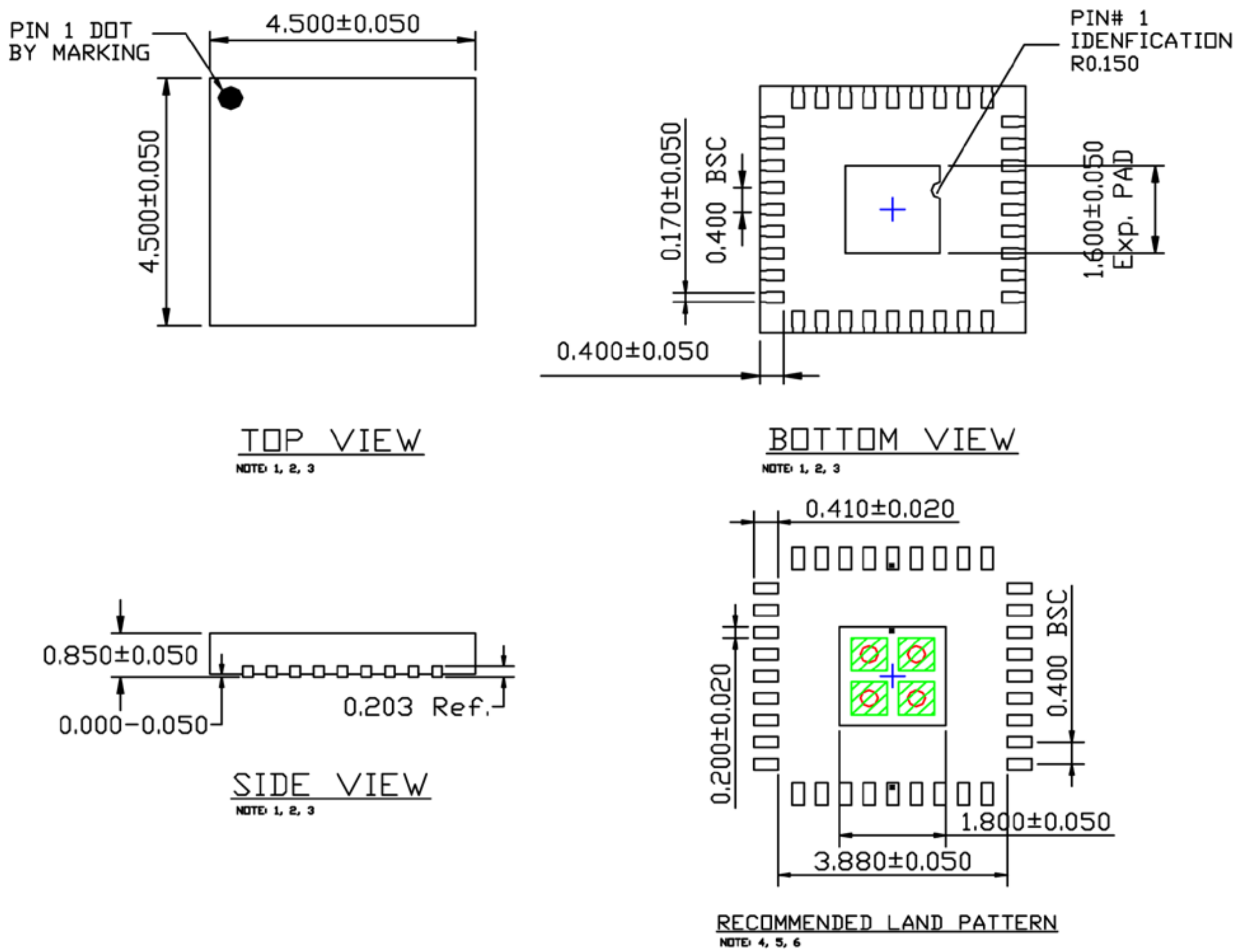


Evaluation Board Layer – Layer 5 (V_{IN} Plane)



Evaluation Board Bottom Later – Layer 6 (Ground Plane)

Package Information[17] and Recommended Landing Pattern



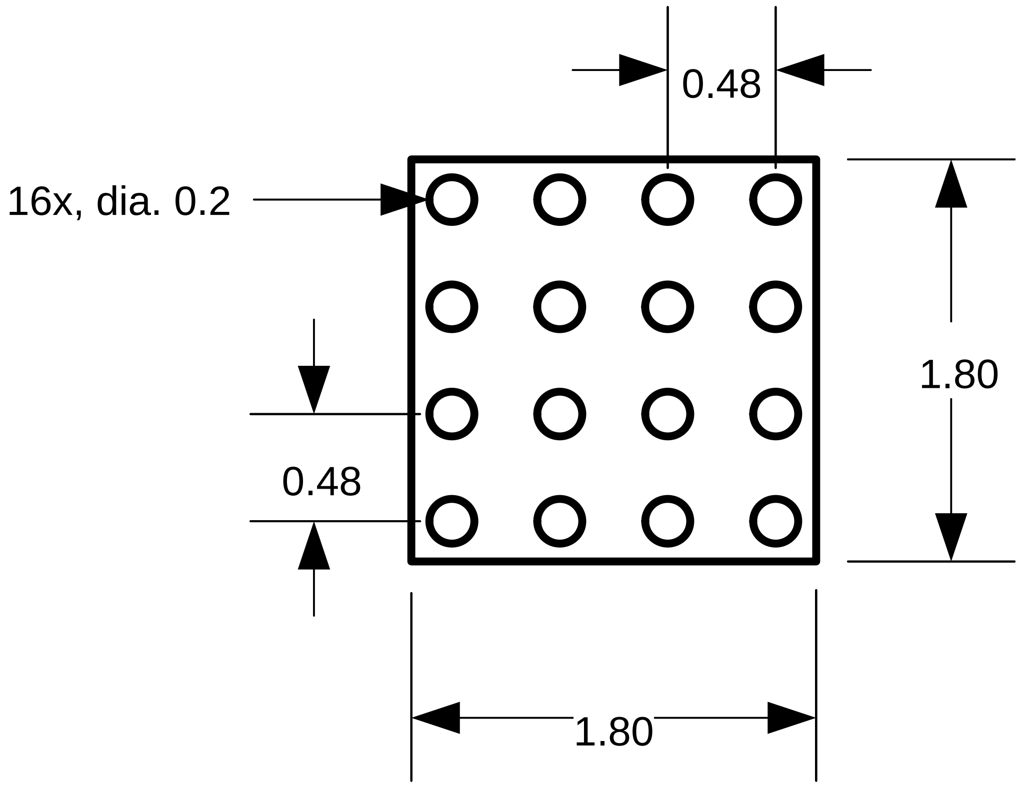
NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN REPRESENT THERMAL VIA. SIZE SHOULD BE 0.30-0.35MM IN DIAMETER, 0.8MM PITCH & MUST BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE
5. GREEN RECTANGLES (SHADED AREA, OPTIONAL) REPRESENT SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.60X0.60 MM IN SIZE, 0.20MM SPACING.
6. LAND PATTERN OPENINGS MARKED BY "*" (PINS#14, 32 & EPAD) ARE OF SAME GND AND SHOULD BE CONNECTED ON BOARD LEVEL FOR MAXIMUM THERMAL PERFORMANCE

36-Pin 4.5mm × 4.5mm FQFN (FL)

Note:

17. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

Via Layout Design and Layout Constraints



Via Layout Design

Notes:

Dimensions in millimeters (mm).

This package is designed to be soldered to a thermal pad on the board. Connect all ground planes together

Customers should contact their board fabrication site for recommended solder mask tolerance and via tenting recommendations for vias placed in the thermal pad.

Appendix A

I²C Control Register

The MIC7401 I²C Read/Write registers are detailed here. During normal operation, the configuration data can be saved into non-volatile registers in EEPROM by addressing the chip and writing to SAVECONFIG key = 66'h. Saving CONFIG data to EEPROM takes time so the external host should poll the MIC7401 and read the CONFIG Bit[1] of EEPROM Ready register 01'h to determine the end of programming.

All transactions start with a control byte sent from the I²C master device. The control byte begins with a START condition, followed by a 7-bit slave address. The slave address is seven bits long followed by an eighth bit which is a data direction bit (R/W), a '0' indicates a transmission (WRITE) and a '1' indicates a request for data (READ). A data transfer is always terminated by a STOP condition that is generated by the master.

Serial Port Operation

External Host Interface

Bidirectional I²C port capable of Standard (up to 100kbits/s), Fast (up to 400kbits/s), Fast Plus (up to 1Mbit/s) and High Speed (up to 3.4Mbit/s) as defined in the I²C-Bus Specification.

The MIC7401 acts as an I²C slave when addressed by the external host. The MIC7401 slave address uses a fixed 7-bit code and is followed by an R/W bit which is part of the control word that is right after the start bit as shown in Figure 22 in the Device Address column.

The MIC7401 can receive multiple data bytes after a single address byte and automatically increments its register pointer to block fill internal volatile memory. Byte data is latched after individual bytes are received so multi-byte transfers could be corrupted if interrupted mid-stream.

No system clock is required by the digital core for I²C access from the external host (only the host SCL clock is assumed).

In order to prevent spurious operation of the I²C, if a start bit is seen, then any partial communication is aborted and new I²C data is allowed. Start bit is when SDA goes low when SCL is high. Stop bit is when SDA goes high when SCL is high. Normal I²C exchange is shown in Figure 22.

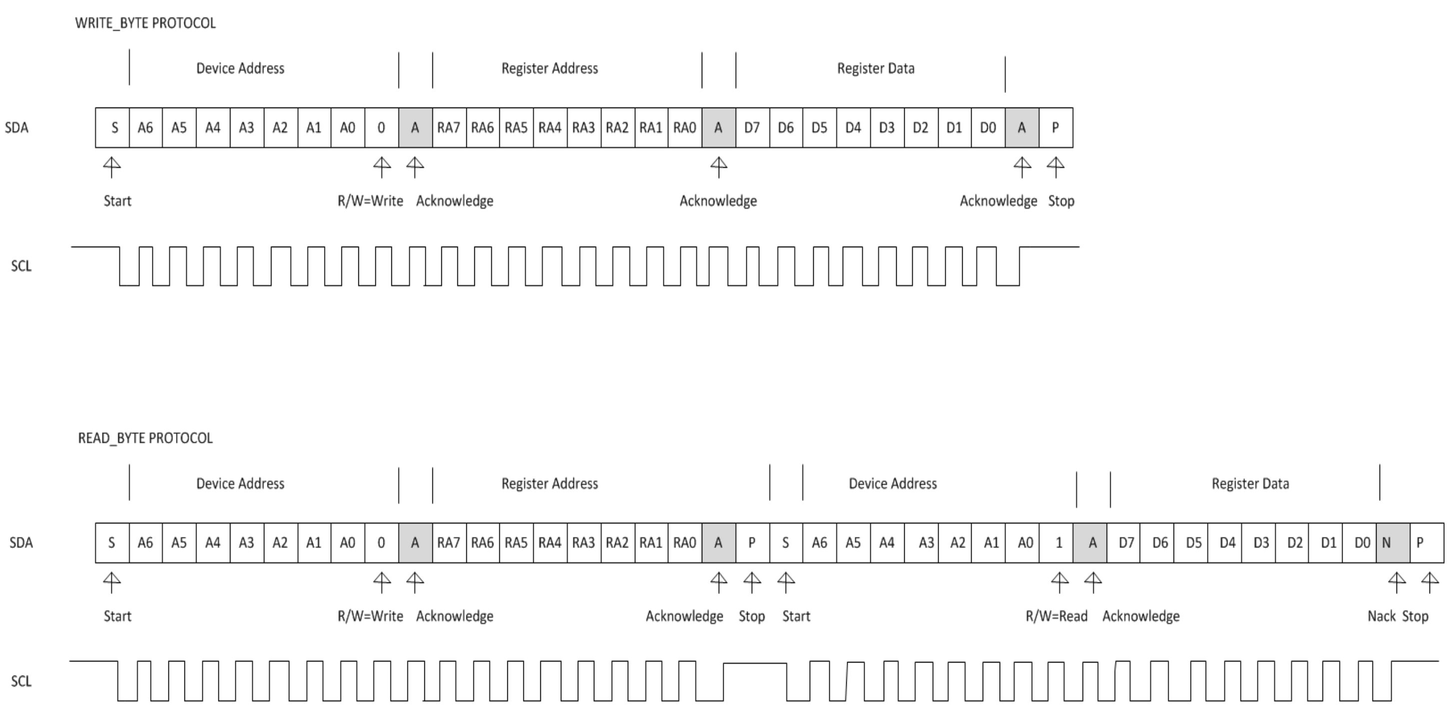


Figure 22. Read/Write Protocol

Special Host I^2C Commands

The following commands are all 2 byte communications:

Byte1 = device address with write bit set, LSB = 0

Byte2 = special key

Special Keys

- **SAVECONFIG Key = 66'h**. Saves the shadow register configuration data into EEPROM registers 03'h thru 23'h.
- **RESET Key = 6A'h**. Reloads only NORMAL mode voltage and current limit settings then enables the regulator to NORMAL mode with no soft-start, no sequencing, and no delays. Then clears the STANDBY register bit 6 in register 03'h.
- **RELOAD Key = 6B'h**. Reloads all data from EEPROM into the shadow registers. No other actions are performed, including soft-start, sequencing, and delay.
- **REBOOT Key = 6C'h**. Turns all regulators OFF, reloads EEPROM data into shadow registers, and then re-sequences the regulators with the programmed soft-start and sequence delays.
- **SEQUENCE Key = 6D'h**. Turns all regulators OFF, restarts the sequencer including soft-start and sequence delays.

Appendix B

Register Settings Descriptions

Power Good Register (00’h)

This register indicates when the regulators 1 – 6 output voltage is above 91% of the target value. The MIC7401 deglitches the input signal for 50µs in order to prevent false events. The global PG pin indicator is functional ‘AND’ of all the power good indicators during sequencing. Once the power-up sequence is complete, the global power good output stays high unless an output falls below its power-good limit, a thermal fault occurs, the input voltage drops below the lower UVLO threshold or an output is turned OFF by setting the enable register bit to “0” if the PGOOD_MASK[x] bit is set to “0”.

Table 5. Power Good Status Register

Register Name	**PGOOD1-6_REG**			**Power Good Status Register**	
Address				**0x00’h**	
Field	**bit**	**R/W**	**Default**	**Description**	
PGOOD1	0	R	0	Power Good Indicator for Regulator 1	
				0 = Buck Not Valid	1 = Buck Valid
PGOOD2	1	R	0	Power Good Indicator for Regulator 2	
				0 = Buck Not Valid	1 = Buck Valid
PGOOD3	2	R	0	Power Good Indicator for regulator 3	
				0 = Buck Not Valid	1 = Buck Valid
PGOOD4	3	R	0	Power Good Indicator for Regulator 4	
				0 = Buck Not Valid	1 = Buck Valid
PGOOD5	4	R	0	Power Good Indicator for Regulator 5	
				0 = Buck Not Valid	1 = Buck Valid
PGOOD6	5	R	0	Power Good Indicator for Regulator 6	
				0 = Boost Not Valid	1 = Boost Valid
Reserved	6	R/W	0	Not Used	
Reserved	7	R/W	0	Not Used	

EEPROM-Ready Register (01'h)

This register indicates the status of EEPROM to external I²C host.

The READY bit = 1 when the Trim and Configuration data have been loaded into core from EEPROM after reset, reboot or reload and the chip is ready for operation. [If the SAVE1 bit in register 04'h is read in as logic 1, the configuration registers will not be loaded from the EEPROM memory and the READY bit will still get set indicating that any startup procedure involving the EEPROM memory is complete.] The READY bit will be set to 1 after loading or attempting to load Trim and Configuration data from EEPROM into volatile memory. The Trim data will always be loaded and if SAVE1 bit in register 04'h is set to logic 0, Configuration data is also loaded. Regardless of the SAVE1 bit being set or not, after the loading operation the READY bit is set to 1.

The CONFIG bit = 1 when the Configuration data have been saved to EEPROM after the SAVECONFIG Code is issued from the Host. If CONFIG=1 before the SAVECONFIG code is issued, CONFIG will be cleared immediately and then will be set to logic 1 again once all Configuration data is written to the EEPROM memory.

The CALIB bit = 1 when the Trim data have been saved to EEPROM after the SAVETRIM Code is issued from the Host. If CALIB=1 before the SAVETRIM code is issued, CALIB will be cleared immediately and then will be set to logic 1 again once all Trim data is written to the EEPROM memory.

The EEPREAD and EEPWRITE bits indicate if an EEPROM read or write fault has occurred. These bits should be read and cleared prior to reloading data from the EEPROM memory.

Table 6. EEPROM Status Register

Register Name	STATUS_REG			**EEPROM Status Register**	
Address				0x01'h	
Field	**bit**	**R/W**	**Default**	**Description**	
READY	0	R	0	Indicate Ready for Operation when the Trim and Configuration Data has been Loaded	
				0 = Data not loaded	1 = Chip Ready
CONFIG	1	R	0	Indicate Configuration saved to EEPROM	
				0 = Configuration not saved	1 = Configuration Saved
CALIB	2	R	0	Indicate Trim Data have been Saved to EEROM	
				0 = Trim not saved	1 = Trim saved
Reserved	3	R/W	0	Not Used	
Reserved	4	R/W	0	Not Used	
Reserved	5	R/W	0	Not Used	
EEPREAD	6	R/W	0	EEPROM Read	
				0 = No Fault	1 = Fault
EEPWRITE	7	R/W	0	EEPROM Write	
				0 = No Fault	1 = Fault

Fault Registers (02'h)

This register indicates the over-current flag for each regulator and one global overtemperature (OT). These register bits are set by an over current condition and reset by writing a logic 0 to each bit by the I²C host.

If the fault condition persists, the bit will be set to Logic 1 again immediately by the MIC7401 after it is written to logic 0 by the host.

Table 7. Overcurrent Status Fault Register

Register Name	FAULT_REG			**Overcurrent Status Fault Register**	
Address				0x02'h	
Field	**bit**	**R/W**	**Default**	**Description**	
REG1OC	0	R/W	0	Regulator 1 Overcurrent	
				0 = No Fault	1 = Fault
REG2OC	1	R/W	0	Regulator 2 Overcurrent	
				0 = No Fault	1 = Fault
REG3OC	2	R/W	0	Regulator 3 Overcurrent	
				0 = No Fault	1 = Fault
REG4OC	3	R/W	0	Regulator 4 Overcurrent	
				0 = No Fault	1 = Fault
REG5OC	4	R/W	0	Regulator 5 Overcurrent	
				0 = No Fault	1 = Fault
REG6OC	5	R/W	0	Regulator 6 Overcurrent	
				0 = No Fault	1 = Fault
Reserved	6	R/W	0	Reserved	
OT	7	R/W	0	Overtemperature	
				0 = No Fault	1 = Fault

Standby Register (03'h)

This register controls standby mode operation. Global stand-by mode can either be enabled by I²C or by changing the logic state of the STBY input pin. Global stand-by is controlled by the STBY_MODEB bit. When STBY_MODEB [6] = 1 then the regulators output voltages are set to their normal-mode output voltage settings, (05'h – 0A'h) registers. When STBY_MODEB [6] = 0 then regulators output voltages are set to the standby-mode output voltage settings, (0B'h – 10'h) registers. If STBY [1-6] register is set to logic "0', then the output is shut off in standby mode.

The global power-good flag is asserted when an output is disabled unless the power-good mask bit (PGOOD_MASK[x]) is set to 1.

Table 8. Standby Register

Register Name	STBY_CTRL_REG			**Standby Register**	
Address				0x03'h	
Field	**bit**	**R/W**	**Default**	**Description**	
STBY1	0	R/W	1	Regulator 1 Standby Voltage Control	
				0 = OFF	1 = ON
STBY2	1	R/W	1	Regulator 2 Standby Voltage Control	
				0 = OFF	1 = ON
STBY3	2	R/W	1	Regulator 3 Standby Voltage Control	
				0 = OFF	1 = ON
STBY4	3	R/W	1	Regulator 4 Standby Voltage Control	
				0 = OFF	1 = ON
STBY5	4	R/W	1	Regulator 5 Standby Voltage Control	
				0 = OFF	1 = ON
STBY6	5	R/W	1	Regulator 6 Standby Voltage Control	
				0 = OFF	1 = ON
STBY_MODEB	6	R/W	1	Global Standby Control	
				0 = All regulators in Standby Mode	
				1 = All regulators in Normal Mode	
Reserved	7	R/W	0	Not Used	

Enable/Disable Register (04'h)

This register controls the enable/disable of each DC-to-DC regulators. When EN(n) bit transitions from 0 to 1 then the regulator(n) is enabled with Soft-Start unless the STBY_MODEB register bit in register 03'h is set to logic 0.

The configuration save bit "SAVE1" should be cleared by customer before saving configuration data to EEPROM. This bit is used during power-up to indicate via the Status register (00'h) that configuration data has previously been stored.

Table 9. Enable Register

Register Name	EN_REG			**Enable Register**	
Address				0x04'h	
Field	**bit**	**R/W**	**Default**	**Description**	
EN1	0	R/W	1	Regulator 1 ON/OFF Control bit	
				0 = OFF	1 = ON
EN2	1	R/W	1	Regulator 2 ON/OFF Control bit	
				0 = OFF	1 = ON
EN3	2	R/W	1	Regulator 3 ON/OFF Control	
				0 = OFF	1 = ON
EN4	3	R/W	1	Regulator 4 ON/OFF Control	
				0 = OFF	1 = ON
EN5	4	R/W	1	Regulator 5 ON/OFF Control	
				0 = OFF	1 = ON
EN6	5	R/W	1	Regulator 6 ON/OFF Control	
				0 = OFF	1 = ON
Reserved	6	R/W	0	Not Used	
SAVE1	7	R/W	0	Save Configuration	
				0 = Configuration Saved to EEPROM	
				1 = Not Configuration Saved to EEPROM	

Regulator Output Voltage Setting NORMAL Mode (05'h – 09'h)

One register for each regulator output (OUT1 – OUT5). Sets output voltage of regulator for NORMAL mode operation.

Table 10. DVC Registers for OUT[1 – 5]

Register Name	OUT1-5_REG			**DVC Registers for OUT[1-5]**			
Address				OUT1 = 0x05'h OUT2 = 0x06'h OUT3 = 0x07'h OUT4 = 0x08'h OUT5 = 0x09'h			
Field	**bit**	**R/W**	**Default**	**Description**			
OUT[1-5]	5:0	R/W	See Table 2	Output Voltage Setting of OUT[1-5], DVC from 3.3 V to 0.8V in –50mV Steps			
				000000 = 3.30V	010000 = 2.50V	100000 = 1.70V	110000 = 0.90V
				000001 = 3.25V	010001 = 2.45V	100001 = 1.65V	110001 = 0.85V
				000010 = 3.20V	010010 = 2.40V	100010 = 1.60V	110010 = 0.80V
				000011 = 3.15V	010011 = 2.35V	100011 = 1.55V	110011 = 0.80V
				000100 = 3.10V	010100 = 2.30V	100100 = 1.50V	110100 = 0.80V
				000101 = 3.05V	010101 = 2.25V	100101 = 1.45V	110101 = 0.80V
				000110 = 3.00V	010110 = 2.20V	100110 = 1.40V	110110 = 0.80V
				000111 = 2.95V	010111 = 2.15V	100111 = 1.35V	110111 = 0.80V
				001000 = 2.90V	011000 = 2.10V	101000 = 1.30V	111000 = 0.80V
				001001 = 2.85V	011001 = 2.05V	101001 = 1.25V	111001 = 0.80V
				001010 = 2.80V	011010 = 2.00V	101010 = 1.20V	111010 = 0.80V
				001011 = 2.75V	011011 = 1.95V	101011 = 1.15V	111011 = 0.80V
				001100 = 2.70V	011100 = 1.90V	101100 = 1.10V	111100 = 0.80V
				001101 = 2.65V	011101 = 1.85V	101101 = 1.05V	111101 = 0.80V
				001110 = 2.60V	011110 = 1.80V	101110 = 1.00V	111110 = 0.80V
				001111 = 2.55V	011111 = 1.75V	101111 = 0.95V	111111 = 0.80V
	6		0	Not Used			
	7		0	Not Used			

Boost Regulator Output Voltage Setting NORMAL Mode (0A'h)

Sets output voltage of the boost regulator (OUT6) in NORMAL mode operation.

Table 11. DVC Registers for OUT6

Register Name	OUT6_REG			**DVC Registers**			
Address				0x0A'h			
Field	**bit**	**R/W**	**Default**	**Description**			
OUT6	5:0	R/W	See Table 2	DVC from 14V to 7V in 200mV Decrements			
				000000 = 14.0V	010000 = 10.8V	100000 = 7.6V	110000 = 7.0V
				000001 = 13.8V	010001 = 10.6V	100001 = 7.4V	110001 = 7.0V
				000010 = 13.6V	010010 = 10.4V	100010 = 7.2V	110010 = 7.0V
				000011 = 13.4V	010011 = 10.2V	100011 = 7.0V	110011 = 7.0V
				000100 = 13.2V	010100 = 10.0V	100100 = 7.0V	110100 = 7.0V
				000101 = 13.0V	010101 = 9.8V	100101 = 7.0V	110101 = 7.0V
				000110 = 12.8V	010110 = 9.6V	100110 = 7.0V	110110 = 7.0V
				000111 = 12.6V	010111 = 9.4V	100111 = 7.0V	110111 = 7.0V
				001000 = 12.4V	011000 = 9.2V	101000 = 7.0V	111000 = 7.0V
				001001 = 12.2V	011001 = 9.0V	101001 = 7.0V	111001 = 7.0V
				001010 = 12.0V	011010 = 8.8V	101010 = 7.0V	111010 = 7.0V
				001011 = 11.8V	011011 = 8.6V	101011 = 7.0V	111011 = 7.0V
				001100 = 11.6V	011100 = 8.4V	101100 = 7.0V	111100 = 7.0V
				001101 = 11.4V	011101 = 8.2V	101101 = 7.0V	111101 = 7.0V
				001110 = 11.2V	011110 = 8.0V	101110 = 7.0V	111110 = 7.0V
				001111 = 11.0V	011111 = 7.8V	101111 = 7.0V	111111 = 7.0V
	6		0	Not Used			
	7		0	Not Used			

Regulator Voltage Setting STBY Mode (0B'h – 0F'h)

This register is used to sets the output voltage of regulators 1 – 5 in STBY mode operation.

Table 12. Standby Registers

<table>
<tr><td>Register Name</td><td colspan="3">STBY_ OUT1-5_REG</td><td colspan="4">Standby DVC Registers</td></tr>
<tr><td>Address</td><td colspan="3"></td><td colspan="4">OUT1 = 0x0B'h
OUT2 = 0x0C'h
OUT3 = 0x0D'h
OUT4 = 0x0E'h
OUT5 = 0x0F'h</td></tr>
<tr><td>Field</td><td>bit</td><td>R/W</td><td>Default</td><td colspan="4">Description</td></tr>
<tr><td rowspan="17">SB_OUT[1-5]</td><td rowspan="17">5:0</td><td rowspan="17">R/W</td><td rowspan="17">See Table 2</td><td colspan="4">Output Voltage Setting of OUT[1-5], DVC from 3.3V to 0.8V in –50mV Steps</td></tr>
<tr><td>000000 = 3.30V</td><td>010000 = 2.50V</td><td>100000 = 1.70V</td><td>110000 = 0.90V</td></tr>
<tr><td>000001 = 3.25V</td><td>010001 = 2.45V</td><td>100001 = 1.65V</td><td>110001 = 0.85V</td></tr>
<tr><td>000010 = 3.20V</td><td>010010 = 2.40V</td><td>100010 = 1.60V</td><td>110010 = 0.80V</td></tr>
<tr><td>000011 = 3.15V</td><td>010011 = 2.35V</td><td>100011 = 1.55V</td><td>110011 = 0.80V</td></tr>
<tr><td>000100 = 3.10V</td><td>010100 = 2.30V</td><td>100100 = 1.50V</td><td>110100 = 0.80V</td></tr>
<tr><td>000101 = 3.05V</td><td>010101 = 2.25V</td><td>100101 = 1.45V</td><td>110101 = 0.80V</td></tr>
<tr><td>000110 = 3.00V</td><td>010110 = 2.20V</td><td>100110 = 1.40V</td><td>110110 = 0.80V</td></tr>
<tr><td>000111 = 2.95V</td><td>010111 = 2.15V</td><td>100111 = 1.35V</td><td>110111 = 0.80V</td></tr>
<tr><td>001000 = 2.90V</td><td>011000 = 2.10V</td><td>101000 = 1.30V</td><td>111000 = 0.80V</td></tr>
<tr><td>001001 = 2.85V</td><td>011001 = 2.05V</td><td>101001 = 1.25V</td><td>111001 = 0.80V</td></tr>
<tr><td>001010 = 2.80V</td><td>011010 = 2.00V</td><td>101010 = 1.20V</td><td>111010 = 0.80V</td></tr>
<tr><td>001011 = 2.75V</td><td>011011 = 1.95V</td><td>101011 = 1.15V</td><td>111011 = 0.80V</td></tr>
<tr><td>001100 = 2.70V</td><td>011100 = 1.90V</td><td>101100 = 1.10V</td><td>111100 = 0.80V</td></tr>
<tr><td>001101 = 2.65V</td><td>011101 = 1.85V</td><td>101101 = 1.05V</td><td>111101 = 0.80V</td></tr>
<tr><td>001110 = 2.60V</td><td>011110 = 1.80V</td><td>101110 = 1.00V</td><td>111110 = 0.80V</td></tr>
<tr><td>001111 = 2.55V</td><td>011111 = 1.75V</td><td>101111 = 0.95V</td><td>111111 = 0.80V</td></tr>
<tr><td></td><td>6</td><td></td><td>0</td><td colspan="2">Not Used</td><td colspan="2"></td></tr>
<tr><td></td><td>7</td><td></td><td>0</td><td colspan="2">Not Used</td><td colspan="2"></td></tr>
</table>

Boost Regulator Output Voltage Setting STBY Mode (10’h)

Sets output voltage of the boost regulator (OUT6) for STBY mode operation.

Table 13. Standby DVC Register for OUT6

Register Name	STBY _OUT6_REG			**DVC Registers**			
Address				0x10’h			
Field	**bit**	**R/W**	**Default**	**Description**			
SB_OUT6	5:0	R/W	See Table 2	DVC from 14V to 7V in 200mV decrements			
				000000 = 14.0V	010000 = 10.8V	100000 = 7.6V	110000 = 7.0V
				000001 = 13.8V	010001 = 10.6V	100001 = 7.4V	110001 = 7.0V
				000010 = 13.6V	010010 = 10.4V	100010 = 7.2V	110010 = 7.0V
				000011 = 13.4V	010011 = 10.2V	100011 = 7.0V	110011 = 7.0V
				000100 = 13.2V	010100 = 10.0V	100100 = 7.0V	110100 = 7.0V
				000101 = 13.0V	010101 = 9.8V	100101 = 7.0V	110101 = 7.0V
				000110 = 12.8V	010110 = 9.6V	100110 = 7.0V	110110 = 7.0V
				000111 = 12.6V	010111 = 9.4V	100111 = 7.0V	110111 = 7.0V
				001000 = 12.4V	011000 = 9.2V	101000 = 7.0V	111000 = 7.0V
				001001 = 12.2V	011001 = 9.0V	101001 = 7.0V	111001 = 7.0V
				001010 = 12.0V	011010 = 8.8V	101010 = 7.0V	111010 = 7.0V
				001011 = 11.8V	011011 = 8.6V	101011 = 7.0V	111011 = 7.0V
				001100 = 11.6V	011100 = 8.4V	101100 = 7.0V	111100 = 7.0V
				001101 = 11.4V	011101 = 8.2V	101101 = 7.0V	111101 = 7.0V
				001110 = 11.2V	011110 = 8.0V	101110 = 7.0V	111110 = 7.0V
				001111 = 11.0V	011111 = 7.8V	101111 = 7.0V	111111 = 7.0V
	6		0	Not Used			
	7		0	Not Used			

Sequence Register (11'h)

Each regulator can be assigned to start in any one of six sequencing slots (1 to 6). If starting in slot 1, the regulator starts immediately. If starting in any other slot the regulator must wait for the PGOOD=1 flags of all regulators assigned to the preceding slot and then wait for the specified delay time (register 17'h) i.e., all PGOODs in preceding state flag then the delay timer is started and when delay completes the regulator is enabled.

Each regulator must delay its startup (after the appropriate preceding PGOOD flags) by the delay set in the Delay Register (17'h), unless the regulator is assigned to sequence state 0.

If all default Enable bits = 0 the IC starts up, but no outputs are enabled.

Sequencing is only used during initial startup, and not used when outputs are enabled via I²C command. If outputs are enabled via I²C then soft-start is still active but start-up delays (timed from preceding PGOODS) are not.

Table 14. Sequence State 1 Register

Register Name	SEQ1_REG			**Sequence Register**	
Address				0x11'h	
Field	**bit**	**R/W**	**Default**	**Description**	
REG1SQ1	0	R/W	0	0 = No Start	1 = Regulator 1 will Start in Sequence State 1
REG2SQ1	1	R/W	0	0 = No Start	1 = Regulator 2 will Start in Sequence State 1
REG3SQ1	2	R/W	0	0 = No Start	1 = Regulator 3 will Start in Sequence State 1
REG4SQ1	3	R/W	1	0 = No Start	1 = Regulator 4 will Start in Sequence State 1
REG5SQ1	4	R/W	0	0 = No Start	1 = Regulator 5 will Start in Sequence State 1
REG6SQ1	5	R/W	0	0 = No Start	1 = Regulator 6 will Start in Sequence State 1
	6	R/W	0	Reserved	
	7	R/W	0	Reserved	

Table 15. Sequence State 2 Register

Register Name	SEQ2_REG			Sequence Register	
Address				0x12'h	
Field	**bit**	**R/W**	**Default**	**Description**	
REG1SQ2	0	R/W	0		
				0 = No Start	1 = Regulator 1 will Start in Sequence State 2
REG2SQ2	1	R/W	1		
				0 = No Start	1 = Regulator 2 will Start in Sequence State 2
REG3SQ2	2	R/W	1		
				0 = No Start	1 = Regulator 3 will Start in Sequence State 2
REG4SQ2	3	R/W	0		
				0 = No Start	1 = Regulator 4 will Start in Sequence State 2
REG5SQ2	4	R/W	0		
				0 = No Start	1 = Regulator 5 will Start in Sequence State 2
REG6SQ2	5	R/W	0		
				0 = No Start	1 = Regulator 6 will Start in Sequence State 2
	6	R/W	0	Reserved	
	7	R/W	0	Reserved	

Table 16. Sequence State 3 Register

Register Name	SEQ3_REG			Sequence Register	
Address				0x13'h	
Field	**bit**	**R/W**	**Default**	**Description**	
REG1SQ3	0	R/W	1		
				0 = No Start	1 = Regulator 1 will Start in Sequence State 3
REG2SQ3	1	R/W	0		
				0 = No Start	1 = Regulator 2 will Start in Sequence State 3
REG3SQ3	2	R/W	0		
				0 = No Start	1 = Regulator 3 will Start in Sequence State 3
REG4SQ3	3	R/W	0		
				0 = No Start	1 = Regulator 4 will Start in Sequence State 3
REG5SQ3	4	R/W	0		
				0 = No Start	1 = Regulator 5 will Start in Sequence State 3
REG6SQ3	5	R/W	0		
				0 = No Start	1 = Regulator 6 will Start in Sequence State 3
	6	R/W	0	Reserved	
	7	R/W	0	Reserved	

Table 17. Sequence State 4 Register

Register Name	SEQ4_REG			Sequence Register	
Address				0x14'h	
Field	**bit**	**R/W**	**Default**	**Description**	
REG1SQ4	0	R/W	0		
				0 = No Start	1 = Regulator 1 will Start in Sequence State 4
REG2SQ4	1	R/W	0		
				0 = No Start	1 = Regulator 2 will Start in Sequence State 4
REG3SQ4	2	R/W	0		
				0 = No Start	1 = Regulator 3 will Start in Sequence State 4
REG4SQ4	3	R/W	0		
				0 = No Start	1 = Regulator 4 will Start in Sequence State 4
REG5SQ4	4	R/W	1		
				0 = No Start	1 = Regulator 5 will Start in Sequence State 4
REG6SQ4	5	R/W	0		
				0 = No Start	1 = Regulator 6 will Start in Sequence State 4
	6	R/W	0	Reserved	
	7	R/W	0	Reserved	

Table 18. Sequence State 5 Register

Register Name	SEQ5_REG			Sequence Register	
Address				0x15'h	
Field	**bit**	**R/W**	**Default**	**Description**	
REG1SQ5	0	R/W	0		
				0 = No Start	1 = Regulator 1 will Start in Sequence State 5
REG2SQ5	1	R/W	0		
				0 = No Start	1 = Regulator 2 will Start in Sequence State 5
REG3SQ5	2	R/W	0		
				0 = No Start	1 = Regulator 3 will Start in Sequence State 5
REG4SQ5	3	R/W	0		
				0 = No Start	1 = Regulator 4 will Start in Sequence State 5
REG5SQ5	4	R/W	0		
				0 = No Start	1 = Regulator 5 will Start in Sequence State 5
REG6SQ5	5	R/W	0		
				0 = No Start	1 = Regulator 6 will Start in Sequence State 5
	6	R/W	0	Reserved	
	7	R/W	0	Reserved	

Table 19. Sequence State 6 Register

Register Name	SEQ6_REG			Sequence Register	
Address				0x16'h	
Field	**bit**	**R/W**	**Default**	**Description**	
REG1SQ6	0	R/W	0		
				0 = No Start	1 = Regulator 1 will Start in Sequence State 6
REG2SQ6	1	R/W	0		
				0 = No Start	1 = Regulator 2 will Start in Sequence State 6
REG3SQ6	2	R/W	0		
				0 = No Start	1 = Regulator 3 will Start in Sequence State 6
REG4SQ6	3	R/W	0		
				0 = No Start	1 = Regulator 4 will Start in Sequence State 6
REG5SQ6	4	R/W	0		
				0 = No Start	1 = Regulator 5 will Start in Sequence State 6
REG6SQ6	5	R/W	1		
				0 = No Start	1 = Regulator 6 will Start in Sequence State 6
	6	R/W	0	Reserved	
	7	R/W	0	Reserved	

Delay Register (17'h)

The STDEL register sets the delay between powering up of each regulator at initial power-up (see Figure 19). Once all the internal power-good registers PGOOD[1-6] are all 1, then the global PG pin goes high without delay.

The PORDEL register sets the delay for the POR flag pin. The POR delay time starts as soon as AVIN pin voltage rises above the system UVLO upper threshold set by the PORUP register (21'h). The POR output goes low without delay if AVIN falls below the lower UVLO threshold set by the PORDN register (22'h).

Table 20. Delay Register

Register Name	DELAY_CNTL_REG			Delay Register			
Address				0x17'h			
Field	**bit**	**R/W**	**Default**	**Description**			
STDEL	2:0	R/W	001 (1ms)	Delay Time from 0ms to 7ms in 1ms Increments			
				000 = 0ms	010 = 2ms	100 = 4ms	110 = 6ms
				001 = 1ms	011 = 3ms	101 = 5ms	111 = 7ms
PORDEL	7:3	R/W	00011 (20ms)	Delay Time from 5ms to 160ms in 5ms Increments			
				00000 = 5ms	01000 = 45ms	10000 = 85ms	11000 = 125ms
				00001 = 10ms	01001 = 50ms	10001 = 90ms	11001 = 130ms
				00010 = 15ms	01010 = 55ms	10010 = 95ms	11010 = 135ms
				00011 = 20ms	01011 = 60ms	10011 = 100ms	11011 = 140ms
				00100 = 25ms	01100 = 65ms	10100 = 105ms	11100 = 145ms
				00101 = 30ms	01101 = 70ms	10101 = 110ms	11101 = 150ms
				00110 = 35ms	01110 = 75ms	10110 = 115ms	11110 = 155ms
				00111 = 40ms	01111 = 80ms	10111 = 120ms	11111 = 160ms

Soft-Start Registers (18'h – 1A'h)

When regulator(n) is turned on from either the Enable Register (04'h) in NORMAL mode or from the Standby Register (03'h) in STANDBY mode, then the three REG(n)SS soft-start bits are used to control both the rising and falling ramp rate of the outputs.

In NORMAL mode, the outputs are stepped from the current regulator voltage settings to a newly-programmed regulator voltage setting or to the default value.

On power up, the regulator voltage output is set to the lowest possible voltage setting which is 3F'h. The voltage regulator will change by one step or increment at a time. The amount of time between each step is controlled by the soft-start registers. Table 21 details the amount of time for each encoded soft-start value.

Table 21. Soft-Start Register Speed Settings

	R/W	Default	Description			
SS_SPEED = 0	R/W	000	Soft-Start Time from 4µs to 512µs			
			000 = 4µs	010 = 16µs	100 = 64µs	110 = 256µs
			001 = 8µs	011 = 32µs	101 = 128µs	111 = 512µs
SS_SPEED = 1	R/W	000	Soft-Start Time from 8µs to 1024µs			
			000 = 8µs	010 = 32µs	100 = 128µs	110 = 512µs
			001 = 16µs	011 = 64µs	101 = 256µs	111 = 1024µs

Table 22. Soft-Start Register OUT1 and OUT2

Register Name	SS1-2_REG			Soft-Start Register for V_{OUT1} and V_{OUT2}	
Address				0x18'h	
Field	**bit**	**R/W**	**Default**	**Description**	
REG1SS	2:0	R/W	001 (8µs)	OUT1 Soft-Start Time	
				See Table 19 for Soft-Start Settings	
REG2SS	5:3	R/W	001 (8µs)	OUT2 Soft-Start Time	
				See Table 19 for Soft-Start Settings	
	6	R/W	0	Reserved	
SS_SPEED	7	R/W	0	Set the speed of the clock to slow or fast for different clock division, see Table 19.	
				0 = Slow Speed	1 = Fast Speed

Table 23. Soft-Start Register OUT3 and OUT4

Register Name	SS3-4_REG			Soft-Start Register for V_{OUT3} and V_{OUT4}	
Address				0x19'h	
Field	**bit**	**R/W**	**Default**	**Description**	
REG3SS	2:0	R/W	001 (8µs)	OUT3 Soft-Start Time	
				See Table 19 for Soft-Start Settings	
REG4SS	5:3	R/W	001 (8µs)	OUT4 Soft-Start Time	
				See Table 19 for Soft-Start Settings	
	6	R/W	0	Reserved	
	7	R/W	0	Reserved	

Table 24. Soft-Start Register OUT5 and OUT6

Register Name	SS5-6_REG			**Soft-Start Register for V_{OUT5} and V_{OUT6}**
Address				0x1A'h
Field	**bit**	**R/W**	**Default**	**Description**
REG5SS	2:0	R/W	001 (8µs)	OUT5 Soft-Start Time See Table 19 for Soft-Start Settings
REG6SS	5:3	R/W	010 (16µs)	OUT6 Soft-Start Time See Table 19 for Soft-Start Settings
	6	R/W	0	Reserved
	7	R/W	0	Reserved

Current-Limit (Normal Mode) Registers (1B'h – 1D'h)

This register is use to set the current limit for each DC-to-DC regulator in normal mode operation.

Table 25. Current-Limit Register I_{OUT1} and I_{OUT2}

Register Name	ILIMIT_1-2_REG			**Current-Limit Register for V_{OUT1} and V_{OUT2}**			
Address				0x1B'h			
Field	**bit**	**R/W**	**Default**	**Description**			
REG1CL	3:0	R/W	1000 (4.1A)	Normal Current-Limit for Regulator 1 from 8.1A to 0.6A in 0.5A Decrements			
				0000 = 8.6A	0100 = 6.6A	1000 = 4.6A	1100 = 2.6 A
				0001 = 8.1A	0101 = 6.1A	1001 = 4.1A	1101 = 2.1A
				0010 = 7.6A	0110 = 5.6A	1010 = 3.6A	1110 = 1.6A
				0011 = 7.1A	0111 = 5.1A	1011 = 3.1A	1111 = 1.1A
REG2CL	7:4	R/W	1000 (4.1A)	Normal Current-Limit for Regulator 2 from 8.1A to 0.6A in 0.5A Decrements			
				0000 = 8.6A	0100 = 6.6A	1000 = 4.6A	1100 = 2.6 A
				0001 = 8.1A	0101 = 6.1A	1001 = 4.1A	1101 = 2.1A
				0010 = 7.6A	0110 = 5.6A	1010 = 3.6A	1110 = 1.6A
				0011 = 7.1A	0111 = 5.1A	1011 = 3.1A	1111 = 1.1A

Table 26. Current-Limit Register I_{OUT3} and I_{OUT4}

Register Name	ILIMIT_3-4_REG			**Current-Limit Register for V_{OUT3} and V_{OUT4}**			
Address				0x1C'h			
Field	**bit**	**R/W**	**Default**	**Description**			
REG3CL	3:0	R/W	1000 (4.1A)	Normal Current-Limit for Regulator 3 from 8.1A to 0.6A in 0.5A Decrements			
				0000 = 8.6A	0100 = 6.6A	1000 = 4.6A	1100 = 2.6 A
				0001 = 8.1A	0101 = 6.1A	1001 = 4.1A	1101 = 2.1A
				0010 = 7.6A	0110 = 5.6A	1010 = 3.6A	1110 = 1.6A
				0011 = 7.1A	0111 = 5.1A	1011 = 3.1A	1111 = 1.1A
REG4CL	7:4	R/W	0100 (6.1A)	Normal Current-Limit for Regulator 4 from 8.1A to 0.6A in 0.5A Decrements			
				0000 = 8.6A	0100 = 6.6A	1000 = 4.6A	1100 = 2.6 A
				0001 = 8.1A	0101 = 6.1A	1001 = 4.1A	1101 = 2.1A
				0010 = 7.6A	0110 = 5.6A	1010 = 3.6A	1110 = 1.6A
				0011 = 7.1A	0111 = 5.1A	1011 = 3.1A	1111 = 1.1A

Table 27. Current-Limit Register I_{OUT5} and I_{OUT6}

Register Name	ILIMIT_5-6_REG			**Current-Limit Register for V_{OUT5} and V_{OUT6}**			
Address				0x1D'h			
Field	**bit**	**R/W**	**Default**	**Description**			
REG5CL	3:0	R/W	1000 (4.1A)	Normal Current-Limit for Regulator 5 from 8.1A to 0.6A in 0.5A Decrements			
				0000 = 8.6A	0100 = 6.6A	1000 = 4.6A	1100 = 2.6 A
				0001 = 8.1A	0101 = 6.1A	1001 = 4.1A	1101 = 2.1A
				0010 = 7.6A	0110 = 5.6A	1010 = 3.6A	1110 = 1.6A
				0011 = 7.1A	0111 = 5.1A	1011 = 3.1A	1111 = 1.1A
REG6CL	6:4	R/W	011 (2.24A)	Current Limit from 2.6A to 1.78A in 0.12A Decrements			
				000 = 2.6A	010 = 2.36A	100 = 2.12A	110 = 1.88A
				001 = 2.48A	011 = 2.24A	101 = 2.00A	111 = 1.76A
	7	R/W	0	0 = Current Limit On		1 = Current Limit Off	

Current-Limit (STBY Mode) Registers (1E – 20’h)

This register is use to set the current limit for each DC-to-DC regulator when in standby (STBY) mode operation.

Table 28. Standby Current-Limit Register I_{OUT1} and I_{OUT2}

Register Name	STBY_ILIMIT_1-2_REG			Standby Current-Limit Register for V_{OUT1} and V_{OUT2}			
Address				0x1E’h			
Field	**bit**	**R/W**	**Default**	**Description**			
SB1CL	3:0	R/W	1000 (4.1A)	Standby current limit for regulator 1 from 8.6A to 0.6A in 0.5A decrements			
				0000 = 8.6A	0100 = 6.6A	1000 = 4.6A	1100 = 2.6 A
				0001 = 8.1A	0101 = 6.1A	1001 = 4.1A	1101 = 2.1A
				0010 = 7.6A	0110 = 5.6A	1010 = 3.6A	1110 = 1.6A
				0011 = 7.1A	0111 = 5.1A	1011 = 3.1A	1111 = 1.1A
SB2CL	7:4	R/W	1000 (4.1A)	Standby current limit for regulator 2 from 8.6A to 0.6A in 0.5A decrements			
				0000 = 8.6A	0100 = 6.6A	1000 = 4.6A	1100 = 2.6 A
				0001 = 8.1A	0101 = 6.1A	1001 = 4.1A	1101 = 2.1A
				0010 = 7.6A	0110 = 5.6A	1010 = 3.6A	1110 = 1.6A
				0011 = 7.1A	0111 = 5.1A	1011 = 3.1A	1111 = 1.1A

Table 29. Standby Current-Limit Register I_{OUT3} and I_{OUT4}

Register Name	STBY_ILIMIT_3-4_REG			Standby Current-Limit Register for V_{OUT3} and V_{OUT4}			
Address				0x1F’h			
Field	**bit**	**R/W**	**Default**	**Description**			
SB3CL	3:0	R/W	1000 (4.1A)	Standby Current Limit for Regulator 3 from 8.1A to 0.6A in 0.5A Decrements			
				0000 = 8.6A	0100 = 6.6A	1000 = 4.6A	1100 = 2.6 A
				0001 = 8.1A	0101 = 6.1A	1001 = 4.1A	1101 = 2.1A
				0010 = 7.6A	0110 = 5.6A	1010 = 3.6A	1110 = 1.6A
				0011 = 7.1A	0111 = 5.1A	1011 = 3.1A	1111 = 1.1A
SB4CL	7:4	R/W	0100 (6.1A)	Standby Current Limit for Regulator 4 from 8.1A to 0.6 A in 0.5A Decrements			
				0000 = 8.6A	0100 = 6.6A	1000 = 4.6A	1100 = 2.6 A
				0001 = 8.1A	0101 = 6.1A	1001 = 4.1A	1101 = 2.1A
				0010 = 7.6A	0110 = 5.6A	1010 = 3.6A	1110 = 1.6A
				0011 = 7.1A	0111 = 5.1A	1011 = 3.1A	1111 = 1.1A

Table 30. Standby Current-Limit Register I_{OUT5} and I_{OUT6}

Register Name	STBY_ILIMIT_5-6_REG			**Standby Current-Limit Register for V_{OUT5} and V_{OUT6}**			
Address				0x20'h			
Field	**bit**	**R/W**	**Default**	**Description**			
SB5CL	3:0	R/W	1000 (4.1A)	Standby Current Limit for Regulator 5 from 8.1A to 0.6A in 0.5A Decrements			
				0000 = 8.6A	0100 = 6.6A	1000 = 4.6A	1100 = 2.6 A
				0001 = 8.1A	0101 = 6.1A	1001 = 4.1A	1101 = 2.1A
				0010 = 7.6A	0110 = 5.6A	1010 = 3.6A	1110 = 1.6A
				0011 = 7.1A	0111 = 5.1A	1011 = 3.1A	1111 = 1.1A
SB6CL	6:4	R/W	011 (2.24A)	Current Limit from 2.6A to 1.78A in 0.12A Decrements			
				000 = 2.6A	010 = 2.36A	100 = 2.12A	110 = 1.88A
				001 = 2.48A	011 = 2.24A	101 = 2.00A	111 = 1.76A
	7	R/W	0	0 = Current Limit On		1 = Current Limit Off	

Power-on-Reset (POR) Threshold Voltage Setting Register (21'h and 22'h)

This register is used to set the rising and falling threshold of power-on-reset (POR) comparator. Refer to Table 20 for POR time delay settings.

Table 31. Rising and Falling Power-on-Reset Threshold Voltage Settings

				Rising and Falling Power On Reset Threshold Voltage Setting			
	bit	**R/W**	**Default**	**Description**			
VSCLT	4:0	R/W	00000	3.3V to 2.3V in 50mV Decrements			
				00000 = 3.25V	01000 = 2.85V	10000 = 2.45V	11000 = 2.25V
				00001 = 3.20V	01001 = 2.80V	10001 = 2.40V	11001 = 2.25V
				00010 = 3.15V	01010 = 2.75V	10010 = 2.35V	11010 = 2.25V
				00011 = 3.10V	01011 = 2.70V	10011 = 2.30V	11011 = 2.25V
				00100 = 3.05V	01100 = 2.65V	10100 = 2.25V	11100 = 2.25V
				00101 = 3.00V	01101 = 2.60V	10101 = 2.25V	11101 = 2.25V
				00110 = 2.95V	01110 = 2.55V	10110 = 2.25V	11110 = 2.25V
				00111 = 2.90V	01111 = 2.50V	10111 = 2.25V	11111 = 2.25V

The three most significant bits [7:5] in Registers 21'h and 22'h are used to mask the output voltage power-good flag after the start-up sequenced is finished.

Table 32. Power-on-Reset Rising Threshold Voltage Setting Register (21'h)

Register Name	PORUO_REG			**Power-on-Reset Falling Threshold**	
Address				0x21'h	
Field	**bit**	**R/W**	**Default**	**Description**	
PORUP	4:0	R/W	01011 (2.7V)	See Table 28	
PGOOD_MASK1	5	R/W	1	0 = Do Not Mask PGOOD1	1 = Mask PGOOD1
PGOOD_MASK2	6	R/W	1	0 = Do Not Mask PGOOD2	1 = Mask PGOOD2
PGOOD_MASK3	7	R/W	1	0 = Do Not Mask PGOOD3	1 = Mask PGOOD3

Table 33. Power-on-Reset Falling Threshold Voltage Setting Register (22'h)

Register Name	PORDN_REG			Power-on-Reset Falling Threshold	
Address				0x22'h	
Field	**bit**	**R/W**	**Default**	**Description**	
PORDN	4:0	R/W	01101 (2.6V)	See Table 28	
PGOOD_MASK4	5	R/W	1	0 = Do Not Mask PGOOD4	1 = Mask PGOOD4
PGOOD_MASK5	6	R/W	1	0 = Do Not Mask PGOOD5	1 = Mask PGOOD5
PGOOD_MASK6	7	R/W	1	0 = Do Not Mask PGOOD6	1 = Mask PGOOD6

Pull-Down when Disabled Register (23'h)

This register is used to set the preference of enabling/disabling a pull-down FET when the DC-to-DC regulators are disabled. The pull-down value for buck regulators 1 – 5 is 90Ω. The pull-down current value for the boost regulator 6 is programmable.

Table 34. Pull-Down when Disabled Register

Register Name	PULLDN1-6_REG			Pull-Down when Disabled Register			
Address				0x23'h			
Field	**bit**	**R/W**	**Default**	**Description**			
PULLD1	0	R/W	0	Enable/Disable the Pull-Down on Regulator 1 when Power-Down			
				0 = No Pull Down		1 = Pull-Down	
PULLD2	1	R/W	0	Enable/Disable the Pull-Down on Regulator 2 when Power-Down			
				0 = No Pull-Down		1 = Pull-Down	
PULLD3	2	R/W	0	Enable/Disable the Pull-Down on Regulator 3 when Power-Down			
				0 = No Pull-Down		1 = Pull Down	
PULLD4	3	R/W	0	Enable/Disable the Pull-Down on Regulator 4 when Power-Down			
				0 = No Pull-Down		1 = Pull-Down	
PULLD5	4	R/W	0	Enable/Disable the Pull-Down on Regulator 5 when Power-Down			
				0 = No Pull-Down		1 = Pull-Down	
PULLD6C	6:5	R/W	00	Sets Boost Pull-Down Current Level			
				00 = 148mA	01 = 111mA	10 = 74mA	11 = 37mA
PULLD6	7	R/W	0	Enable/Disable the Pull-Down on Regulator 6 when Power-Down			
				0 = No Pull-Down		1 = Pull-Down	

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http://www.micrel.com

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