DATA SHEET
03 NOVEMBER 2003

No. 00022
REV 1-03

REPLACEMENT OF:
UC 3714
UC 3715

MIK371x family

COMPLEMENTARY SWITCH FET DRIVERS

DESCRIPTION

The MIK3714 and the MIK3715 are two families of high speed drivers. These are designed to provide drive waveforms for complementary switches. Complementary switch configurations are commonly used in synchronous rectification circuits and active clamp/reset circuits, which can provide zero voltage switching. In order to facilitate the soft switching transitions, independently programmable delays between the two output waveforms are provided on these drivers. The delay pins also have true zero voltage sensing capability which allows immediate activation of the corresponding switch when zero voltage is applied. These devices require a PWM-type input to operate and can be interfaced with commonly available PWM controllers.

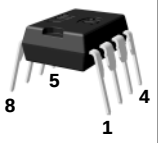
In the MIK3714 series, the AUX output is inverted to allow driving a P-channel MOSFET. In the MIK3715 series the two outputs are configured in a true complementary fashion.

FEATURES

- Single Input (PWM and TTL Compatible)
- High Current Power FET Driver, 1.0A Source/2A Sink
- Auxiliary Output FET Driver, 0.5A Source/1A Sink
- Time Delays Between Power and Auxiliary Outputs Independently Programmable from 50 ns to 500 ns
- Time Delay or True Zero-Voltage Operation Independently Configurable for Each Output
- Switching Frequency to 1MHz
- Typical 50 ns Propagation Delays
- ENBL Pin Activates 220 µA Sleep Mode
- Power Output is Active Low in Sleep Mode
- Synchronous Rectifier Driver

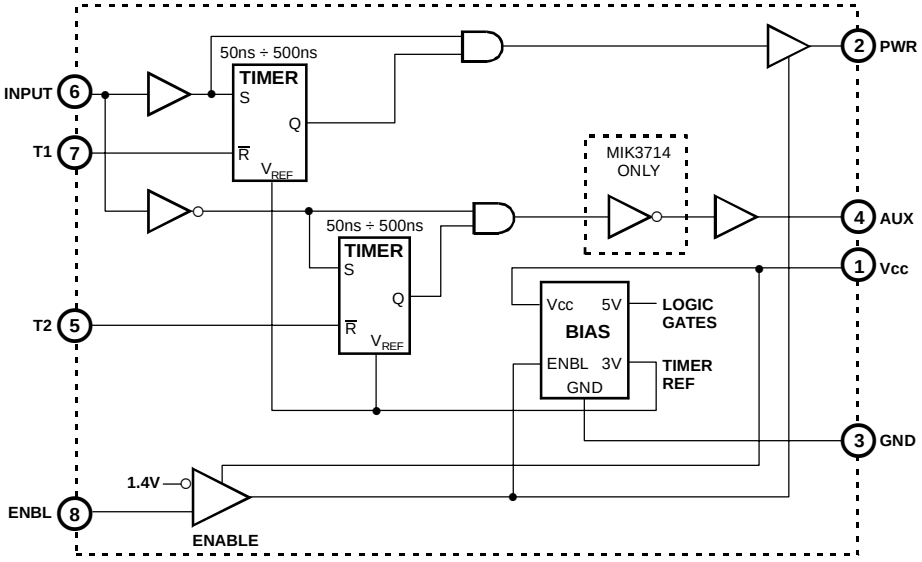
PIN CONNECTION AND DESCRIPTION

PIN NAME	DESCRIPTION
AUX	The AUX switches immediately at INPUT`S rising edge but waits through the T2 delay after INPUT'S falling edge before switching. AUX is capable of sourcing 0.5A and sinking 1.0A of drive current. See the Time Relationships diagram below for the difference between the MIK3714 and MIK3715 for INPUT, MAIN, and AUX. During sleep mode, AUX is inactive with a high impedance.
ENBL	The ENBL input switches at TTL logic levels (approximately 1.2V), and its input range is from 0V to 20V. The ENBL input will place the device into sleep mode when it is a logical low. The current into Vcc during the sleep mode is typically 220mA.

	MIK371x **N**	MIK371x **D**
1 — Vcc **2 — PWR** **3 — GND** **4 — AUX** **5 — T2** **6 — INPUT** **7 — T1** **8 — ENBL**	**DIP-8**  	**SOP-8** 

GND	This is the reference pin for all input voltages and the return point for all device currents. It carries the full peak sinking current from the outputs. Any tendency for the outputs to ring below GND voltage must be damped or clamped such that GND remains the most negative potential.
INPUT	The input switches at TTL logic levels (approximately 1.4V) but the allowable range is from 0V to 20V, allowing direct connection to most common IC PWM controller outputs. The rising edge immediately switches the AUX output, and initiates a timing delay, T1, before switching on the PWR output. Similarly, the INPUT falling edge immediately turns off the PWR output and initiates a timing delay, T2, before switching the AUX output. It should be noted that if the input signal comes from a controller with FET drive capability, this signal provides another option. INPUT and PWR provide a delay only at the leading edge while INPUT and AUX provide the delay at the trailing edge.
PWR	The PWR output waits for the T1 delay after the INPUT`S rising edge before switching on, but switches off immediately at INPUT`S falling edge (neglecting propagation delays). This output is capable of sourcing 1A and sinking 2A of peak gate drive current. PWR output includes a passive, self-biased circuit which holds this pin active low, when ENBL ≥ 0.8V regardless of Vcc's voltage.
T1	A resistor to ground programs the time delay between AUX switch turn-off and PWR turn-on.
T2	This pin functions in the same way as T1 but controls the time delay between PWR turn-off and activation of the AUX switch.
T1, T2	The resistor on each of these pins sets the charging current on internal timing capacitors to provide independent time control. The nominal voltage level at each pin is 3V and the current is internally limited to 1mA. The total delay from INPUT to each output includes a propagation delay in addition to the programmable timer but since the propagation delays are approximately equal, the relative time delay between the two outputs can be assumed to be solely a function of the programmed delays. The relationship of the time delay vs. RT is shown in the Typical Characteristics curves. Either or both pins can alternatively be used for voltage sensing in lieu of delay programming. This is done by pulling the timer pins below their nominal voltage level which immediately activates the timer output.
V_{CC}	The Vcc input range is from 7V to 20V. This pin should be bypassed with a capacitor to GND consistent with peak load current demands.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		MAXIMUM	UNIT
V_{CC}	Supply Voltage (low impedance source)		20	V
I_{OH}	Power Driver	continuous	-200	mA
		peak	-1	A
I_{OL}	Power Driver	continuous	400	mA
		peak	2	A
I_{OH}	Auxiliary Driver	continuous	-100	mA
		peak	-500	
I_{OL}	Auxiliary Driver	continuous	200	mA
		peak	1	A
INPUT, ENBL	Input Voltage Range		-0.3 to 20	V
	Storage Temperature Range		-65 to 150	°C
	Operating Junction Temperature (Note 1)		150	
	Lead Temperature (Soldering 10 seconds)		300	

Note 1: Unless otherwise indicated, voltages are referenced to ground and currents are positive info, negative out of, the specified terminals.

ELECTRICAL CHARACTERISTICS

(V_{CC}=15V, **ENBL** ≥ 2V, R_T**1**=100kΩ from **T1** to GND, R_T**2**=100kΩ from **T2** to GND, and T_A=0°C to +70°C, T_A = T_J unless otherwise stated)

SYMBOL	CHARACTERISTICS	TEST CONDITION	MIN	TYP	MAX	UNIT
OVERALL						
V_{CC}	V_{CC}		7		20	V
I_{CC}	I_{CC}, nominal	ENBL = 2.0V		18	24	mA
$I_{CC\ sleep}$	I_{CC}, sleep mode	ENBL = 0.8V		200	300	µA
POWER DRIVER (PWR)						
V_{OL} **Pre Turn-on**	Pre Turn-on PWR Output, Low	V_{CC} = 0V, I_{OUT} = 10mA, ENBL= 0.8V		0.3	1.6	V
V_{OL}	PWR Output Low, Sat. (V_{PWR})	INPUT= 0.8V, I_{OUT}= 40 mA		0.3	0.8	
		INPUT= 0.8V, I_{OUT}= 400 mA		2.1	2.8	
V_{OH}	PWR Output High, Sat. (V_{CC} -V_{PWR})	INPUT= 2.0V, I_{OUT}= -20 mA		2.1	3	
		INPUT= 2.0V, I_{OUT}= -200 mA		2.3	3	
Tr	Rise Time	C_L = 2200pF		30	60	ns
Tf	Fall Time	C_L = 2200pF		25	60	
T1 delay	T1 Delay, AUX to PWR	INPUT= rising edge, R_T1= 10kΩ (Note 3)	20	35	80	
T1 delay	T1 Delay, AUX to PWR	INPUT= rising edge, R_T1=100kΩ (Note 3)	350	500	700	
Tpd	PWR Prop Delay	INPUT falling edge, 50% (Note 2)		35	100	
AUXILIARY DRIVER (AUX)						
V_{OL}	AUX Output Low, Sat (V_{AUX})	V_{IN} = 2.0V, I_{OUT} = 20mA		0.3	0.8	V
		V_{IN} = 2.0V, I_{OUT} = 200mA		1.8	2.6	
V_{OH}	AUX Output High, Sat (V_{CC} -V_{AUX})	V_{IN} = 0.8V, I_{OUT} = -10mA		2.1	3.0	
		V_{IN} = 0.8V, I_{OUT} = -100mA		2.3	3.0	
Tr	Rise Time	C_L = 1000pF		45	60	ns
Tf	Fall Time	C_L = 1000pF		30	60	
T2 delay	T2 Delay, AUX to PWR	INPUT= rising edge, R_T2= 10kΩ (Note 3)	20	50	80	
T2 delay	T2 Delay, AUX to PWR	INPUT= rising edge, R_T2=100kΩ (Note 3)	250	350	550	
Tpd	AUX Prop Delay	INPUT falling edge, 50% (Note 2)		35	80	

Continuation of the table on the next page ...

ELECTRICAL CHARACTERISTICS (CONTINUED)

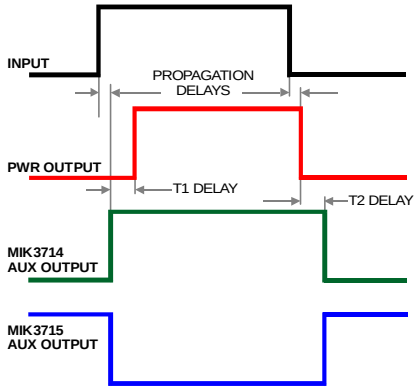
(V_{CC}=15V, **ENBL** ≥ 2V, R_T1=100kΩ from **T1** to **GND**, R_T2=100kΩ from **T2** to **GND**, and T_A=0°C to +70°C, T_A = T_J unless otherwise stated)

ENABLE (ENBL)						
Vth	Input Threshold		0.8	1.2	2.0	V
I_{IH}	Input Current, I_{IH}	ENBL = 15V		1	10	µA
I_{IL}	Input Current, I_{IL}	ENBL = 0V		-1	-10	µA
T1						
I_{LIM}	Current Limit	T1 = 0V		-1.6	-2	mA
V_{T1}	Nominal Voltage at T1		2.7	3	3.3	V
TdZVS	Minimum T1 Delay	T1 = 2.5V (Note 3)		40	70	ns
T2						
I_{LIM}	Current Limit	T2 = 0V		-1.2	-2	mA
V_{T2}	Nominal Voltage at T2		2.7	3	3.3	V
TdZVS	Minimum T2 Delay	T2 = 2.5V (Note 3)		50	100	ns
INPUT (INPUT)						
Vth	Input Threshold		0.8	1.4	2.0	V
I_{IH}	Input Current, I_{IH}	INPUT = 15V		1	10	µA
I_{IL}	Input Current, I_{IL}	INPUT = 0V		-5	-20	µA

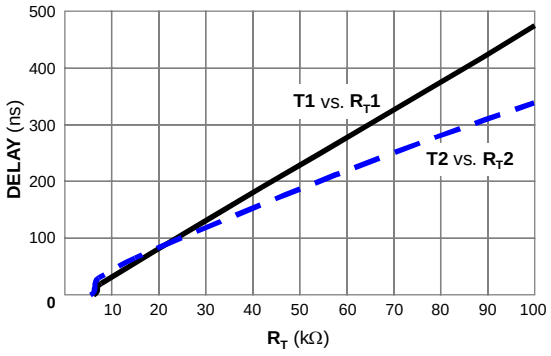
Note 2: Propagation delay times are measured from the 50% point of the input signal to the 10% point of the output signal's transition with no load on outputs.
Note 3: T1 delay is defined from the 50% point of the transition edge of AUX to the 10% of the rising edge of PWR. T2 delay is defined from the 90% of the falling edge of PWR to the 50% point of the transition edge of AUX.

TYPICAL CHARACTERISTICS

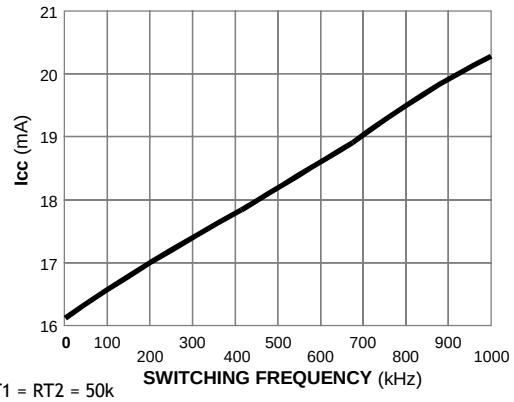
TIME RELATIONSHIPS (NOTES 2, 3)



T1 DELAY, T2 DELAY VS. R_T

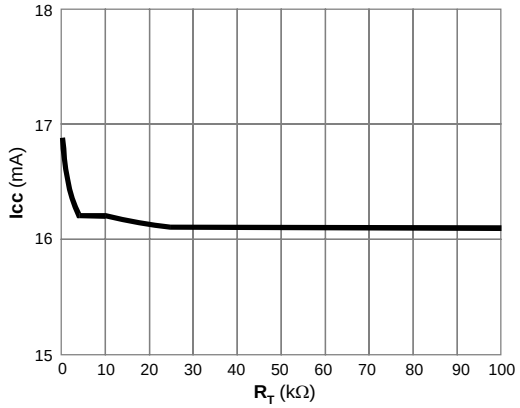


ICC VS. SWITCHING FREQUENCY



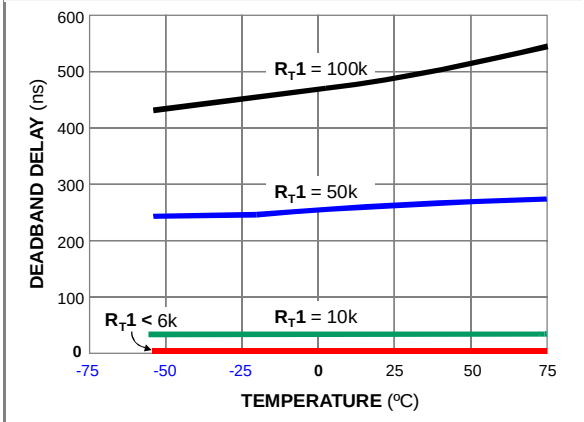
RT1 = RT2 = 50k
Duty Cycle = 50%
No Load

ICC VS. R_T WITH OPPOSITE R_T = 50K

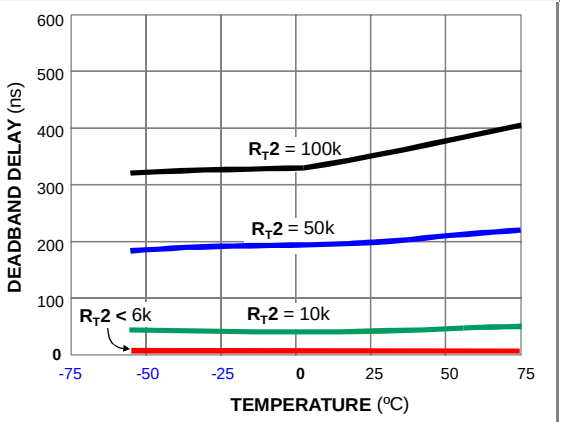


TYPICAL CHARACTERISTICS (CONTINUED)

T1 DEADBAND VS. TEMPERATURE AUX TO PWR

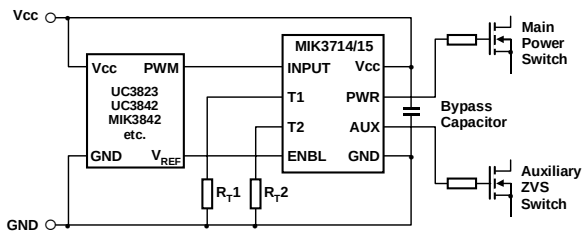


T2 DEADBAND VS. TEMPERATURE PWR TO AUX

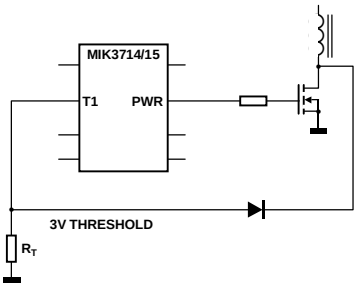


TYPICAL APPLICATIONS

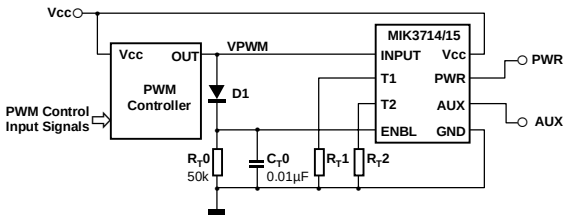
TYPICAL APPLICATION WITH TIMED DELAYS



USING THE TIMER INPUT FOR ZERO-VOLTAGE SENSING

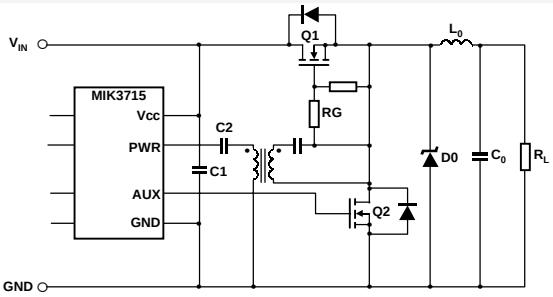


SELF-ACTUATED SLEEP MODE WITH THE ABSENCE OF AN INPUT PWM SIGNAL

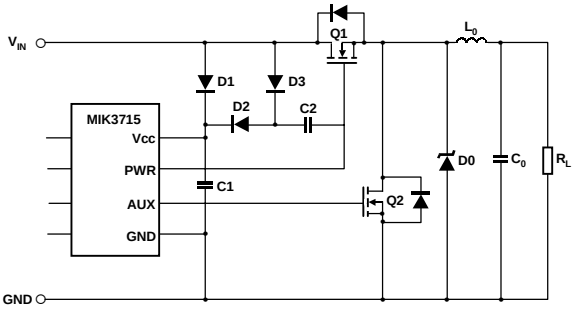


WAKE UP OCCURS WITH THE FIRST PULSE WHILE TURN-OFF IS DETERMINED BY THE (RTO CTO) TIME CONSTANT

USING AS A COMPLEMENTARY SYNCHRONOUS RECTIFIER SWITCH DRIVER WITH N-CHANNEL FETS

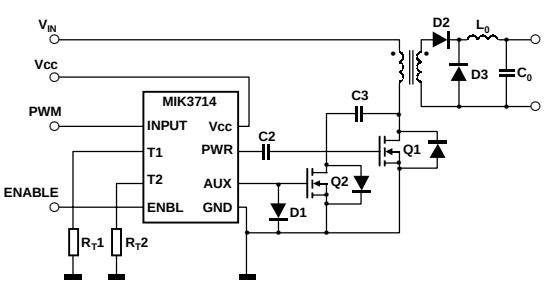


SYNCHRONOUS RECTIFIER APPLICATION WITH A CHARGE PUMP TO DRIVE THE HIGH-SIDE N-CHANNEL BUCK SWITCH



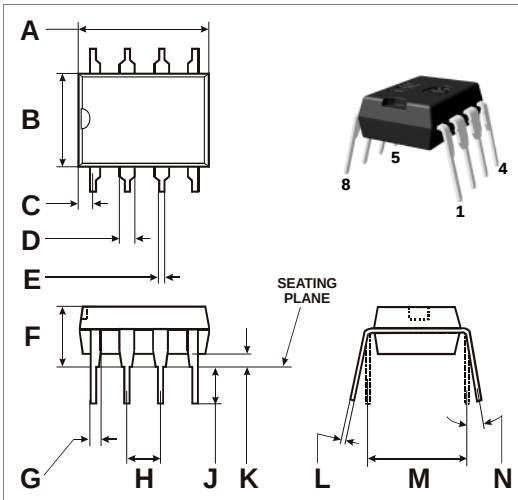
V_{IN} is limited to 10V as Vcc will rise to approximately $2V_{IN}$

TYPICAL FORWARD CONVERTER TOPOLOGY WITH ACTIVE RESET PROVIDED BY THE MIK3714 DRIVING AN N-CHANNEL SWITCH (Q1) AND A P-CHANNEL AUXILIARY SWITCH (Q2)



PHYSICAL DIMENSIONS AND MARKING DIAGRAMS

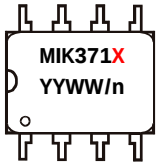
DIP-8 PACKAGE



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9,35	9,45	0,368	0,372
B	6.30	6.40	0,248	0,252
C	0,84	0,94	0,033	0,037
D		1.82		0,072
E	0,41	0,51	0,016	0,020
F	3,75	4,35	0,148	0,171
G	0,94	1,04	0,037	0,041
H	2,49	2,59	0,098	0,102
J	3.00	3.50	0,118	0,138
K	0.50	1.10	0,020	0,043
L	0.20	0.30	0,008	0,012
M	7.57	7.67	0,298	0,302
N		10°		10°

DIP-8

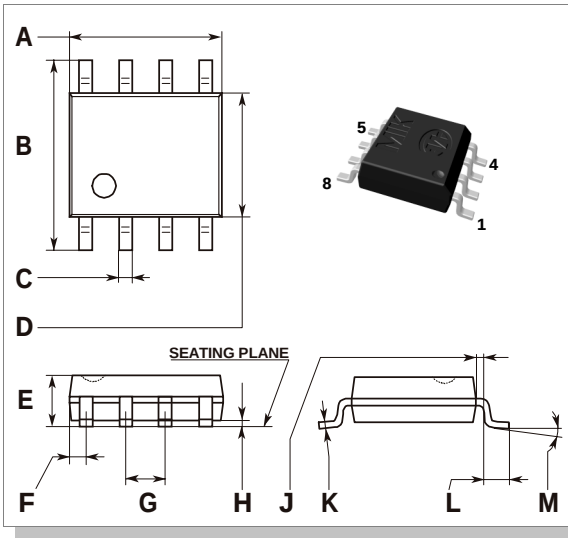
MARKING DIAGRAM



X – see table below
Y – Year
WW – Work Week
n – assembly location

X	SUBFAMILY
4	MIK3714
5	MIK3715

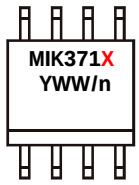
SOP-8 PACKAGE



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.78	4.91	0.188	0.193
B	5.96	6.12	0.235	0.241
C	0.406		0.016	
D	3.89	3.99	0.153	0.157
E	1.60	1.70	0.063	0.067
F	0.30	0.70	0.012	0.028
G	1.27		0.050	
H	0.20		0.008	
J	0.32		0.013	
K	0.203		0.008	
L	1.05		0.041	
M	1°	5°	1°	5°

SOP-8

MARKING DIAGRAM



X – see table below
Y – Year
WW – Work Week
n – assembly location

X	SUBFAMILY
4	MIK3714
5	MIK3715

ORDERING INFORMATION

ORDERING NUMBER	PACKAGE	OPERATING TEMPERATURE	SHIPPING
MIK 3714 **N**	DIP-8	0°C to +70°C	50 units/Tube
MIK 3715 **N**			
MIK 3714 **D**	SOP-8	0°C to +70°C	100 units/Tube 2500 units/Reel
MIK 3715 **D**			

NOTE: The form of packing is stipulated in the contract.

MIKRON JSC Head Office

Address: 1ST Zapadny Proezd 12, Building 1, Zelenograd, Moscow, Russia, 124460
Telephone: +7 (095) 535-23-43; 536-85-44
Fax: +7 (095) 530-92-01
Email: export@mikron.ru

MIKRON ShenZhen Office

Tel/Fax: +86-755-329-7574
Voice: +86-755-329-7573
Email: miksz@963.net