

# MIP3550MS

Silicon MOS FET type integrated circuit

## ■ Features

- Expanding the range of input / output
- High-efficiency and the reduction of coil sound
- Lower the average noise
- Protecting function (overload protection, over voltage protection, overheat protection)

## ■ Applications

- IH rice cooker, air conditioners, air purification system, dehumidifier, washing machines and fan motor (for refrigerators)

## ■ Package

- Code  
DIP7-A1
- Pin Name
 

1. f	5. DRAIN
2. VDD	6. —
3. CL	7. SOURCE
4. FB	8. SOURCE

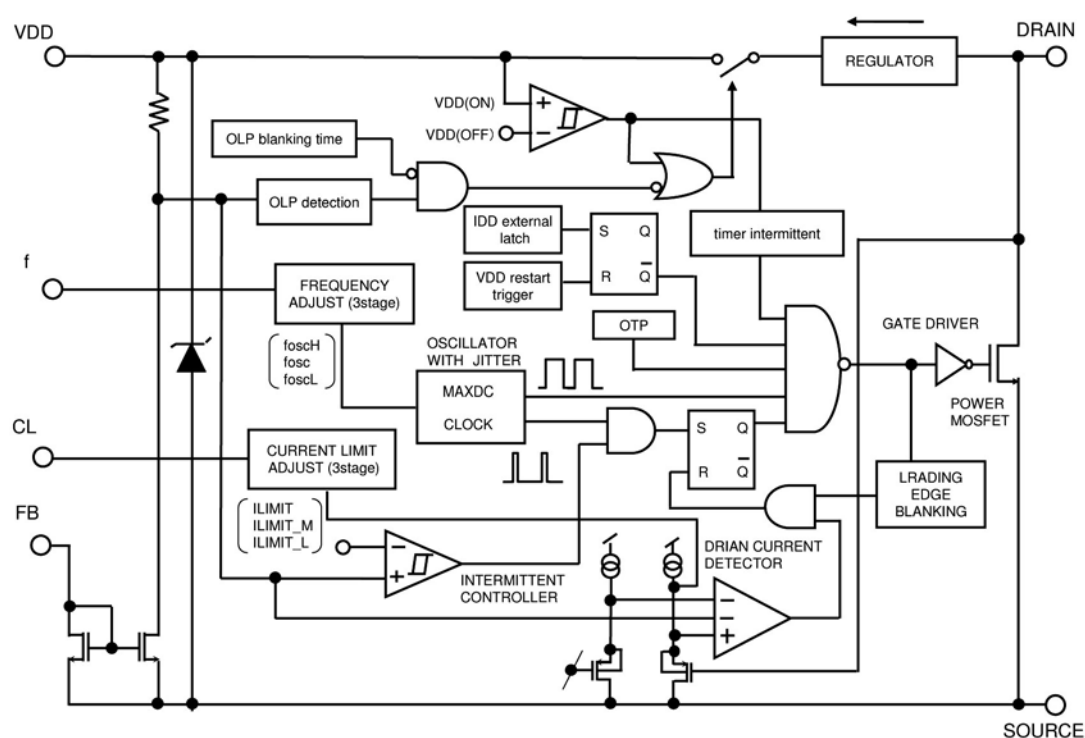
## ■ Marking Symbol: MIP355

## ■ Absolute Maximum Ratings $T_a = 25^{\circ}\text{C} \pm 3^{\circ}\text{C}$

Parameter	Symbol	Rating	Unit
DRAIN voltage	VD	-0.3 to +700	V
VDD voltage	VDD	-0.3 to +8	V
FB pin voltage	VFB	-0.3 to +6	V
FB pin current	IFB	500	$\mu\text{A}$
f pin voltage	Vf	-0.3 to +8	V
CL pin voltage	VCL	-0.3 to +8	V
Output peak current *	IDP	3	A
Channel temperature	Tch	150	$^{\circ}\text{C}$
Storage temperature	Tstg	-55 to +150	$^{\circ}\text{C}$

Note) \*: The guarantee within the following pulse width.  
Leading edge blanking delay + Current limit delay

## ■ Block Diagram



**■ Electrical Characteristics**  $T_C = 25^{\circ}\text{C} \pm 3^{\circ}\text{C}$ 

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>Control functions</b>						
Output frequency *2	fosc	VD = 5 V, VDD = VDD(ON) + 0.1 V, IFB = 30 $\mu\text{A}$ , Vf = VDD, VCL = 0 V, after dis_OLP	39	43.5	48	kHz
Jitter frequency deviation *2	$\Delta f$	VD = 5 V, VDD = VDD(ON) + 0.1 V, IFB = 30 $\mu\text{A}$ , Vf = VDD, VCL = 0 V, after dis_OLP	1.2	3	4.8	kHz
Jitter frequency modulation rate *1,2	fM	VD = 5 V, VDD = VDD(ON) + 0.1 V, IFB = 30 $\mu\text{A}$ , Vf = VDD, VCL = 0 V, after dis_OLP		150		Hz
Maximum duty cycle	MAXDC	VD = 5 V, VDD = VDD(ON) + 0.1 V, IFB = 30 $\mu\text{A}$ , Vf = VDD, VCL = 0 V, after dis_OLP	65	70	75	%
VDD start voltage	VDD(ON)	VD = 5 V, IFB = 30 $\mu\text{A}$ , Vf = VDD, VCL = 0 V	5.4	5.9	6.4	V
VDD stop voltage	VDD(OFF)	VD = 5 V, IFB = 30 $\mu\text{A}$ , Vf = VDD, VCL = 0 V	4.4	4.9	5.4	V
VDD start / stop hysteresis	VDD(HYS)	VDD(ON) – VDD(OFF)	0.5	1.0	1.5	V
VDD clamp voltage	VDD(CLP)	IDD = 10 mA	6.9	7.4	8.9	V
FB threshold current	IFB1	ON $\rightarrow$ OFF, VD = 5 V, VDD = VDD(ON) + 0.1 V, Vf = VDD, VCL = 0 V	57	97	137	$\mu\text{A}$
FB hysteresis current	IFB(HYS)	VD = 5 V, VDD = VDD(ON) + 0.1 V, Vf = VDD, VCL = 0 V		2.5		$\mu\text{A}$
FB pin voltage	VFB1	VD = 5 V, VDD = VDD(ON) + 0.1 V, IFB = IFB1, Vf = VDD, VCL = 0 V	1.6	1.9	2.2	V
	VFB	VD = 5 V, VDD = VDD(ON) + 0.1 V, IFB = 80 $\mu\text{A}$ , Vf = VDD, VCL = 0 V	1.5	1.8	2.1	V
Supply current before start-up	IDD(SB)	VD = 5 V, VDD = VDD(ON) – 0.2 V, Vf = VDD, VCL = 0 V, FB: OPEN	170	350	530	$\mu\text{A}$
Supply current	IDD	VD = 5 V, VDD = VDD(ON) + 0.1 V, IFB = 30 $\mu\text{A}$ , Vf = VDD, VCL = 0 V	250	510	750	$\mu\text{A}$
Supply current at light load	IDD(OFF)	VD = 5 V, VDD = VDD(ON) + 0.1 V, IFB = IFB1 + 5 $\mu\text{A}$ , Vf = VDD, VCL = 0 V	300	550	800	$\mu\text{A}$
VDD charging current	Ich1	VDD = 0 V, VD = 40 V, FB, CL, f: OPEN	–13.6	–8.5	–4.1	mA
	Ich2	VDD = 5 V, VD = 40 V, FB, CL, f: OPEN	–8.5	–5.3	–2.1	mA
f pin threshold voltage	Vf1	VDD = VDD(ON) + 0.1 V, fosc: foscL $\rightarrow$ foscH	0.65	1.25	1.85	V
f pin current before start-up	If1	VDD = VDD(ON) – 0.1 V, Vf = 0 V	–70	–50	–30	$\mu\text{A}$
f pin threshold current	If2	VDD = VDD(ON) + 0.1 V, fosc: foscL $\rightarrow$ foscH	–44	–29	–14	$\mu\text{A}$
f pin voltage foscH change	Vf2	VDD = VDD(ON) + 0.1 V, If = If2	2	2.3	2.6	V
f pin short current	If_GND	VDD = VDD(ON) + 0.1 V, Vf = 0 V	–37	–22	–7	$\mu\text{A}$
f pin voltage	Vf	VDD = VDD(ON) + 0.1 V, If = –50 $\mu\text{A}$	1.55	2.25	2.85	V

■ Electrical Characteristics (continued)  $T_C = 25^\circ\text{C} \pm 3^\circ\text{C}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
CL pin threshold voltage	VCL1	VDD = VDD(ON) + 0.1 V, ILIMIT: ILIMIT → ILIMIT_M	0.75	1.35	1.95	V
CL pin current before start-up	ICL1	VDD = VDD(ON) - 0.4 V, VCL = 0 V	-70	-50	-30	μA
CL pin threshold current	ICL2	VDD = VDD(ON) + 0.1 V, ILIMIT: ILIMIT_L → ILIMIT_M	-44	-29	-14	μA
CL pin voltage for ILIMIT_M change	VCL2	VDD = VDD(ON) + 0.1 V, ICL = ICL2	1.75	2.35	2.95	V
CL pin short current	ICL_GND	VDD = VDD(ON) + 0.1 V, VCL = 0 V	-37	-22	-7	μA
CL pin voltage	VCL	VDD = VDD(ON) + 0.1 V, ICL = -50 μA	1.6	2.3	2.9	V
Output frequency High *2	foscH	VD = 5 V, VDD = VDD(ON) + 0.1 V, IFB = 30 μA, If = -50 μA, VCL = 0 V, after dis_OLP	57.5	64	70.5	kHz
Jitter frequency deviation at foscH *2	ΔfH	VD = 5 V, VDD = VDD(ON) + 0.1 V, IFB = 30 μA, If = -50 μA, VCL = 0 V, after dis_OLP	1.6	4	6.4	kHz
Jitter frequency modulation rate at foscH *1, 2	fMH	VD = 5 V, VDD = VDD(ON) + 0.1 V, IFB = 30 μA, If = -50 μA, VCL = 0 V, after dis_OLP		250		Hz
Output frequency Low *2	foscL	VD = 5 V, VDD = VDD(ON) + 0.1 V, IFB = 30 μA, Vf = 0 V, VCL = 0 V, after dis_OLP	22	24	26	kHz
Jitter frequency deviation at foscL *2	ΔfL	VD = 5 V, VDD = VDD(ON) + 0.1 V, IFB = 30 μA, Vf = 0 V, VCL = 0 V, after dis_OLP	0.6	1.5	2.4	kHz
Jitter frequency modulation rate at foscL *1, 2	fML	VD = 5 V, VDD = VDD(ON) + 0.1 V, IFB = 30 μA, Vf = 0 V, VCL = 0 V, after dis_OLP		100		Hz

Circuit protections

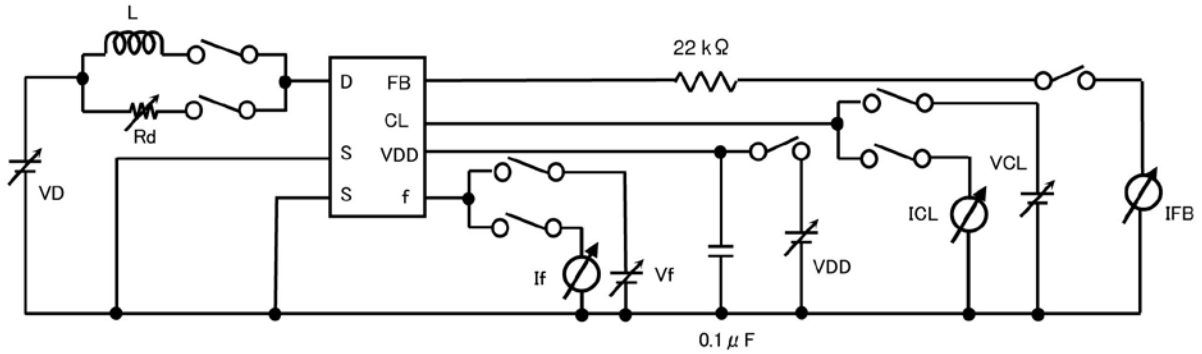
Self protection current limit *6	ILIMIT	VDD = VDD(ON) + 0.1 V, Vf = VDD, VCL = 0 V, FB: OPEN, Duty = 30%	0.92	1	1.08	A
Drain current at light load *1, 3	ID(OFF)	VDD = VDD(ON) + 0.1 V, IFB = IFB1 - IFBHYS, Vf = VDD, VCL = 0 V, Duty = 30%	80	200	320	mA
OLP detection blanking time *1	dis_OLP	VD = 30 V, Vf = VDD, VCL = 0 V, VDD, VB: OPEN	8	16	25	ms
Self protection current ILIMIT_M *3	ILIMIT_M	VDD = VDD(ON) + 0.1 V, Vf = VDD, ICL = -50 μA, FB: OPEN, Duty = 30%	0.724	0.8	0.876	A
Drain current at light load of ILIMIT_M *1, 3	ID(OFF)_M	VDD = VDD(ON) + 0.1 V, IFB = IFB1 - IFBHYS, Vf = VDD, ICL = -50 μA, Duty = 30%	28	73	118	mA
Self protection current ILIMIT_L *3	ILIMIT_L	VDD = VDD(ON) + 0.1 V, Vf = VDD, VCL = VDD, FB: OPEN, Duty = 30%	0.263	0.29	0.318	A
Drain current at light load of ILIMIT_L *1, 3	ID(OFF)_L	VDD = VDD(ON) + 0.1 V, IFB = IFB1 - IFBHYS, Vf = VDD, VCL = VDD, Duty = 30%	20	50	80	mA
VDD current at latch stop	IDD(OV)	VD = 5 V, IFB = 30 μA, VCL = 0 V, Vf = 0 V	22	32	42	mA

**■ Electrical Characteristics (continued)  $T_C = 25^\circ\text{C} \pm 3^\circ\text{C}$** 

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
FB current at detecting OLP	IFB(OLP)	VD = 20 V, VCL = 0 V, Vf = VDD, VDD: OPEN	6	11.5	17	$\mu\text{A}$
Timer intermittent function *4	TIMER	VDD(ON) $\leftrightarrow$ VDD(OFF), VD = 45 V, IFB < IFB(OLP)		8		—
Timer intermittent function disabled at MAXDC *5	TIMER2	VDD(ON) $\leftrightarrow$ VDD(OFF), IFB < IFB(OLP) Duty = MAXDC		1		—
Power-up reset threshold voltage	VDDreset		1.8	2.6	3.5	V
Over temperature protection *1	OTP		130	140	150	$^\circ\text{C}$
Over temperature protection hysteresis *1	$\Delta\text{OTP}$			70		$^\circ\text{C}$
<b>Output</b>						
Leading edge blanking delay *1	ton(BLK)	VDD = VDD(ON) + 0.1 V, IFB = 30 $\mu\text{A}$ , Vf = VDD, VCL = 0 V	240	300	360	ns
Current limit delay *1	td(OCL)		20	70	120	ns
ON state resistance	RDS(ON)	IDS = 100 mA		4.6	5.8	$\Omega$
Breakdown voltage	VDSS	VDD: VDD(ON) + 0.1 V $\rightarrow$ VDD(OFF) – 0.1 V $\rightarrow$ VDD(ON) + 0.1 V, ID = 100 $\mu\text{A}$ , VFB = 0 V	700			V
Off state current	IDSS	VDD: VDD(ON) + 0.1 V $\rightarrow$ VDD(OFF) – 0.1 V $\rightarrow$ VDD(ON) + 0.1 V, VDS = 650 V, VFB = 0 V		10	20	$\mu\text{A}$
Rise time *7	tr	VD = 5 V, VDD = VDD(ON) + 0.1 V, IFB = 30 $\mu\text{A}$ , Vf = VDD, VCL = 0 V		110		ns
Fall time *7	tf	VD = 5 V, VDD = VDD(ON) + 0.1 V, IFB = 30 $\mu\text{A}$ , Vf = VDD, VCL = 0 V		40		ns
<b>Supply voltage characteristics</b>						
Drain supply voltage	VD(MIN)	IFB = 30 $\mu\text{A}$ , Vf = VDD, VCL = 0 V, VDD: OPEN		10	35	V
<b>Control functions during VDD = VDD(CLP)</b>						
Output frequency at CLAMP *2	fossC	VD = 5 V, VDD = VDD(CLP) – 0.1 V, IFB = 30 $\mu\text{A}$ , Vf = VDD, VCL = 0 V	40	46	52	kHz
Jitter frequency deviation at CLAMP *2	$\Delta\text{fC}$	VD = 5 V, VDD = VDD(CLP) – 0.1 V, IFB = 30 $\mu\text{A}$ , Vf = VDD, VCL = 0 V	1.92	4.8	7.68	kHz
Jitter frequency modulation rate at CLAMP *1, 2	fMC	VD = 5 V, VDD = VDD(CLP) – 0.1 V, IFB = 30 $\mu\text{A}$ , Vf = VDD, VCL = 0 V		100		Hz
<b>Circuit protections during VDD = VDD(CLP)</b>						
Self protection current limit at CLAMP	ILIMIT_C	VDD = VDD(CLP) – 0.1 V, Vf = VDD, VCL = 0 V, FB: OPEN, Duty = 30%	0.95	1.06	1.17	A
<b>Output during VDD = VDD(CLP)</b>						
Leading edge blanking delay at CLAMP *1	ton(BLK)_C	VDD = VDD(CLP) – 0.1 V, IFB = 30 $\mu\text{A}$ , Vf = VDD, VCL = 0 V	290	360	430	ns

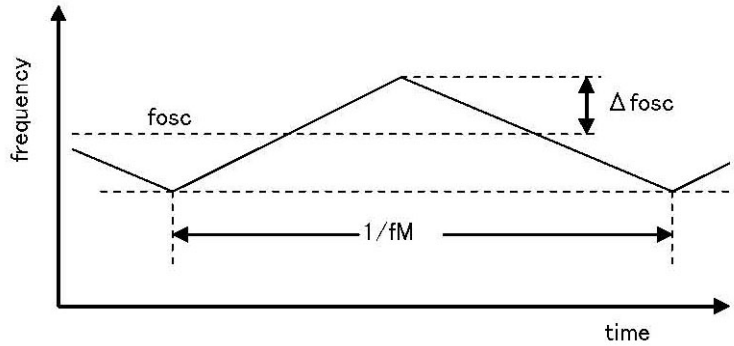
■ Electrical Characteristics (continued)  $T_C = 25^\circ\text{C} \pm 3^\circ\text{C}$

1. Measurement circuit

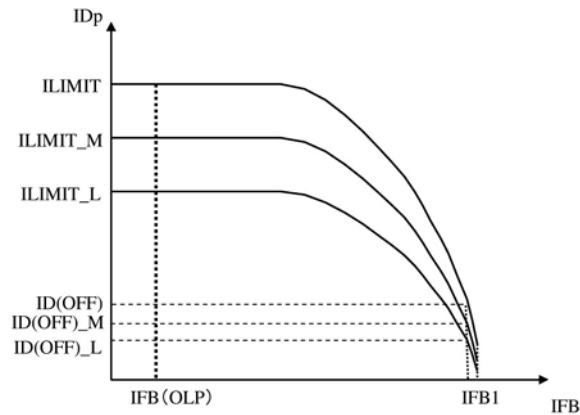


2. \*1 : Design guarantee item

\*2 :  $f_{osc}$ ,  $\Delta f$ ,  $f_M$  measurement

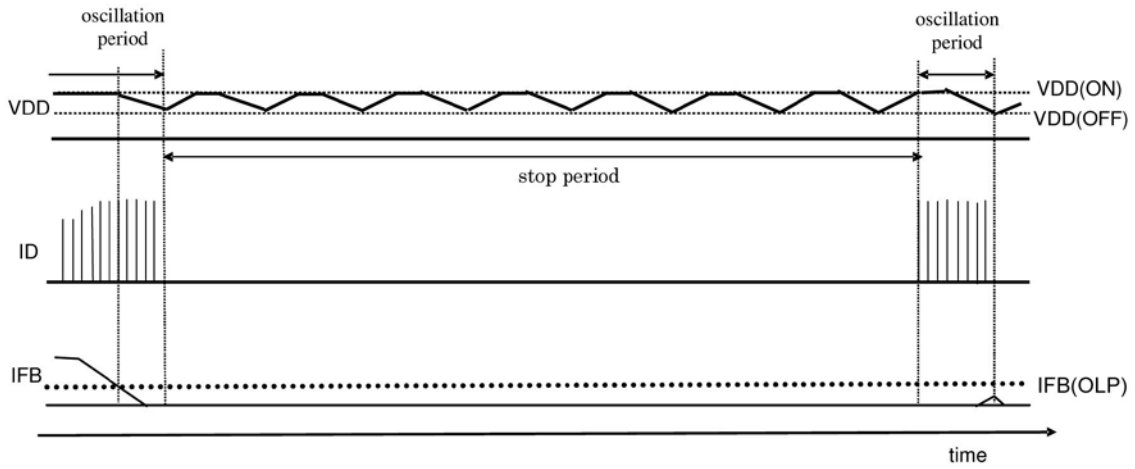


\*3 : FB current IFB vs drain peak current IDP characteristic

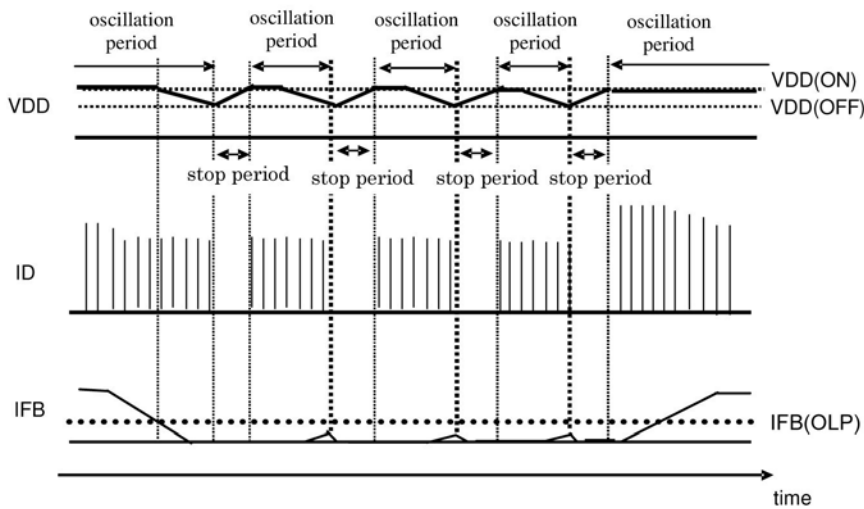


■ Electrical Characteristics (continued)  $T_C = 25^{\circ}\text{C} \pm 3^{\circ}\text{C}$

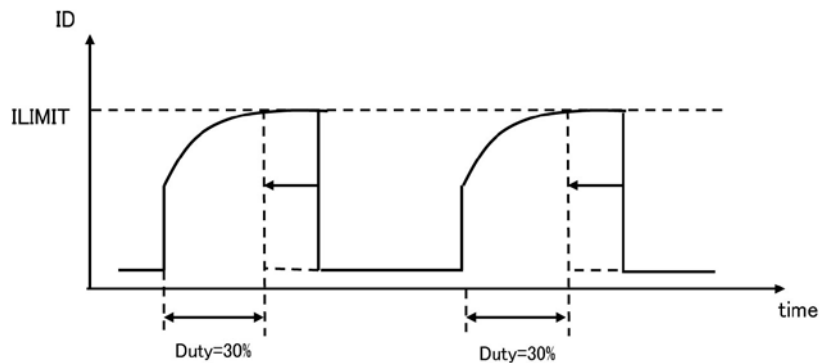
2. \*4 : Terminal waveforms during timer intermittent operation due to the overload protection



\*5 : Terminal waveforms when MAXDC is detected which makes timer intermittent operation becomes invalid. Though FB current is below IFB(OLP) which indicates the detection of overload state, if the ON duty of the drain current is operating at MAXDC, drain oscillation will occur in every rise and fall cycle of the VDD terminal.



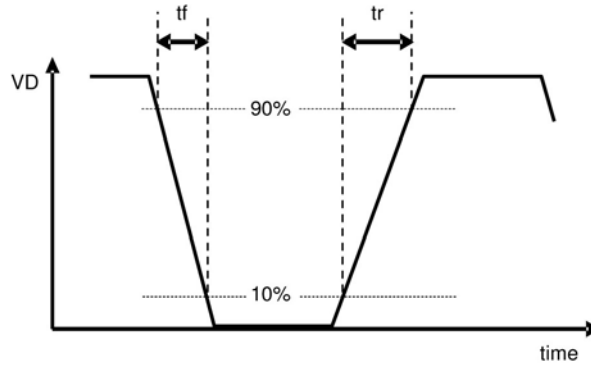
\*6 : ILIMIT measurement



\* Load L, R during the ILIMIT measurement are:  $L=100\mu\text{H}$ ,  $R_d=130\Omega$

■ Electrical Characteristics (continued)  $T_C = 25^\circ\text{C} \pm 3^\circ\text{C}$

2. \*7 : tr, tf measurement



3. fosc, ILIMIT setting method through f, CL terminals

Depending upon selection at f terminal and CL terminal according to description below 1) to 3), would output frequency (fosc) or over-current protection detection (ILIMIT) based on the setting in the below-mentioned table.

- 1) Connection to S terminal
  - 2) Resistor (47 kΩ) connected between S terminal \*
  - 3) Connection to VDD terminal
- \*: 2) please use resistor of 47 kΩ (tolerance: within ±5%)

	f	f <sub>psc</sub> (kHz)
1)	S	foscL
2)	resistor (47 kΩ)	foscH
3)	VDD	fosc

	CL	ILIMIT (A)
1)	S	ILIMIT
2)	resistor (47 kΩ)	ILIMIT_M
3)	VDD	ILIMIT_L

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- (6) Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.
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Note) The products of MIP50\*\*, MIP51\*\*, and MIP7\*\* are excluded from above-mentioned precautions, 1) to 3).

Attached table "IPD availability by customer"

Parts No.			Companies/areas to which products can be sold	Companies/areas to which products cannot be sold	Application
MIP01** MIP2** MIP9A**	MIP02** MIP3** MIP9L**	MIP1** MIP4**	<ul style="list-style-type: none"> <li>· Japanese companies in Japan</li> <li>· Japanese companies in Asia (50% or more owned)</li> </ul>	<ul style="list-style-type: none"> <li>· Companies in European and American countries</li> <li>· Asian companies in Asia</li> <li>· Other local companies</li> </ul>	<ul style="list-style-type: none"> <li>· For power supply</li> <li>· For DC-DC converter</li> </ul>
MIP00** MIP55** MIP816/826	MIP52** MIP56** MIP9E**	MIP53** MIP803/804	<ul style="list-style-type: none"> <li>· Japanese companies in Japan</li> <li>· Japanese companies in Asia (50% or more owned)</li> <li>· Asian companies in Asia</li> </ul>	<ul style="list-style-type: none"> <li>· Companies in European and American countries</li> <li>· Other local companies</li> </ul>	<ul style="list-style-type: none"> <li>· For power supply</li> <li>· For EL driver</li> <li>· For LED lighting driver</li> </ul>
MIP50**	MIP51**	MIP7**	<ul style="list-style-type: none"> <li>· No restrictions in terms of contract</li> </ul>	<ul style="list-style-type: none"> <li>· No restrictions in terms of contract</li> </ul>	<ul style="list-style-type: none"> <li>· For lamp driver/ car electronics accessories</li> </ul>

Note) For details, contact our sales division.