PLESSEY
Semiconductors

# 2 MBIT PCM SIGNALLING CIRCUIT
# MJ 1440
## HDB3 ENCODER/DECODER

The 2.048 MBit PCM Signalling Circuits comprise a group of circuits which will perform the common signalling and error detection functions for a 2.048 MBit PCM transmission link operating to the appropriate CCITT recommendations. The circuits are fabricated in N-channel metal gate MOS and operate from a single 5 volt supply, relevant inputs and outputs are TTL compatible.

The MJ1440 is an encoder/decoder for the pseudo-ternary transmission code, HDB3 (CCITT Orange Book Vol III.2 Annex to Rec. G703). The device encodes and decodes simultaneously and asynchronously. Error monitoring functions are provided to detect violations of HDB3 coding, all ones detection and loss of input (all zeroes detection). In addition a loop back function is provided for terminal testing.

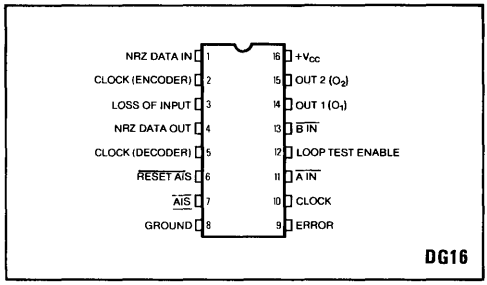


*Fig. 1 Pin connections*

### FEATURES

- 5v ± 5% Supply −50mA Max
- HDB3 Encoding and Decoding to CCITT rec. G703.
- Asynchronous Operation.
- Simultaneous Encoding and Decoding.
- Clock Recovery Signal Generated from Incoming HDB3 Data.
- Loop Back Control.
- HDB3 Error Monitor
- 'All Ones' Error Monitor
- Loss of Input Alarm (All Zeros Detector).
- Decode Data in NRZ Form.

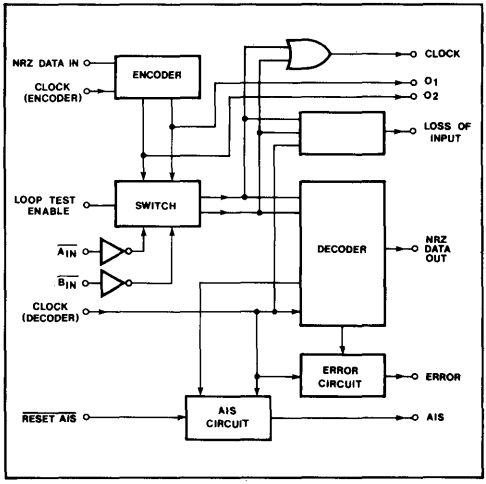


*Fig. 2 Block diagram*

### ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

**Electrical Ratings**

| | |
|---|---|
| +Vcc | 7V |
| Inputs | Vcc + 0.5V Gnd − 0.3V |
| Outputs | Vcc, Gnd −0.3V |

**Thermal Ratings**

Max Junction Temperature 175°C

| | |
|---|---|
| Thermal Resistance: Chip to Case | Chip to Amb. |
| 40°C/Watt | 120°C/Watt |

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
Supply voltage, $V_{CC} = 5V \pm 0.25V$
Ambient temperature, $T_{amb} = 0°C$ to $+70°C$

**Static characteristics**

| Characteristic | Symbol | Pins | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Low level input voltage | $V_{IL}$ | 1,2,5,6 10,11,12,13 | -0.3 | | 0.8 | V | |
| Low level input current | $I_{IL}$ | | | | 50 | µA | $V_{IL} = 0V$ |
| High level input voltage | $V_{IH}$ | | 2.5 | | $V_{cc}$ | V | |
| High level input current | $I_{IH}$ | | | | 50 | µA | $V_{IH} = 5V$ |
| Low level output voltage | $V_{OL}$ | 10,14,15 | | | 0.5 | V | Isink = 80µA |
| | | 3,4,7,9 | | | 0.4 | V | Isink = 1.6mA |
| High level output voltage | $V_{OH}$ | 3,4,7,9 | 2.7 | | | V | Isource = 60µA |
| | | 14,15 | 2.8 | | | V | Isource = 2mA |
| | | 10 | 2.8 | | | V | Isource = 1mA |
| Supply current | $I_{cc}$ | | | 20 | 50 | mA | All inputs to 0V<br>All outputs open circuit |

**Dynamic Characteristics**

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Max. Clock (Encoder) frequency | $fmax_{enc}$ | 4.0 | | | MHz | Figs.10, 15 |
| Max. Clock (Decoder) frequency | $fmax_{dec}$ | 2.2 | | | MHz | Figs.11, 15 |
| Propagation delay Clock (Encoder) to $O_1$, $O_2$ | tpd1A/B | | | 100 | ns | Figs.10, 15. See Note 1 |
| Rise and Fall times $O_1$, $O_2$ | | | | 20 | ns | Figs.10, 15 |
| tpd1A-tpd1B | | | | 20 | ns | Figs.10, 15 |
| Propagation delay Clock (Encoder) to Clock | tpd3 | | | 150 | ns | Loop test enable = Figs.13, 15 |
| Setup time of NRZ data in to Clock (Encoder) | ts3 | 30 | | | ns | Figs.8, 10, 15 |
| Hold time of NRZ data in | th3 | 55 | | | ns | Figs.10, 15 |
| Propagation delay $A_{in}$, $B_{in}$ to Clock | tpd2 | | | 150 | ns | Loop test enable = '0' Figs.9, 13, 15 |
| Propagation delay Clock (Decoder) to loss of input | | | | 150 | ns | |
| Propagation delay Clock (Decoder) to error | tpd4 | | | 200 | ns | Figs.12, 15 |
| Propagation delay $\overline{\text{Reset AIS}}$ to AIS | tpd5 | | | 200 | ns | Loop test enable = '0' Figs.14, 15 |
| Propagation delay Clock (Decoder) to NRZ data out | tpd6 | | | 150 | ns | Figs.9, 11, 15. See Note 2 |
| Setup time of $A_{in}$, $B_{in}$ to Clock (Decoder) | ts1 | 75 | | | ns | Figs.9, 11, 15 |
| Hold time of $A_{in}$, $B_{in}$ to Clock (Decoder) | th1 | 5 | | | ns | Figs.9, 11, 15 |
| Hold time of $\overline{\text{Reset AIS}}$ = '0' | th2 | 100 | | | ns | Figs.9, 14, 15 |
| Setup time Clock (Decoder) to $\overline{\text{Reset AIS}}$ | ts2 | 200 | | | ns | Figs.9, 14, 15 |
| Setup time $\overline{\text{Reset AIS}}$ = 1 to Clock (Decoder) | ts2 | 0 | | | ns | Figs.14, 15 |

NOTES
1. Encoded HDB3 outputs ($O_1$, $O_2$) are delayed by 3½ clock periods from NRZ data in (Fig.3).
2. The decoded NRZ output is delayed by 3 clock periods from the HDB3 inputs ($A_{IN}$, $B_{IN}$) (Fig.4).

## FUNCTIONAL DESCRIPTION

### Functions Listed by pin number

**1. NRZ Data in**
Input data for encoding into ternary HDB3 form. The NRZ data is clocked by the negative edge of the Clock (Encoder).

**2. Clock (Encoder)**
Clock for encoding data on pin 1

**3. Loss of input alarm**
This output goes to logic '1' if eleven consecutive zeroes are detected in the incoming HDB3 data. The output is set to logic '0' on receipt of a '1'.

**4. NRZ data out**
Decoded data in NRZ form from ternary HDB3 input data ($A_{in}$,$B_{in}$), data is clocked out by positive going edge of clock (Decoder).

**5. Clock (Decoder)**
Clock for decoding ternary data $A_{in}$, $B_{in}$.

**6, 7. Reset AIS, AIS**
Logic '0' on $\overline{\text{Reset AIS}}$ resets a decoded zero counter and either resets AIS outputs to zero provided 3 or more zeroes have been decoded in the preceding $\overline{\text{Reset AIS}}$ = 1 period or sets AIS to '1' if less than 3 zeroes have been decoded in the preceding two $\overline{\text{Reset AIS}}$ = 1 periods.
Logic '1' on Reset AIS enables the internal decoded zero counter.

**8. Ground**
Zero volts

**9. Error**
A logic '1' indicates that a violation of the HDB3 coding has been received i.e. 3 '1's of the same polarity.

**10. Clock**
'OR' function of $\overline{A_{in}}$,$\overline{B_{in}}$ for clock regeneration when pin 12 = '0'. 'OR' function of $O_1$,$O_2$ when pin 12 = '1'.

**11,13. $\overline{A}_{in}$,$\overline{B}_{in}$**
Inputs representing the received ternary HDB3 PCM signal. $\overline{A_{in}}$ = '0' represents a positive going '1', $\overline{B_{in}}$ = '0' represents a negative going '1'. $\overline{A_{in}}$ and $\overline{B_{in}}$ are sampled by the positive going edge of the Clock (Decoder). $\overline{A_{in}}$ and $\overline{B_{in}}$ may be interchanged.

**12. Loop test enable**
Input to select normal or loop back operation. Pin 12 = '0' selects normal operation, encode and decode are independent and asynchronous. When pin 12 = '1' $O_1$ is connected internally to $A_{in}$. $O_2$ is connected internally to $B_{in}$. Clock becomes the OR function $O_1 + O_2$. The delay from NRZ in to NRZ out is 6½ clock periods in the loop back condition.

**14, 15. $O_1$, $O_2$**
Outputs representing the ternary encoded data for line transmission $O_1$ = '1' representing a positive going '1', $O_2$ = '1' represents a negative going '1'. $O_1$ and $O_2$ may be interchanged.

**16. $V_{cc}$**
Positive supply, 5V ± 5%

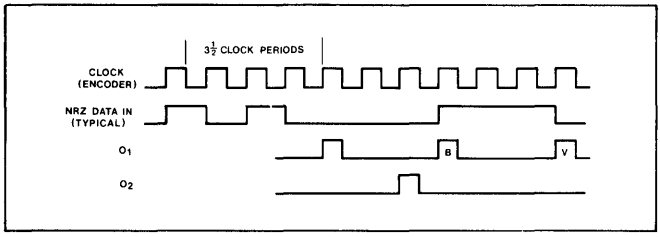


*Fig. 3 Encode waveforms*

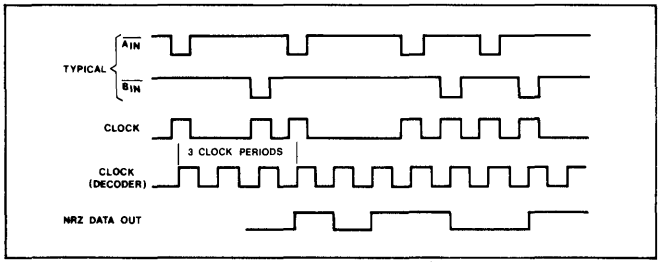


*Fig. 4 Decode waveforms*

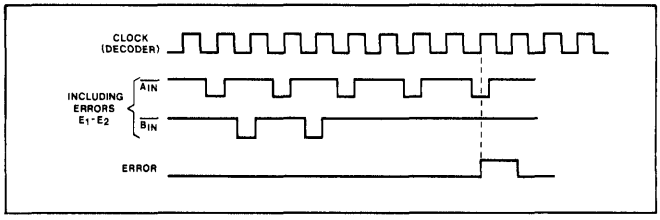


*Fig. 5 HDB3 error output waveforms*

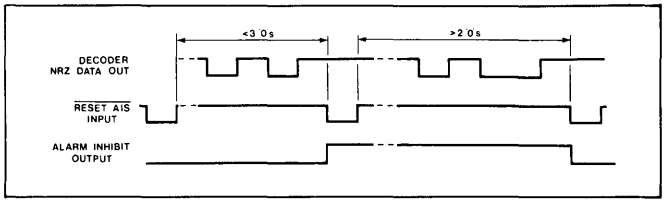


*Fig. 6 AIS error and reset waveforms*

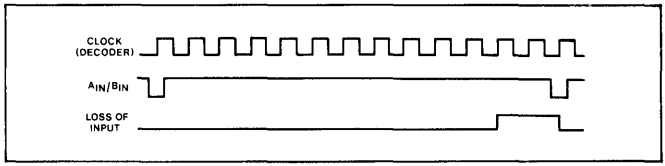


*Fig. 7 Loss of input waveforms*

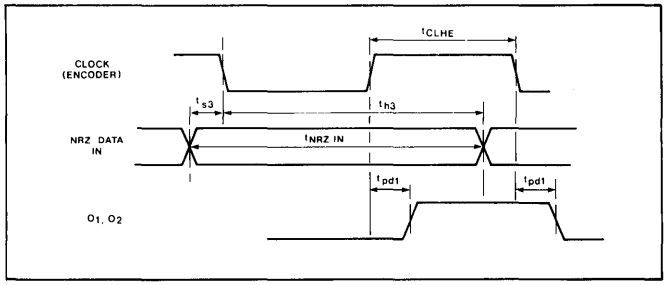


*Fig. 8 Encoder timing relationship*

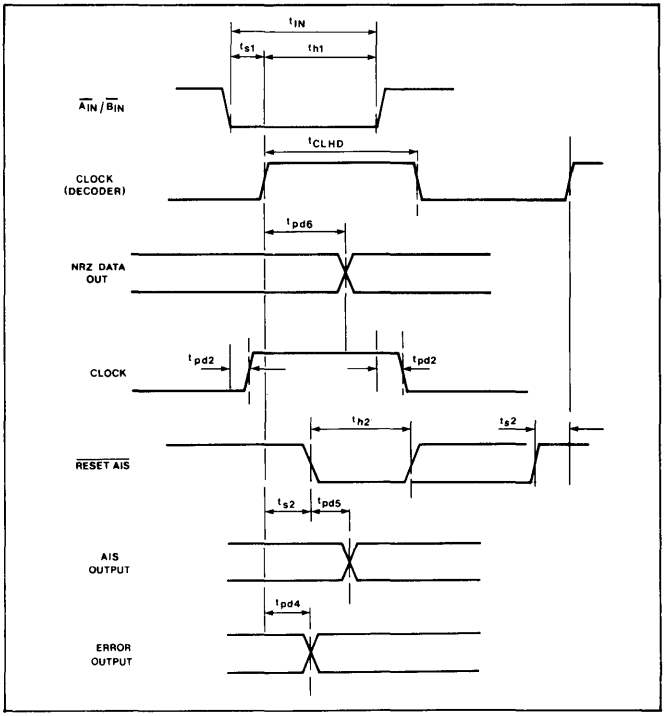


*Fig. 9 Decoder timing relationship*

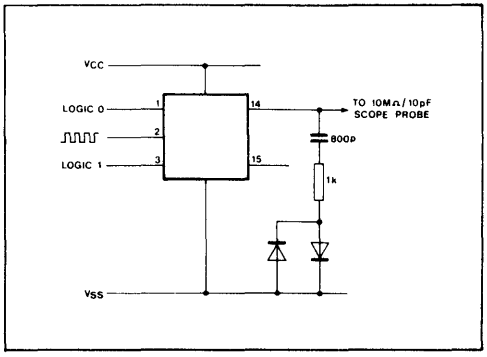


Fig. 10

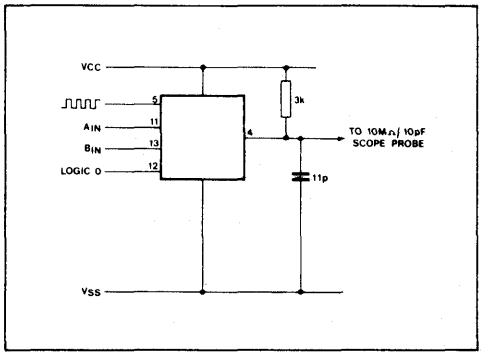


Fig. 11

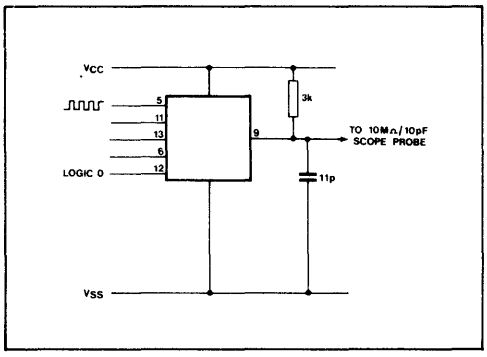


Fig. 12

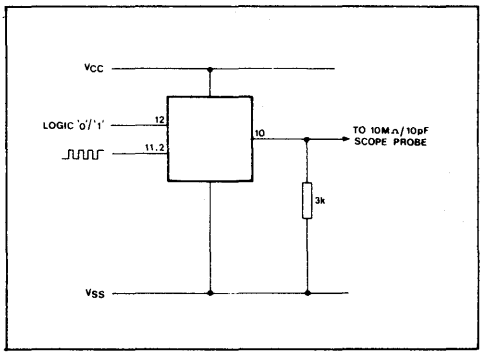


Fig. 13

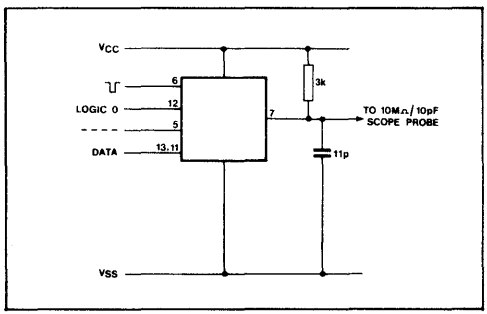


Fig. 14

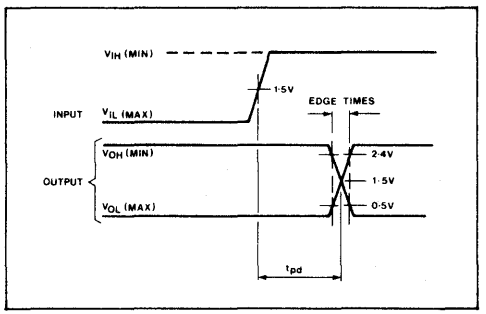


Fig. 15 *Test timing definitions*

## DEFINITION OF THE HDB3 CODE

Coding of a binary signal into an HDB3 signal is done according to the following rules:

**1.** The HDB3 signal is psuedo-ternary; the three states are denoted $B_+$, $B_-$ and O.

**2.** Spaces in the binary signal are coded as spaces in the HDB3 signal. For strings of four spaces however, special rules apply (see 4. below).

**3.** Marks in the binary signal are coded alternately as $B_+$ and $B_-$ in the HDB3 signal (alternate mark inversion). Violations of the rule of alternate mark inversion are introduced when coding strings of four spaces (see 4. below).

**4.** Strings of four spaces in the binary signal are coded according to the following rules:

**a** The first space of a string is coded as a space if the preceding mark of the HDB3 signal has a polarity opposite to the polarity of the preceding violation and is not a violation by itself; it is coded as a mark, i.e. not a violation (i.e. $B_+$, $B_-$), if the preceding mark of the HDB3 signal has the same polarity as that of the preceding violation or is by itself a violation.
This rule ensures that successive violations are of alternative polarity so that no DC component is introduced.

**b** The second and third spaces of a string are always coded as spaces.

**c** The last space of a string of four is always coded as a mark, the polarity of which is such that it violates the rule of alternate mark inversion. Such violations are denoted $V_+$ or $V_-$ according to their polarity.