PLESSEY
Semiconductors

2 MBIT PCM SIGNALLING CIRCUIT

MJ 1444

PCM SYNCHRONISING WORD GENERATOR

The 2.048 Mbit PCM signalling circuits comprise a group of circuits which will perform the common signalling and error detection functions for a 2.048 Mbit 30 channel PCM transmission link operating to the appropriate CCITT recommendations. The circuits are fabricated in N-channel metal gate MOS and operate from a single 5 volt supply. Relevant inputs and outputs are TTL compatible.

The MJ1444 generates the synchronising word in accordance with CCITT recommendations G732. The MJ1445 has been designed to detect this synchronising word when received at the remote end of the transmission system.

The synchronising word is injected onto the PCM data highway during time slot 0 in alternate frames. The spare time slot 0 data bits, bit 1 in every frame and bits 3 to 8 inclusive in alternate frames (i.e. those not containing the synchronising word) are available as parallel inputs and are output onto the PCM data highway.

The data output of the MJ1444 is 'open collector' and can be wire-OR'd directly onto the highway.

The device also provides a time slot 0 channel pulse 'TS0', time slot 0 non-sync. frame 'TS0 $\overline{SF}$', and time slot 16 'TS16' outputs.

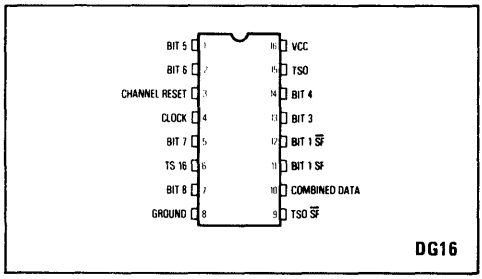

Fig.1 Pin connections

FEATURES

- 5V ± 5% Supply — 20mA Typical
- Fully Conforms to CCITT Recommendation G732
- Outputs Directly Onto PCM Data Highway
- Provides Both Time Slot 0 and Time Slot 16 Channel Pulses
- All Inputs and Outputs are TTL Compatible

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Electrical Ratings

+Vcc	7V
Inputs	Vcc + 0.5V Gnd − 0.3V
Outputs	Vcc, Gnd −0.3V

Thermal Ratings

Max Junction Temperature 175°C

Thermal Resistance: Chip to Case	Chip to Amb.
35°C/Watt	120°C/Watt

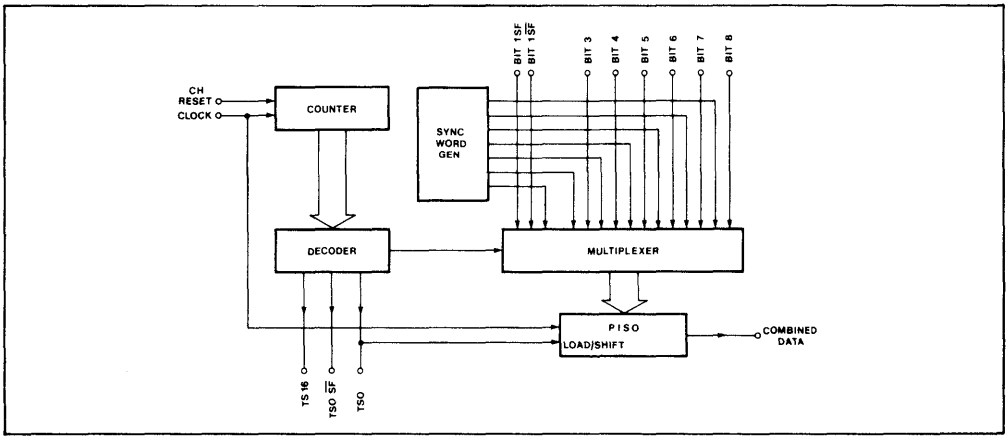

Fig.2 MJ1444 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage, $V_{CC} = 5V \pm 0.25V$
Ambient operating temperature -10°C to +70°C

Static Characteristics

Characteristic	Symbol	Pins	Value			Units	Conditions
			Min.	Typ.	Max.		
Low level input voltage	V_{IL}	1, 2, 3, 4, 5, 7, 11, 12, 13, 14.	-0.3		0.8	V	
Low level input current High level input current	I_{IN}	11		1	50	μA	
High level input voltage	V_{IH}	11	2.4		V_{CC}		
Low level output voltage	V_{OL}	6, 9, 15			0.5	V	$I_{sink} = 2mA$
		10			0.7	V	$I_{sink} = 5mA$
High level output voltage	V_{OH}	6, 9, 15	2.8			V	$I_{source} = 200\mu A$
High level output leakage current	I_{OH}	10			20	μA	$V_{OUT} = V_{CC}$
Supply current	I_{CC}			20	40	mA	$V_{CC} = 5.25V$

Dynamic Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Max clock frequency	F_{max}	3			MHz	
Propagation delay, clock to TS0, TS0 $\overline{SF}$, TS16 and combined data outputs.	t_p	80		200	ns	See Figs.5 and 6
Set up time channel reset to clock	T_{S1}	100		450	ns	$f_{clock} = 2.048MHz$
Hold time of channel reset input	t_{H1}	20		400	ns	
Set up time of bit 1 (SF) to datum B	t_{S2}	100			ns	
Hold time of bit 1 (SF) wrt datum B	t_{H2}	300			ns	
Set up time of bit 1 ($\overline{SF}$) and data bits 3—8 to datum B	t_{S2}	100			ns	
Hold time of bit 1 ($\overline{SF}$) and data bits 3—8 wrt datum B	t_{H2}	300			ns	

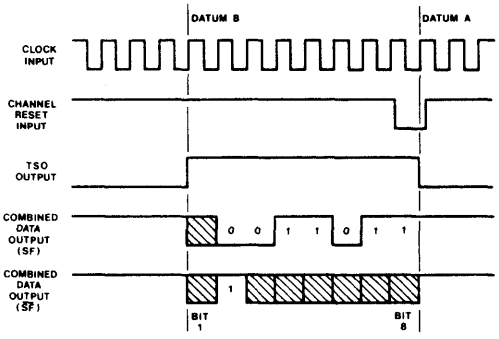

Fig.3 Data timing

FUNCTIONAL DESCRIPTION

Functions Listed by pin number

1, 2, 5, 7, 13, 14. Bits 3 to 8
Parallel data on these inputs is asynchronously loaded into bits 3 to 8 of the PISO shift register for transmission during Time slot 0 of non-sync. frames.

3. Channel Reset
A low going pulse at this input synchronises the MJ1444 with the other devices at the transmit end of the PCM link. It may be applied as a start pulse or repeated at the same instant in successive frames.

4. Clock
System clock input (2.048MHz for a 2 Mbit PCM system).

6. TS16
This output provides a positive pulse equivalent to 8 clock periods during time slot 16 of every 30 + 2 channel PCM frame.

8. GND
Zero volts.

9. TS0 $\overline{SF}$
This output provides a positive pulse equivalent to 8 clock periods during time slot 0 of non-sync. frames.

10. Combined data
This 'open collector' output injects the contents of the PISO shift register onto the PCM data highway during time slot 0 in successive frames. The contents of the PISO shift register are defined as follows:

	Bit 1	2	3	4	5	6	7	8
Sync. Frame	X	0	0	1	1	0	1	1
Non-sync. frame	X	1	X	X	X	X	X	X

X — indicates that these bits may be set according to the parallel data inputs.

11. Bit 1 SF
Data on this input is asynchronously loaded into bit 1 of the PISO shift register for transmission during time slot 0 of sync. frames.

12. Bit 1 $\overline{SF}$
Data on this input is asynchronously loaded into bit 1 of the PISO shift register for transmission during time slot 0 of non-sync. frames.

15. TS0
This output provides a positive pulse equivalent to 8 clock period during time slot 0 of every 30 channel PCM frame.

16. V_{CC}
Positive supply, 5V ±5%.

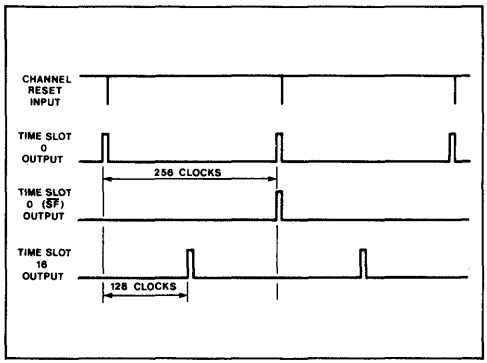

Fig.4 Sync. timing

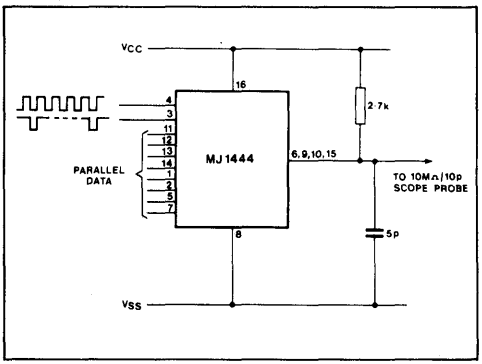

Fig.5 Test conditions (all outputs)

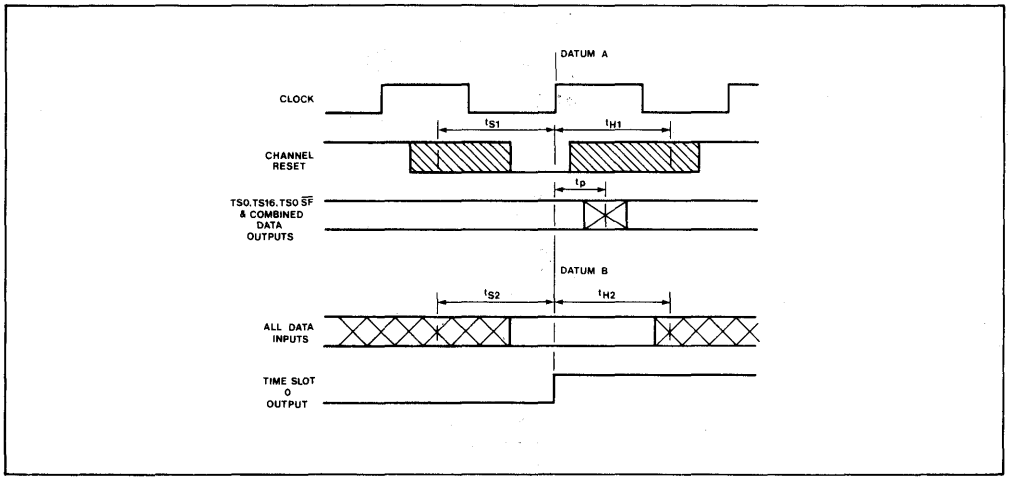

Fig.6 Timing definitions