PLESSEY
Semiconductors

2 MBIT PCM SIGNALLING CIRCUIT

MJ1471

HDB3 OR AMI ENCODER/DECODER

The MJ1471 is an encoder/decoder for pseudo-ternary transmission codes. The codes are true Alternate Mark Inversion (AMI) or AMI modified according to HDB3 rules (CCITT Orange Book Vol 111-2, Annex to Rec.G703). The device encodes and decodes simultaneously and asynchronously. Error monitoring functions are provided to detect violations of HDB3 coding and all ones detection (AIS). In addition a loop test function is provided for terminal testing.

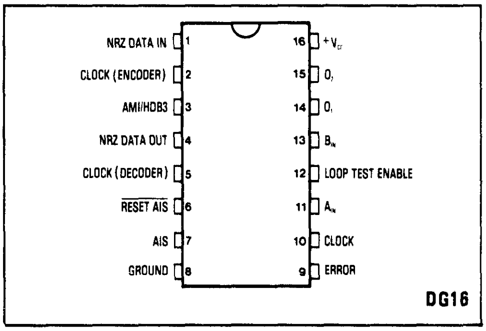

Fig.1 Pin connections

FUNCTIONS

- 5V ±5% Supply—40mA Max.
- AMI or HDB3 Operation—TTL Selectable
- Loop Back Facility
- 'All Ones' Error Monitor to Detect Loss of Synchronising Word (Time Slot Zero)
- Error Monitor of HDB3 Incoming Code
- Decoded Data in NRZ Form

FUNCTIONAL DESCRIPTION

Functions listed by pin number

1. NRZ data in
Input data for encoding into ternary form. The data is clocked by the negative-going edge of the Clock (Encoder).

2. Clock (Encoder)
Clock for encoding data on pin 1.

3. AMI/HDB3
MJ1471 operates in HDB3 if pin 3 is at logic '1'. AMI if pin 3 is at logic '0'.

4. NRZ Data out
Decoded data from ternary inputs A_{in}, B_{in}.

5. Clock (Decoder)
Clock for decoding ternary data A_{in}, B_{in}.

6, 7. $\overline{\text{Reset AIS}}$, AIS
Logic '0' on $\overline{\text{Reset AIS}}$ resets a decoded zero counter and either resets AIS outputs to zero provided 3 or more zeroes have been decoded in the preceding $\overline{\text{Reset AIS}}$ = 1 period or sets AIS to '1' if less than 3 zeroes have been decoded in the preceding two $\overline{\text{Reset AIS}}$ = 1 periods.
Logic '1' on $\overline{\text{Reset AIS}}$ enables the internal decoded zero counter.

8. Ground
Zero volts.

9. Error
A logic '1' indicates that a violation of the HDB3 encoding law has been decoded i.e. 3 '1's of the same polarity.

10. Clock
OR function of A_{in}, B_{in} for clock regeneration when pin 12 = '0', OR function of O_1 O_2 when pin 12 = '1'.

11, 13. A_{in}, B_{in}
Inputs representing the received ternary PCM signal. A_{in} = '1' represents a positive going '1', B_{in} = '1' represents a negative going '1'. A_{in} and B_{in} are sampled by the positive going edge of the clock decoder. A_{in} and B_{in} may be interchanged.

12. Loop test enable
TTL input to select normal or loop back operation. Pin 12 = '0' selects normal operation, encode and decode are independent and asynchronous.
When pin 12 = '1' O_1 is connected internally to A_{in} and O_2 to B_{in}. Clock becomes the OR function of O_1 O_2. **N.B.** a decode clock has to be supplied. The delay from NRZ in to NRZ out is 7½ clock periods in loop back.

14, 15, O_1, O_2
Outputs representing the ternary encoded PCM AMI/HDB3 signal for line transmission. O_1 and O_2 are in Return to zero form and are clocked out on the positive going edge of the encode clock. The length of O_1 and O_2 pulses is set by the positive clock pulse length.

16. $+V_{CC}$
Positive 5V ±5% supply.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage $V_{CC} = 5V \pm 0.25V$
Ambient temperature $T_{amb} = 0°C$ to $+70°C$

Static Characteristics

Characteristic	Symbol	Pins	Value			Units	Conditions
			Min	Typ	Max		
Low level input voltage	V_{IL}	1,2,3,5,6 10,11,12,13	-0.3		0.8	volts	
Low level input current	I_{IL}	1,2,3,5,6 10,11,12,13			50	μA	$V_{IL} = 0V$
High level input voltage	V_{IH}	1,2,3,5,6 10,11,12,13	2.5		V_{cc}	V	
High level input current	I_{IH}	1,2,3,5,6 10,11,12,13			50	μA	$V_{IH} = 5V$
Low level output voltage	V_{OL}	10,14,15			0.5	V	Isink = 800μA
		4,7,9			0.4	V	Isink = 1.6mA
High level output voltage	V_{OH}	4,7,9	2.7			V	Isource = 60μA
		14,15	2.8			V	Isource = 2mA
		10	2.8			V	Isource = 1mA
Supply current	I_{cc}			20	40	mA	All inputs to 0v All outputs open circuit

Dynamic Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Max. Clock (Encoder) frequency	$fmax_{enc}$	4.0			MHz	Figs.9, 14
Max. Clock (Decoder) frequency	$fmax_{dec}$	2.2			MHz	Figs.10, 14
Propagation delay Clock (Encoder) to O_1, O_2	tpd1A/B			100	ns	Figs.8, 9, 14. See Note 1
Rise and Fall times O_1, O_2				20	ns	Figs.9, 14
tpd1A-tpd1B				20	ns	Figs.9, 14
Propagation delay Clock (Encoder) to Clock	tpd3			150	ns	Loop test enable = 1, Figs.9, 14
Setup time of NRZ data in to Clock (Encoder)	ts3	30			ns	Figs.7, 9, 14
Hold time of NRZ data in	th3	55			ns	Figs.7, 9, 14
Propagation delay A_{in}, B_{in} to Clock	tpd2			150	ns	Loop test enable = '0' Figs.12, 14
Propagation delay Clock (Decoder) to error	tpd4			200	ns	Figs.11, 14
Propagation delay $\overline{\text{Reset AIS}}$ to AIS	tpd5			200	ns	Loop test enable = '0' Figs.13, 14
Propagation delay Clock (Decoder) to NRZ data out	tpd6			150	ns	Figs.7, 10, 14. See Note 2
Setup time of A_{in}, B_{in} to Clock (Decoder)	ts1	75			ns	Figs.7, 10, 14
Hold time of A_{in}, B_{in} to Clock (Decoder)	th1	5			ns	Figs.7, 10, 14
Hold time of $\overline{\text{Reset AIS}}$ = '0'	th2	100			ns	Figs.7, 13, 14
Setup time Clock (Decoder) to $\overline{\text{Reset AIS}}$	ts2	200			ns	Figs.7, 13, 14
Setup time $\overline{\text{Reset AIS}}$ = 1 to Clock (Decoder)	ts2'	0			ns	Figs.13, 14

NOTES
1. The Encoded ternary outputs (O_1, O_2) are delayed by 3½ clock periods from NRZ data in (Fig.3).
2. The decoded NRZ output is delayed by 3 clock periods from the HDB3 inputs (A_{IN}, B_{IN}) (Fig.4).

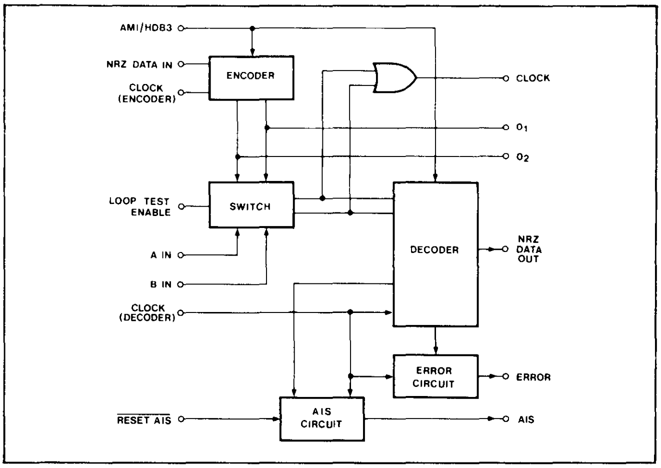

Fig. 2 MJ1471 Block diagram

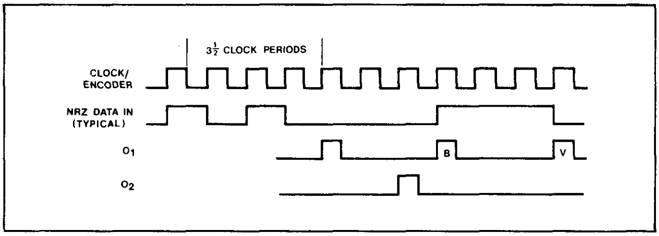

Fig. 3 Encode waveforms

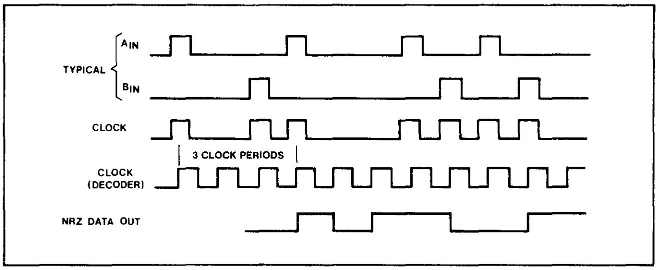

Fig. 4 Decode waveforms

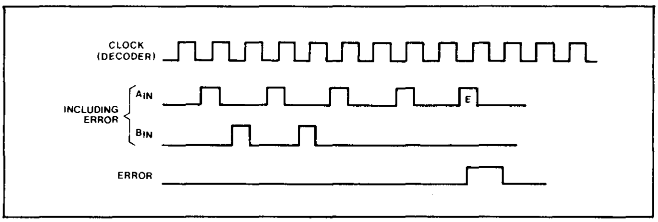

Fig. 5 HDB3 error output waveforms

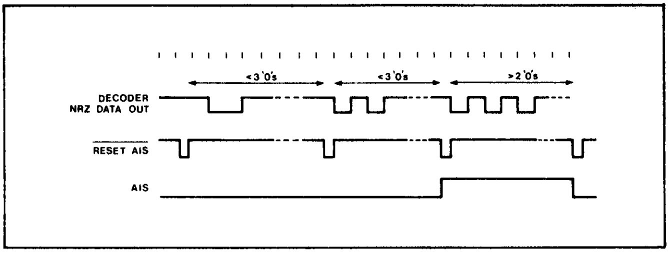

Fig.6 A/S error and reset waveforms

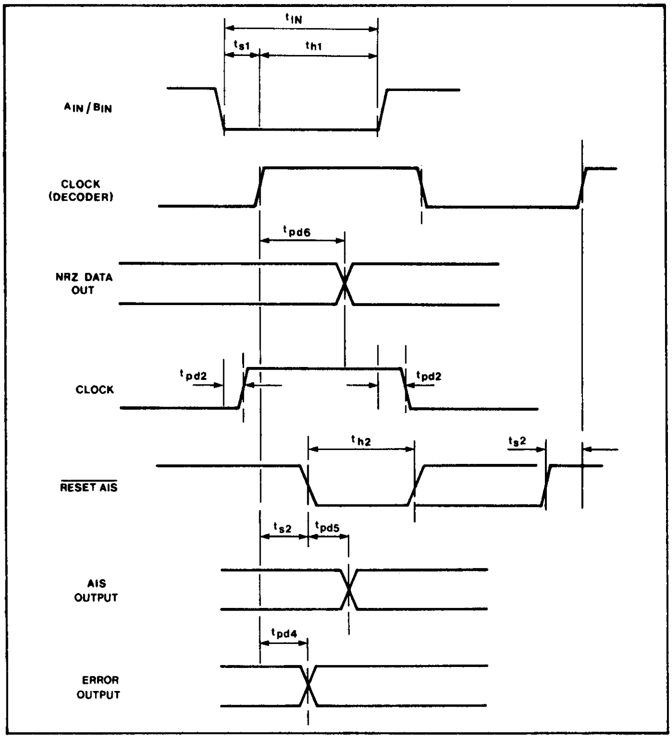

Fig. 7 Decoder timing relationship

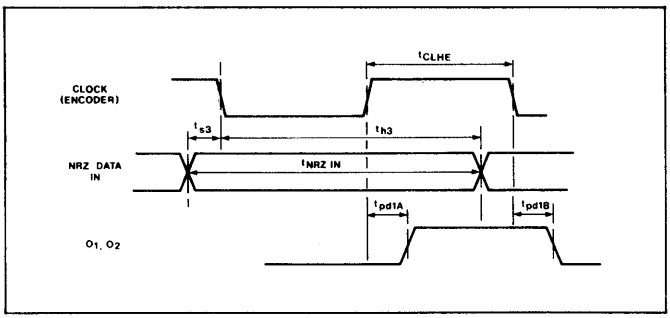

Fig. 8 Encoder timing relationship

DEFINITION OF THE HDB3 CODE

Coding of a binary signal into an HDB3 signal is done according to the following rules:

1. The HDB3 signal is psuedo-ternary; the three states are denoted B_+, B_- and O.

2. Spaces in the binary signal are coded as spaces in the HDB3 signal. For strings of four spaces however, special rules apply (see 4. below).

3. Marks in the binary signal are coded alternately as B_+ and B_- in the HDB3 signal (alternate mark inversion). Violations of the rule of alternate mark inversion are introduced when coding strings of four spaces (see 4. below).

4. Strings of four spaces in the binary signal are coded according to the following rules:

a The first space of a string is coded as a space if the preceding mark of the HDB3 signal has a polarity opposite to the polarity of the preceding violation and is not a violation by itself; it is coded as a mark, i.e. not a violation (i.e. B_+, B_-), if the preceding mark of the HDB3 signal has the same polarity as that of the preceding violation or is by itself a violation.
This rule ensures that successive violations are of alternative polarity so that no DC component is introduced.

b The second and third spaces of a string are always coded as spaces.

c The last space of a string of four is always coded as a mark, the polarity of which is such that it violates the rule of alternate mark inversion. Such violations are denoted V_+ or V_- according to their polarity.

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Electrical Ratings

+Vcc	7V
Inputs	Vcc + 0.5V Gnd − 0.3V
Outputs	Vcc, Gnd −0.3V

Thermal Ratings

Max Junction Temperature 175°C

Thermal Resistance:	Chip to Case	Chip to Amb.
	40°C/Watt	120°C/Watt

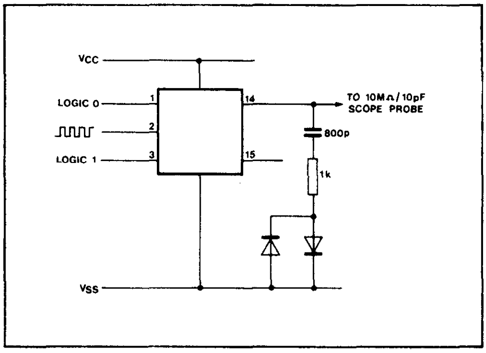

Fig. 9

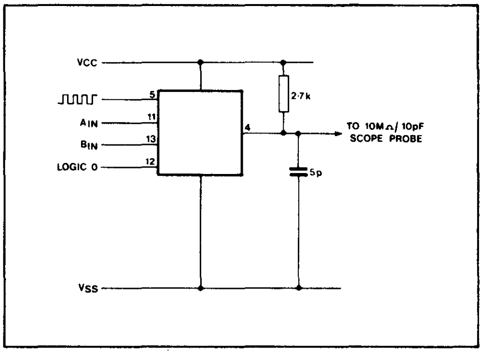

Fig. 10

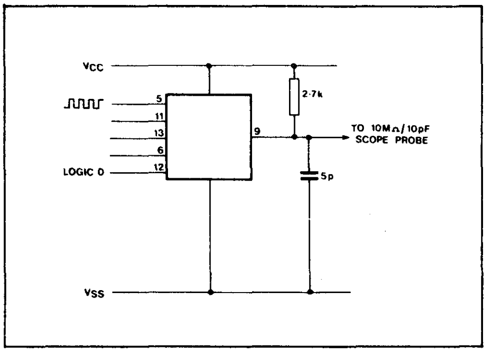

Fig. 11

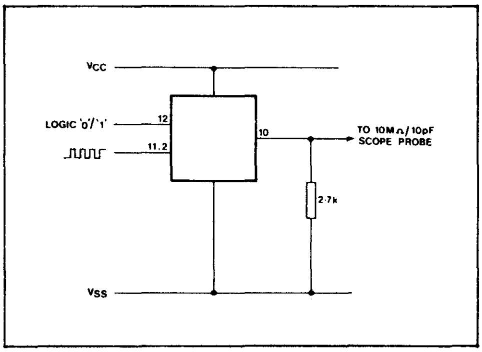

Fig. 12

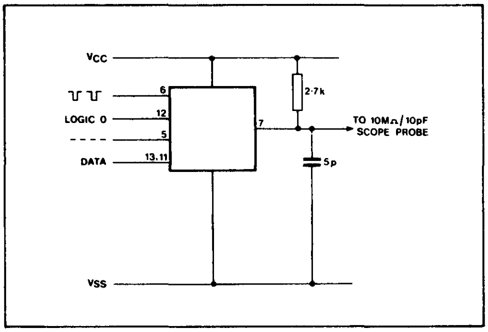

Fig. 13

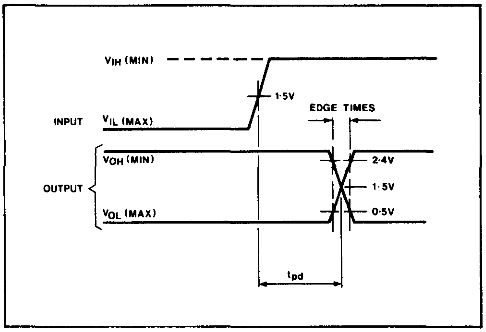

Fig. 14 Test timing definitions