PLESSEY
Semiconductors

MJ1473

PCM TRANSMITTER CIRCUIT

The MJ1400 Series of circuits have been specifically designed for use in 30 channel PCM systems.

The MJ1473 is designed to simplify the transmit section of a 30 channel, 2 MBit PCM link by converting NRZ PCM data to either AMI or HDB3 format after inserting a synchronising word in channel 0 (conforming to CCITT recommendations G.703 and G.732).

The data is output in pseudo-ternary form to facilitate driving the line interface via a transformer and AMI or HDB3 code may be remotely selected using bits 2 and 3 in channel 0 of the incoming data stream.

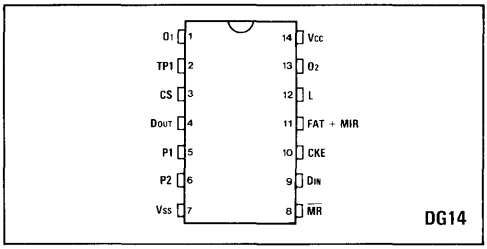

Fig.1 Pin connections - top view

FEATURES

- 5V - 30mA Power Requirements
- 0-70°C Operation
- Complies with Relevant CCITT Recommendations
- Control Signals Compatible with MJ1472,4
- NRZ, AMI or HDB3 Transmission Format
- Transmission Format Controlled Locally or Remotely Via TSO Data
- Fabricated in NMOS Technology
- Inputs and Outputs TTL Compatible

Bit	1	2	3	4	5	6	7	8
Channel 0 TS0.TA	X	0	0	1	1	0	1	1
Channel 0 TS0.TB	X	1	ATL	X	X	X	X	X

Table 1

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin with respect to Vss : 7V
Storage temperature : -55° C to +155° C

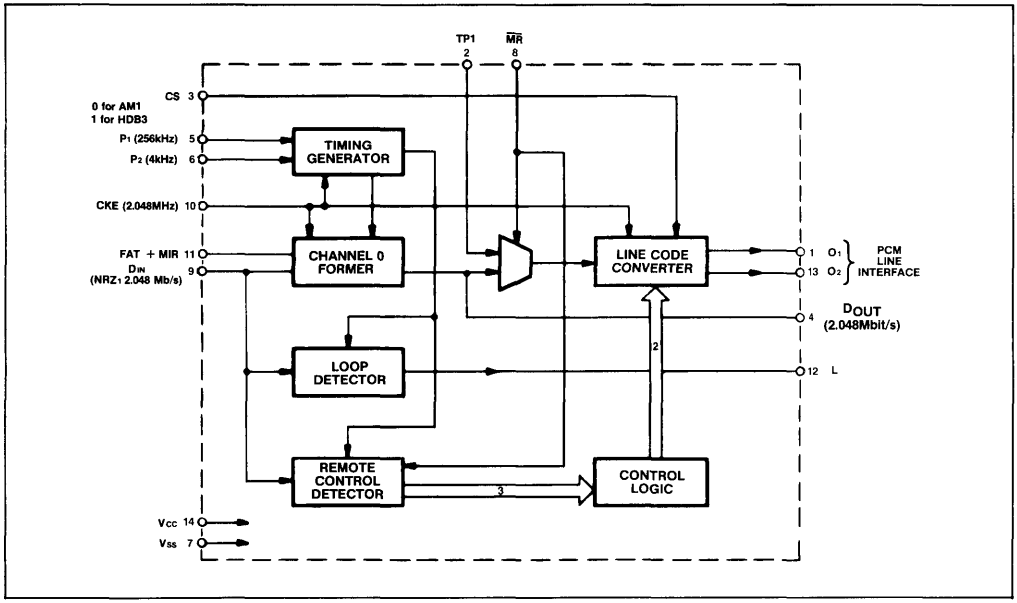

Fig.2 Block diagram of MJ1474

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage 5V ± 0.25V
Ambient operating temperature 0°C to +70°C
Package thermal resistance 95°C/watt

DC CHARACTERISTICS

Characteristic	Symbol	Inputs/outputs	Value			Units	Test conditions
			Min.	Typ.	Max.		
High-level input voltage	V_{IH}	All inputs	2.0			V	
Low-level input voltage	V_{IL}	All inputs			0.8	V	
High-level output voltage	V_{OH}	Outputs L & D_{OUT}	2.7			V	-60μA
Low-level output voltage	V_{OL}	Outputs L & D_{OUT}			0.5	V	0.8mA
High-level input current	I_{IH}	All inputs			50	μA	V_{IN} = 5.25V 25°C
High-level output current	I_{OH1}	Outputs L & D_{OUT}	60			μA	V_{OH} = 2.7V
High-level output current	I_{OH2}	Outputs O_1 & O_2	2			mA	V_{OH} = 2.8V
Low-level output current	I_{OL}	Outputs L & D_{OUT}	0.8			mA	V_{OH} = 0.5V
Input capacitance	C_{IN1}	All inputs except CKE			10	pF	1MHz 100mV
	C_{IN2}	Input CKE			20	pF	
Supply current	I_{CC}			30	45	mA	V_{CC} = 5.25V

AC CHARACTERISTICS

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
O_1 & O_2	t_{pd1}			100	ns	Fig. 4 for loading; measure from CKE leading edge. See Fig. 5 for definition: total delay in t_{pd1} + 4 CKE periods.
L (Propagation delays)	t_{pd2}			200	ns	Fig. 3 for loading; measure from CKE trailing edge. See Fig. 5 for definition.
D_{OUT}	t_{pd3}			180	ns	Fig. 3 for loading; measure from CKE leading edge. See Fig. 5 for definition: total delay is t_{pd3} + 8 CKE periods.
Rise and fall times of O_1 & O_2	t_r/t_f			20	ns	Fig. 4 for loading. Measured between 0.5V and 2.4V points.
Required delay from D_{IN} P1.P2 transition to CKE TE	t_1	50		430	ns	
Required delay from FAT + MIR transition to CKE LE	t_2	50		430	ns	
Required delay from CS transition to CKE TE	t_3	50		430	ns	

CIRCUIT DESCRIPTION

The MJ1473 generates exchange timing by a synchronous 9-bit counter driven by exchange clock CKE and preset by P1,P2. The exchange clock also clocks data, D_{IN},through the channel 0 former and to D_{OUT} via an eight bit shift register. In the channel 0 former, data bits of channel 0 are modified as shown in Table 1.

An X in Table 1 indicates transparency through the circuit, bits 2 and 3 of the shift register are concerned with the loop command circuitry. When '01' is detected an internal latch is set and the loop condition on output L is registered.

D_{OUT} may also be routed through the HDB3/AMI Encoder. The CS control is logic '0' for AMI and logic '1' for HDB3. Encoded data is then output to O_1 and O_2 in a form suitable for driving the PCM interface.

The line code converter can also be controlled by the remote control commands present on bits 2 and 3 of the shift register. These commands are as follows:

1. The presence of '00' in the first frame yields AMI transmission except channel 0 and 1, which are transmitted in a code determined by CS.
   The presence of '00' in each consecutive frame yields unipolar transmission except in channel 0 and 1 as above. The polarity of unipolar transmission is constant for any number of consecutive '00' frames but will alternate with respect to the previous unipolar transmission provided there has been an intermediate frame where '00' was not detected.
2. The presence of '11' in any frame yields AMI transmission except for channel 0 and 1 which are transmitted in a code determined by CS.

ATL is forced to a '1' by the presence of the external signal FAT + MIR, or by the presence of one of the two remote control commands or by the loop comand.

An 'all ones' condition on the encoded data outputs (O_1 O_2) is forced in the presence of a '1' in position 4 of channel 0, when the loop condition is met.

For normal operation $\overline{MR}$ = TP1 = 1. The test point TP1 is provided as an input independent of the line code converter. In order to enable this input when $\overline{MR}$ = 0.

All inputs and outputs are compatible with LSTTL.

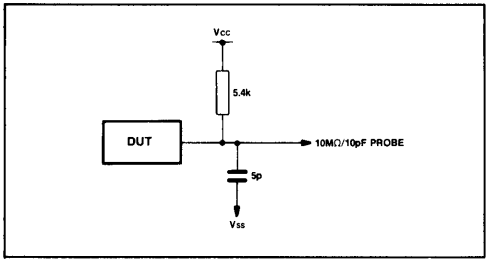

Fig.3 Propagation delay test circuits

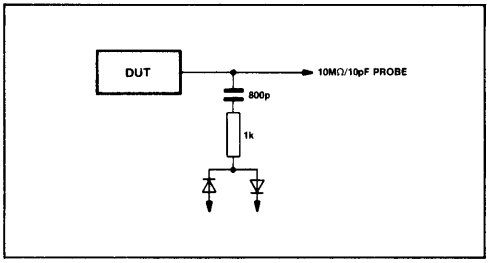

Fig.4

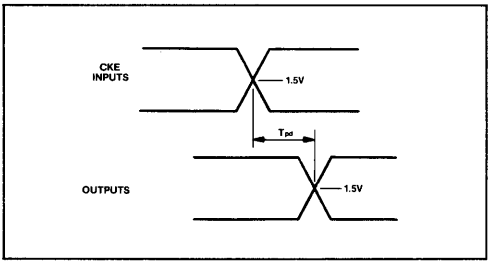

Fig.5 Waveforms for t_{pd}

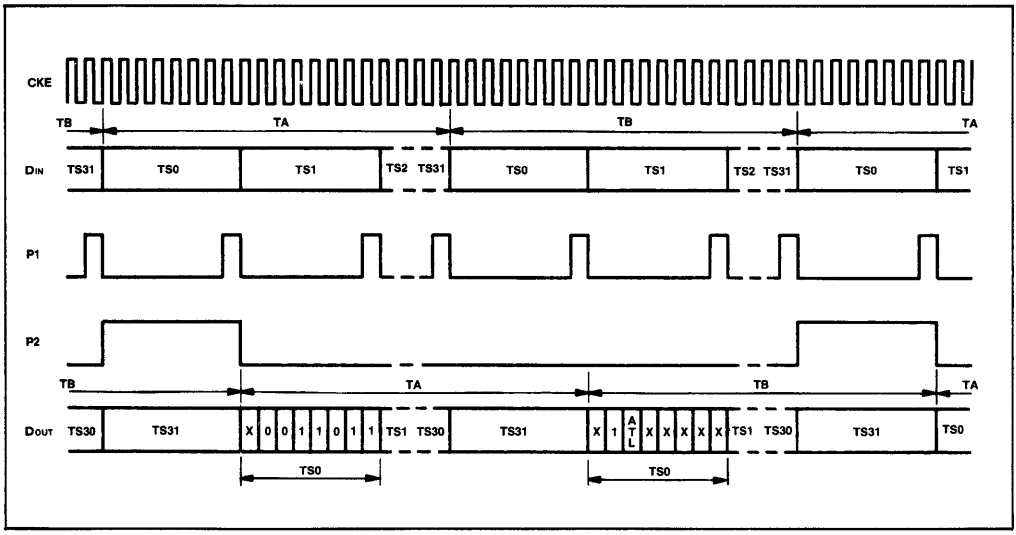

Fig.6 Timing diagram