PLESSEY Semiconductors

ADVANCE INFORMATION

Advance information is issued to advise Customers of new additions to the Plessey Semiconductors range which, nevertheless, still have '*pre-production*' status. Details given may, therefore, change without notice although we would expect this performance data to be representative of '*full production*' status product in most cases. Please contact your local Plessey Semiconductors Sales Office for details of current status.

MJ1474

PCM ELASTIC STORE

The MJ1400 Series of circuits have been specifically designed for use in 30 channel PCM systems.

The MJ1474 retimes the received 30 (+2) channel PCM data stream to the exchange clock and also produces a 5-bit output which identifies the individual channels within the retimed data stream.

Slip is handled by control logic which causes a repetition (or jump) of channel 0 for two consecutive frames whenever the Store capacity is about to be exceeded.

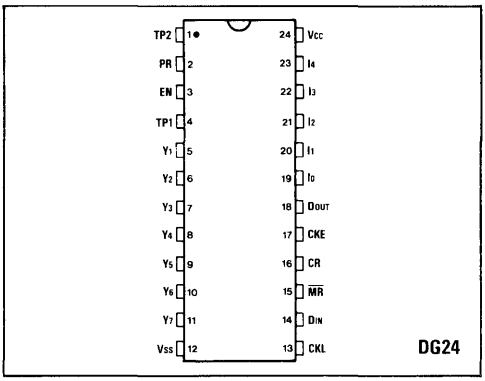

Fig.1 Pin connections - top view

FEATURES

- 5V - 50mA Power Requirements
- Performance Guaranteed Over 0-70°C Temperature Range
- Performs Slip/Alignment Function in 2.048 MBit PCM Systems
- Conforms to Relevant CCITT Recommendations
- Compatible with MJ1472, 3 Control Formats
- Fabricated in NMOS Technology
- Inputs and Outputs TTL Compatible

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin with respect to Vss : 7V

Storage temperature : -55° C to +155° C

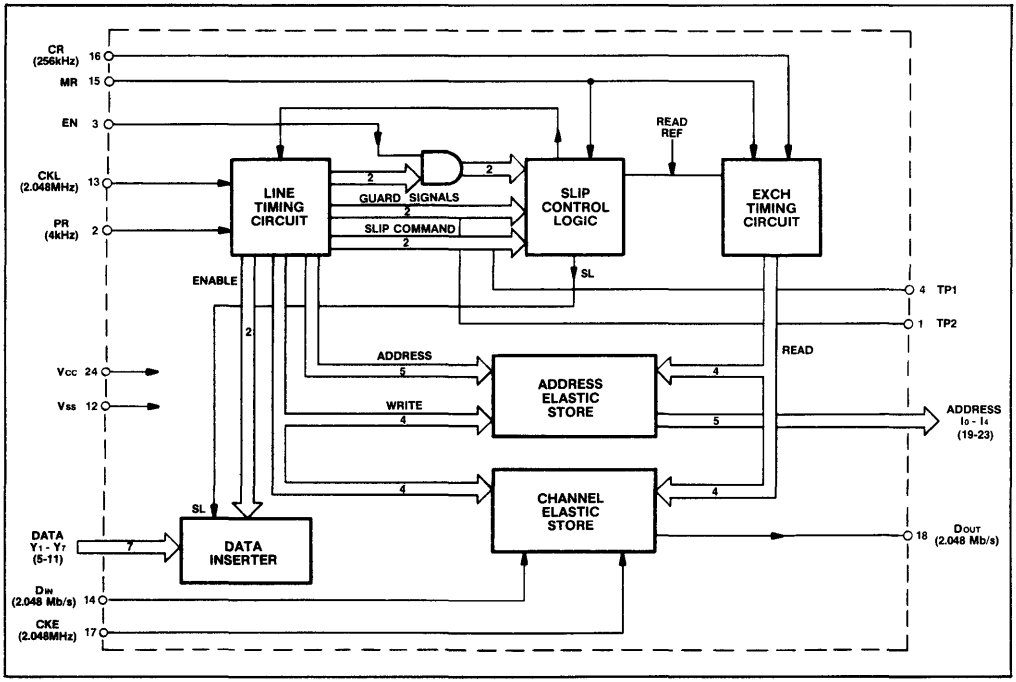

Fig. 2 Block diagram of MJ1473

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage 5V ± 0.25V
Ambient operating temperature 0° C to +70° C
Package thermal resistance 60° C/watt

DC CHARACTERISTICS

Characteristic	Symbol	Inputs/outputs	Value			Units	Test conditions
			Min.	Typ.	Max.		
High-level input voltage	V_{IH}	All inputs	2.0			V	
Low-level input voltage	V_{IL}	All inputs			0.8	V	
High-level output voltage	V_{OH}	All outputs	2.7			V	-60μA
Low-level output voltage	V_{OL}	All outputs except I_0 - I_4			0.5	V	0.8mA
High-level input current	I_{IH}	All inputs			50	μA	V_{IN} = 5.25V 25° C
Low-level output voltage	V_{OL1}	Outputs I_0 - I_4			0.4	V	3mA
High-level output current	I_{OH}	All outputs	60			μA	V_{OH} = 2.7V
Low-level output current	I_{OL0}	All outputs except I_0 - I_4	0.8			mA	V_{OH} = 0.5V
Low-level output current	I_{OL1}	Outputs I_0 - I_4	3.0			mA	V_{OL} = 0.4V
Input capacitance	C_{IN}	All inputs			10	pF	1MHz 100mV
Supply current	I_{CC}			50	80	mA	

AC CHARACTERISTICS

Characteristics	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
D_{OUT}	t_{pd1}			100	ns	Fig. 4 for loading; measure from CKE leading edge. See Fig. 5 for definition.
TP1	t_{pd2}			150	ns	Fig. 3 for loading; measure from CR and CKL. See Fig. 5 for definition.
TP2	t_{pd3}			150	ns	Fig. 3 for loading; measure from CKL trailing edge. See Fig. 5 for definition.
I_0 - I_4	t_{pd4}			200	ns	Fig. 4 for loading: measure from CR trailing edge.
Propagation delays						
Required delay from D_{IN} transition to CKL leading edge	t_1	50		430	ns	
Required delay from FAT + MIR transition to CKL leading edge	t_2	50		430	ns	
Required delay from CS transition to CKL trailing edge	t_3	50		430	ns	

CIRCUIT DIAGRAM

The line timing circuit consists of a 9-bit counter clocked by CKL and preset by PR. Counter states are decoded to form slip commands for the slip control logic and enable signals for the data inserter. The counter also controls the switching logic that delivers the write signals for the two elastic stores, i.e. channel and address, and the guard signals for the slip control circuit.

The channel elastic store has the function of retiming the 32 channels from D_{IN}, clocked by CKL, to D_{OUT} clocked by the exchange clock CKE. The address elastic store has the function of retiming the address of the 32 channels from the line clock CKL to parallel I_0 to I_4 outputs clocked by the exchange clock CKE.

The elastic stores are controlled by a slip control logic, which compares guard signals and the read reference signal. The read reference is generated together with 4 read signals from a 2-bit counter, driven by CR, in the exchange timing circuit. When the store capacity is about to be exceeded the slip control logic becomes active. The effects are a repetition (or jump) of channel zero for the two consecutive frames. Full capacity is always recovered after a normal slip. The contents of all other channels are unchanged during a slip.

A slip may also be forced in the presence of signal EN. This effect is a repetition (or jump) of channel 0 and address 0 for one frame only.

The data inserter modifies channel 0 data out according to Table 1:

Position	1	2	3	4	5	6	7	8
Frame TA	X	X	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6
Frame TB	X	1	Y_7	SL	X	X	X	X

Table 1 TSO format

Where SL is generated by the slip control logic Y_1 to Y_7 are external inputs and X indicates transparency through the circuit.

The circuit also has a master reset (MR) input for initialization of slip control and exchange timing circuits. TP1 and TP2 are also available as test points.

All inputs and outputs are compatible with LSTTL. Outputs I_0 - I_4 are capable of sinking 3mA at 0.4V.

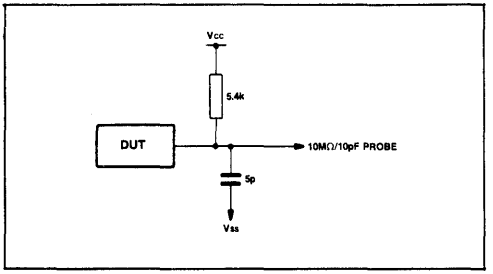

Fig.3

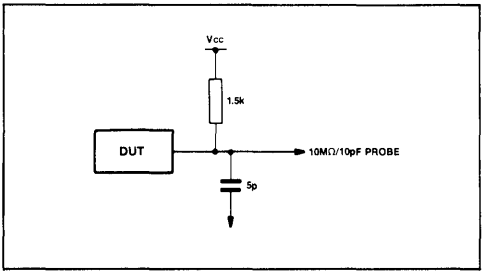

Fig.4

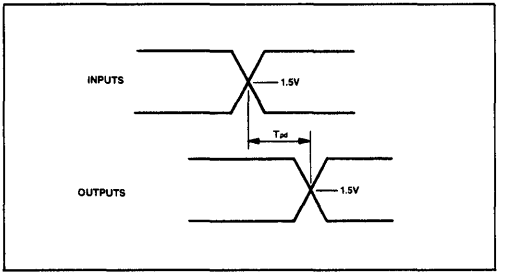

Fig.5 Waveforms for t_{pd}

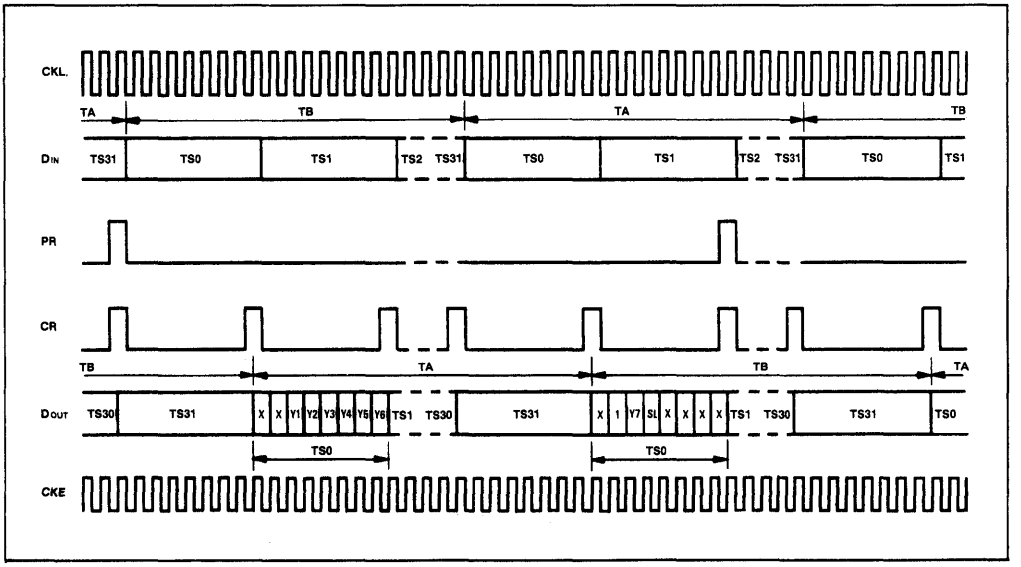

Fig.6 Timing diagram