# MJ21195 - PNP MJ21196 - NPN

Preferred Devices

# **Silicon Power Transistors**

The MJ21195 and MJ21196 utilize Perforated Emitter technology and are specifically designed for high power audio output, disk head positioners and linear applications.

#### **Features**

- Total Harmonic Distortion Characterized
- High DC Current Gain  $h_{FE} = 25$  Min @  $I_C = 8$  Adc
- Excellent Gain Linearity
- High SOA: 3 A, 80 V, 1 Sec
- Pb-Free Packages are Available\*

#### **MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V <sub>CEO</sub>	250	Vdc
Collector-Base Voltage	V <sub>CBO</sub>	400	Vdc
Emitter-Base Voltage	V <sub>EBO</sub>	5	Vdc
Collector–Emitter Voltage – 1.5V	V <sub>CEX</sub>	400	Vdc
Collector Current – Continuous – Peak (Note 1)	I <sub>C</sub>	16 30	Adc
Base Current – Continuous	I <sub>B</sub>	5	Adc
Total Device Dissipation @ T <sub>C</sub> = 25°C Derate above 25°C	P <sub>D</sub>	250 1.43	W W/°C
Operating and Storage Junction Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-65 to +200	°C

### THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{ heta JC}$	0.7	°C/W

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Pulse Test: Pulse Width = 5 μs, Duty Cycle ≤10%.



### ON Semiconductor®

http://onsemi.com

# 16 AMPERES COMPLEMENTARY SILICON-POWER TRANSISTORS 250 VOLTS, 250 WATTS



TO-204AA (TO-3) CASE 1-07

### **MARKING DIAGRAM**



MJ2119x = Device Code

x = 5 or 6

G = Pb-Free Package A = Assembly Location

Y = Year WW = Work Week MEX = Country of Origin

#### **ORDERING INFORMATION**

Device	Package	Shipping
MJ21195	TO-204	100 Units / Tray
MJ21195G	TO-204 (Pb-Free)	100 Units / Tray
MJ21196	TO-204	100 Units / Tray
MJ21196G	TO-204 (Pb-Free)	100 Units / Tray

**Preferred** devices are recommended choices for future use and best overall value.

<sup>\*</sup>For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## **ELECTRICAL CHARACTERISTICS** ( $T_C = 25^{\circ}C \pm 5^{\circ}C$ unless otherwise noted)

Characteristic		Symbol	Min	Typical	Max	Unit
OFF CHARACTERISTICS			•	•		
Collector–Emitter Sustaining Voltage (I <sub>C</sub> = 100 mAdc, I <sub>B</sub> = 0)		V <sub>CEO(sus)</sub>	250	-	-	Vdc
Collector Cutoff Current (V <sub>CE</sub> = 200 Vdc, I <sub>B</sub> = 0)	I <sub>CEO</sub>	_	-	100	μAdc	
Emitter Cutoff Current (V <sub>CE</sub> = 5 Vdc, I <sub>C</sub> = 0)	I <sub>EBO</sub>	_	-	100	μAdc	
Collector Cutoff Current (V <sub>CE</sub> = 250 Vdc, V <sub>BE(off)</sub> = 1.5 Vdc)	I <sub>CEX</sub>	-	-	100	μAdc	
SECOND BREAKDOWN		•				
Second Breakdown Collector Current with Base For (V <sub>CE</sub> = 50 Vdc, t = 1 s (non-repetitive) (V <sub>CE</sub> = 80 Vdc, t = 1 s (non-repetitive)	I <sub>S/b</sub>	5 2.5	_	<u>-</u>	Adc	
ON CHARACTERISTICS			•			
DC Current Gain ( $I_C = 8$ Adc, $V_{CE} = 5$ Vdc) ( $I_C = 16$ Adc, $V_{CE} = 5$ Vdc)		h <sub>FE</sub>	25 8		75	-
Base–Emitter On Voltage (I <sub>C</sub> = 8 Adc, V <sub>CE</sub> = 5 Vdc)	V <sub>BE(on)</sub>	-	_	2.2	Vdc	
Collector–Emitter Saturation Voltage ( $I_C = 8$ Adc, $I_B = 0.8$ Adc) ( $I_C = 16$ Adc, $I_B = 3.2$ Adc)	V <sub>CE(sat)</sub>	- -	- -	1.4 4	Vdc	
DYNAMIC CHARACTERISTICS						
Total Harmonic Distortion at the Output $V_{RMS}$ = 28.3 V, f = 1 kHz, $P_{LOAD}$ = 100 $W_{RMS}$	h <sub>FE</sub>	T <sub>HD</sub>		0.0		%
(Matched pair h <sub>FE</sub> = 50 @ 5 A/5 V)	unmatched h <sub>FE</sub> matched		_	0.8	-	
Current Gain Bandwidth Product (I <sub>C</sub> = 1 Adc, V <sub>CE</sub> = 10 Vdc, f <sub>test</sub> = 1 MHz)	f <sub>T</sub>	4	_	-	MHz	
Output Capacitance (V <sub>CB</sub> = 10 Vdc, I <sub>E</sub> = 0, f <sub>test</sub> = 1 MHz)	C <sub>ob</sub>	-	-	500	pF	

<sup>2.</sup> Pulse Test: Pulse Width = 300 µs, Duty Cycle ≤2%

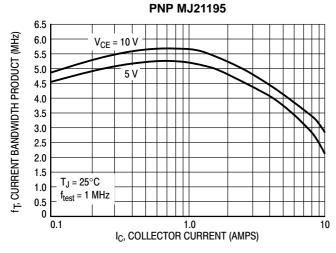
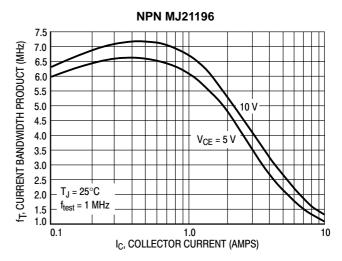


Figure 1. Typical Current Gain Bandwidth Product



**Figure 2. Typical Current Gain Bandwidth Product** 

### TYPICAL CHARACTERISTICS

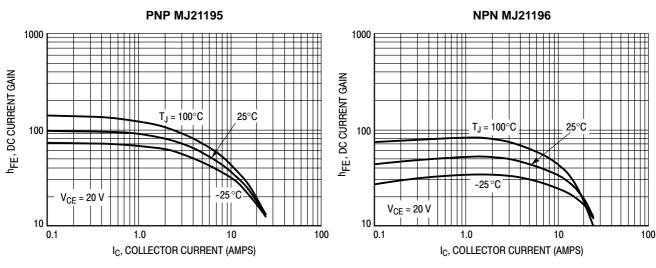


Figure 3. DC Current Gain, V<sub>CE</sub> = 20 V

Figure 4. DC Current Gain, V<sub>CE</sub> = 20 V

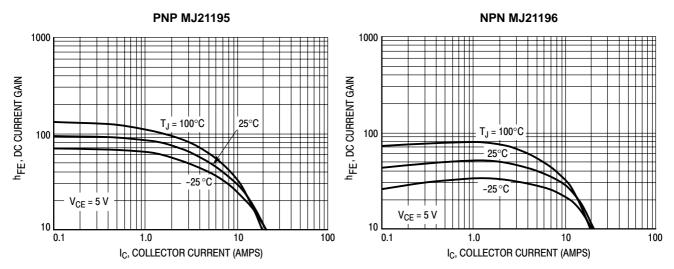


Figure 5. DC Current Gain, V<sub>CE</sub> = 5 V

Figure 6. DC Current Gain,  $V_{CE} = 5 \text{ V}$ 

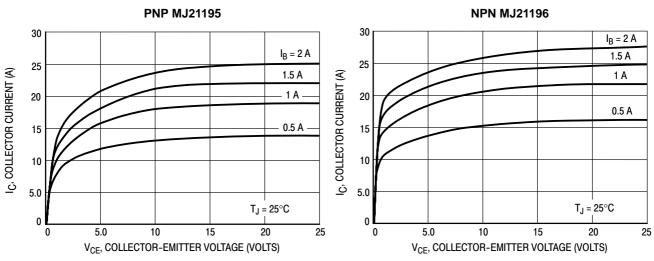
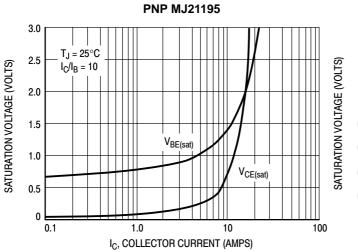


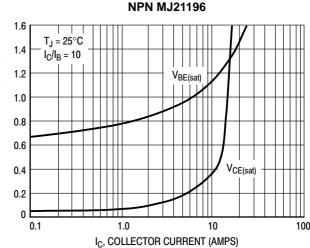
Figure 7. Typical Output Characteristics

Figure 8. Typical Output Characteristics

#### TYPICAL CHARACTERISTICS



**Figure 9. Typical Saturation Voltages** 



**Figure 10. Typical Saturation Voltages** 

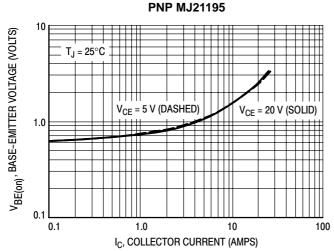


Figure 11. Typical Base-Emitter Voltage

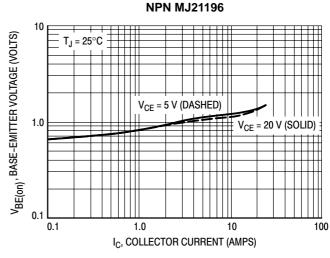


Figure 12. Typical Base-Emitter Voltage

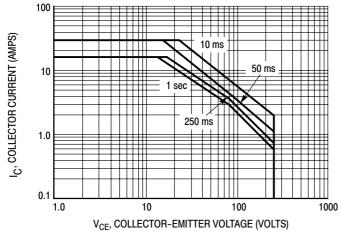


Figure 13. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on  $T_{J(pk)} = 200^{\circ} C$ ;  $T_{C}$  is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

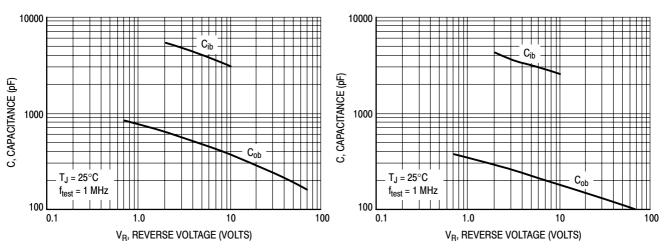


Figure 14. MJ21195 Typical Capacitance

Figure 15. MJ21196 Typical Capacitance

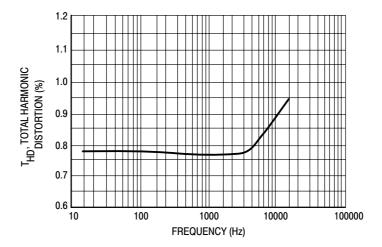


Figure 16. Typical Total Harmonic Distortion

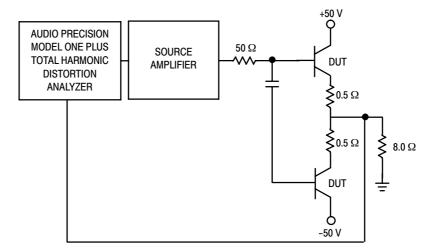
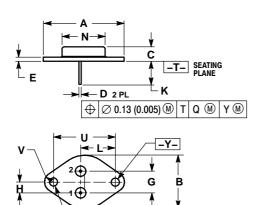


Figure 17. Total Harmonic Distortion Test Circuit

#### PACKAGE DIMENSIONS

**TO-204 (TO-3)**CASE 1-07
ISSUE Z



 $\oplus | \varnothing$  0.13 (0.005) M | T | Y | M

-Q-

#### NOTES

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- 2. CONTROLLING DIMENSION: INCH.
- ALL RULES AND NOTES ASSOCIATED WITH
   REFERENCED TO-204AA OUTLINE SHALL APPLY.

	INCHES		MILLIN	IETERS	
DIM	MIN	MAX	MIN	MAX	
Α	1.550 REF		39.37	REF	
В		1.050		26.67	
С	0.250	0.335	6.35	8.51	
D	0.038	0.043	0.97	1.09	
Ε	0.055	0.070	1.40	1.77	
G	0.430 BSC		10.92 BSC		
Н	0.215 BSC		5.46	BSC	
K	0.440	0.480	11.18	12.19	
L	0.665 BSC		16.89	BSC	
N		0.830		21.08	
Q	0.151	0.165	3.84	4.19	
O	1.187 BSC		30.15	BSC	
٧	0.131	0.188	3.33	4.77	

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use a components in systems intended for surgical implant into the body, or other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### **PUBLICATION ORDERING INFORMATION**

#### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor P.O. Box 61312, Phoenix, Arizona 85082–1312 USA Phone: 480–829–7710 or 800–344–3860 Toll Free USA/Canada Fax: 480–829–7709 or 800–344–3867 Toll Free USA/Canada Email: orderlit@onsemi.com

N. American Technical Support: 800–282–9855 Toll Free USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center 2–9–1 Kamimeguro, Meguro–ku, Tokyo, Japan 153–0051 Phone: 81–3–5773–3850

ON Semiconductor Website: http://onsemi.com

Order Literature: http://www.onsemi.com/litorder

For additional information, please contact your local Sales Representative.