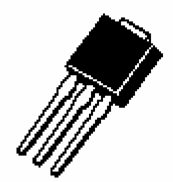
MJD42C TRANSISTOR (PNP)

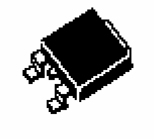
TO-251
TO-252-2L



1.BASE

2.COLLECTOR

3.EMITTER



FEATURES

- Designed for general purpose amplifier and low speed switching applications.
- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("–1" Suffix)
- Lead Formed Version in 16 mm Tape and Reel ("T4" Suffix)
- Electrically Similar to Popular TIP41 and TIP42 Series
- Monolithic Construction With Built–in Base–Emitter Resistors

MAXIMUM RATINGS (T_A=25℃ unless otherwise noted)

Symbol	Parameter	Value	Units
V_{CBO}	Collector-Base Voltage	-100	V
V_{CEO}	Collector-Emitter Voltage	-100	V
V_{EBO}	Emitter-Base Voltage	-5	V
I_C	Collector Current -Continuous	-6	A
P_C	Collector Power Dissipation	1.25	W
T_J	Junction Temperature	150	℃
T_{stg}	Storage Temperature	-65-150	℃

ELECTRICAL CHARACTERISTICS (Tamb=25℃ unless otherwise specified)

Parameter	Symbol	Test conditions	MIN	TYP	MAX	UNIT
Collector-base breakdown voltage	$V_{(BR)CBO}$	I_C=-100μA,I_E=0	-100			V
Collector-emitter breakdown voltage	$V_{(BR)CEO}$	I_C=-30mA,I_B=0	-100			V
Emitter-base breakdown voltage	$V_{(BR)EBO}$	I_E=-100μA,I_C=0	-5			V
Collector cut-off current	I_{CEO}	V_{CB}=-60V,I_E=0			-50	μA
Emitter cut-off current	I_{EBO}	V_{EB}=-5V I_C=0			-0.5	mA
DC current gain	$h_{FE(1)}$	V_{CE}=-4V I_C=-0.3A	30			
	$h_{FE(2)}$	V_{CE}=-4V,I_C=-3A	15		75	
Collector-emitter saturation voltage	$V_{CE(sat)}$	I_C=-6A,I_B=-0.6A			-1.5	V
Base-emitter voltage	V_{BE}	V_{CE}=-4V,I_C=-6A			-2	V
Transition frequency	f_T	V_{CE}=-10V,I_C=-500mA,f=1MHz	3			MHz

Typical Characteristics

TYPICAL CHARACTERISTICS

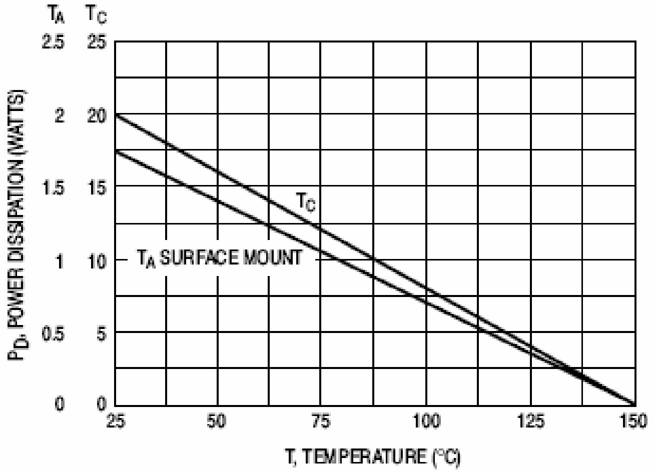
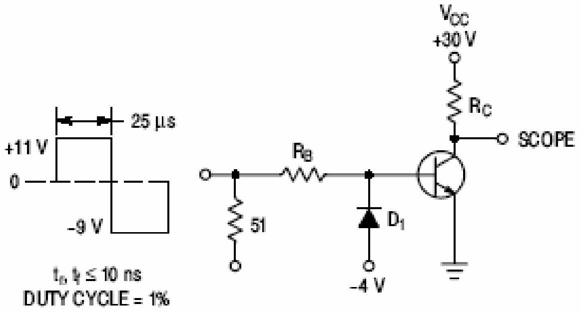


Figure 1. Power Derating



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS
D_1 MUST BE FAST RECOVERY TYPE, e.g.:
MSB5300 USED ABOVE $I_B \approx 100$ mA
MSD6100 USED BELOW $I_B \approx 100$ mA
REVERSE ALL POLARITIES FOR PNP.

Figure 2. Switching Time Test Circuit

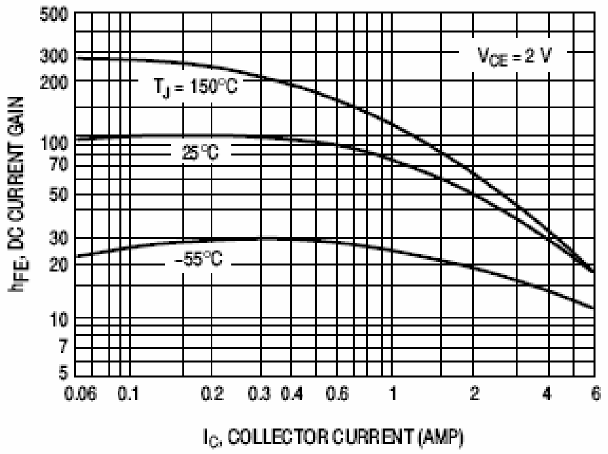


Figure 3. DC Current Gain

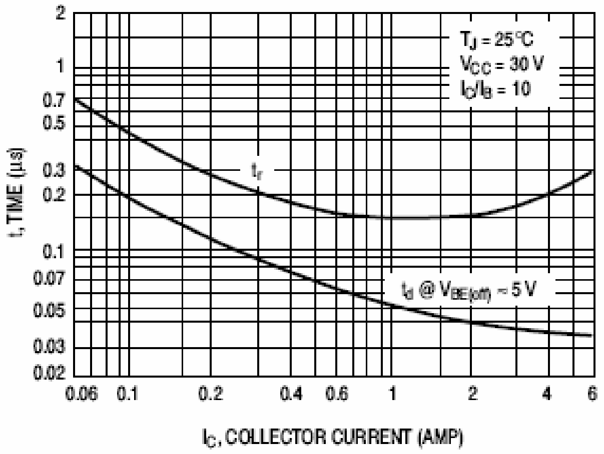


Figure 4. Turn–On Time

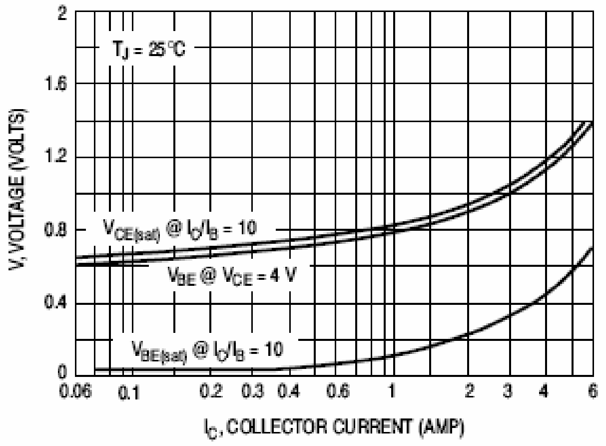


Figure 5. “On” Voltages

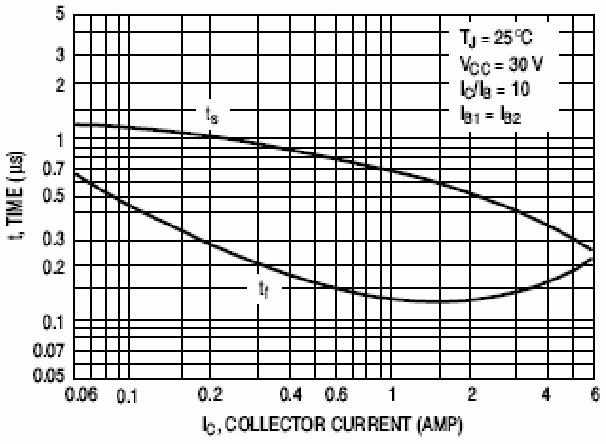


Figure 6. Turn–Off Time

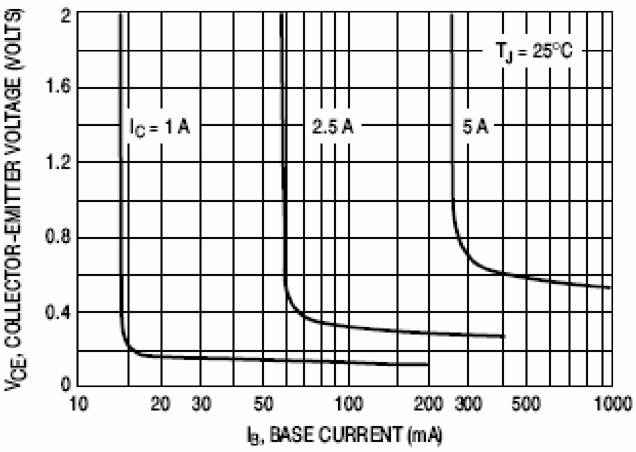


Figure 7. Collector Saturation Region

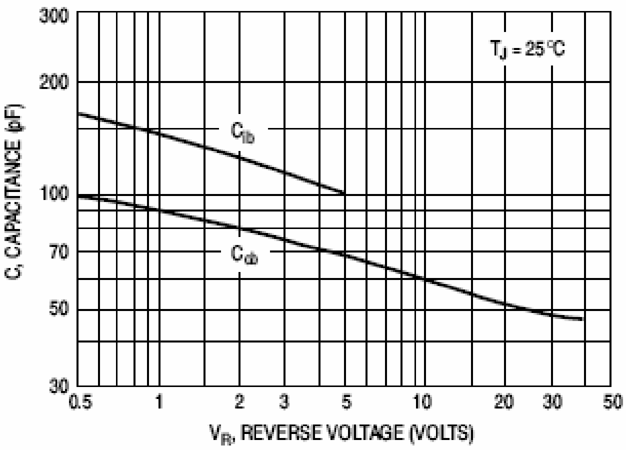


Figure 8. Capacitance

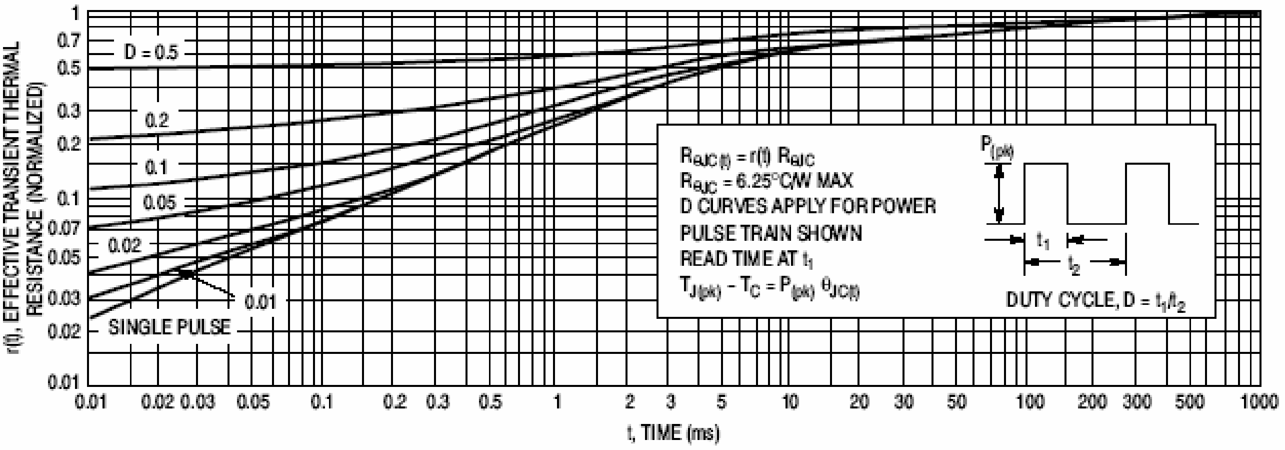


Figure 9. Thermal Response

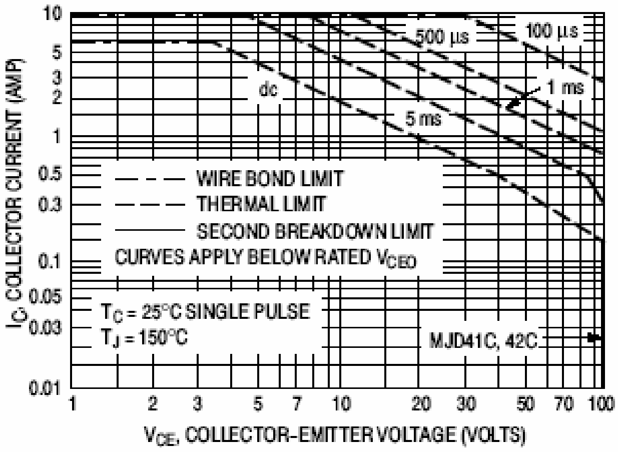


Figure 10. Maximum Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 9. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.