



## MJE13005-H

## NPN SILICON TRANSISTOR

### NPN SILICON POWER TRANSISTORS

#### DESCRIPTION

These devices are designed for high-voltage, high-speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V SWITCHMODE.

#### FEATURES

- \*  $V_{CE0(SUS)} = 400\text{ V}$
- \* Reverse bias SOA with inductive loads @  $T_C = 100^\circ\text{C}$
- \* Inductive switching matrix 2 to 4 Amp, 25 and  $100^\circ\text{C}$   
 $t_c @ 3\text{A}, 100^\circ\text{C}$  is 180 ns (Typ)
- \* 700V blocking capability
- \* SOA and switching applications information

#### APPLICATIONS

- \* Switching regulator's, inverters
- \* Motor controls
- \* Solenoid/Relay drivers
- \* Deflection circuits

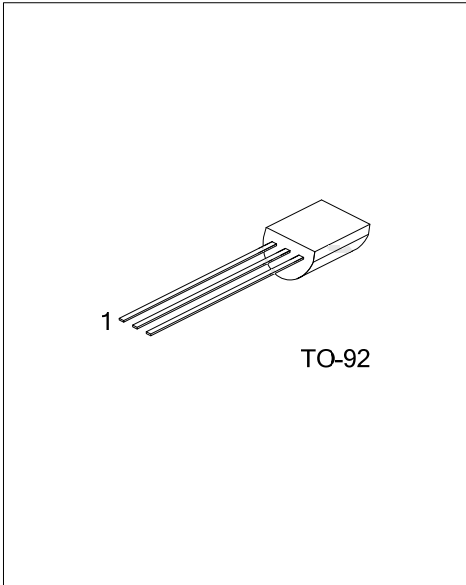
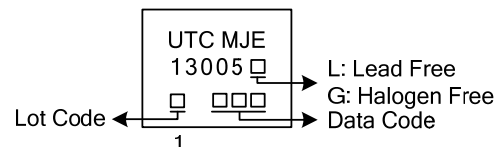
#### ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen-Free		1	2	3	
MJE13005L-H-x-T92-B	MJE13005G-H-x-T92-B	TO-92	B	C	E	Tape Box
MJE13005-L-H-x-T92-K	MJE13005G-H-x-T92-K	TO-92	B	C	E	Bulk

Note: Pin assignment: E: Emitter B: Base C: Collector

<p>MJE13005L-H-x-T92-K</p>	<p>(1) B: Tape Box, K: Bulk (2) T92: TO-92 (3) x: refer to Classification of <math>h_{FE1}</math> (4) L: Lead Free, G: Halogen Free and Lead Free</p>
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#### MARKING



■ ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	RATINGS	UNIT
Collector-Emitter Voltage		$V_{CEO(SUS)}$	400	V
Collector-Emitter Voltage ( $V_{BE}=0$ )		$V_{CES}$	900	V
Collector-Base Voltage		$V_{CBO}$	900	V
Emitter Base Voltage		$V_{EBO}$	9	V
Collector Current	Continuous	$I_C$	4	A
	Peak (1)	$I_{CM}$	8	A
Base Current	Continuous	$I_B$	2	A
	Peak (1)	$I_{BM}$	4	A
Emitter Current	Continuous	$I_E$	6	A
	Peak (1)	$I_{EM}$	12	A
Power Dissipation at $T_A=25^\circ\text{C}$		$P_D$	0.8	W
Derate above $25^\circ\text{C}$			6.4	mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature		$T_J, T_{STG}$	-65 ~ +150	$^\circ\text{C}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	$\theta_{JA}$	150	$^\circ\text{C}/\text{W}$
Junction to Case	$\theta_{JC}$	45	$^\circ\text{C}/\text{W}$

■ ELECTRICAL CHARACTERISTICS (T<sub>C</sub>=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFF CHARACTERISTICS (Note 1)</b>						
Collector-Emitter Sustaining Voltage	V <sub>CEO(SUS)</sub>	I <sub>C</sub> =10mA, I <sub>B</sub> =0	400			V
Collector Cutoff Current	I <sub>CBO</sub>	V <sub>CEO</sub> =Rated Value, V <sub>BE(OFF)</sub> =1.5V			1	mA
		V <sub>CEO</sub> =Rated Value, V <sub>BE(OFF)</sub> =1.5V, T <sub>C</sub> =100°C			5	
Emitter Cutoff Current	I <sub>EBO</sub>	V <sub>EB</sub> =9V, I <sub>C</sub> =0			1	mA
<b>SECOND BREAKDOWN</b>						
Second Breakdown Collector Current with base forward biased	I <sub>S/B</sub>				See Fig. 11	
Clamped Inductive SOA with Base Reverse Biased	RBSOA				See Fig. 12	
<b>ON CHARACTERISTICS (Note 1)</b>						
DC Current Gain	h <sub>FE1</sub>	I <sub>C</sub> =0.5A, V <sub>CE</sub> =5V	15		50	
	h <sub>FE2</sub>	I <sub>C</sub> =1A, V <sub>CE</sub> =5V	10		60	
	h <sub>FE3</sub>	I <sub>C</sub> =2A, V <sub>CE</sub> =5V	8		40	
Collector-Emitter Saturation Voltage	V <sub>CE(SAT)</sub>	I <sub>C</sub> =1A, I <sub>B</sub> =0.2A			0.5	V
		I <sub>C</sub> =2A, I <sub>B</sub> =0.5A			0.6	V
		I <sub>C</sub> =4A, I <sub>B</sub> =1A			1	V
		I <sub>C</sub> =2A, I <sub>B</sub> =0.5A, T <sub>a</sub> =100°C			1	V
Base-Emitter Saturation Voltage	V <sub>BE(SAT)</sub>	I <sub>C</sub> =1A, I <sub>B</sub> =0.2A			1.2	V
		I <sub>C</sub> =2A, I <sub>B</sub> =0.5A			1.6	V
		I <sub>C</sub> =2A, I <sub>B</sub> =0.5A, T <sub>C</sub> =100°C			1.5	V
<b>DYNAMIC CHARACTERISTICS</b>						
Current-Gain-Bandwidth Product	f <sub>T</sub>	I <sub>C</sub> =500mA, V <sub>CE</sub> =10V, f=1MHz	4			MHz
Output Capacitance	C <sub>OB</sub>	V <sub>CB</sub> =10V, I <sub>E</sub> =0, f=0.1MHz		65		pF
<b>SWITCHING CHARACTERISTICS</b>						
Resistive Load (Table 1)						
Delay Time	t <sub>D</sub>	V <sub>CC</sub> =125V, I <sub>C</sub> =2A, I <sub>B1</sub> =I <sub>B2</sub> =0.4A, t <sub>P</sub> =25μs, Duty Cycle≤1%		0.025	0.1	μs
Rise Time	t <sub>R</sub>			0.3	0.7	μs
Storage Time	t <sub>S</sub>			1.7	4	μs
Fall Time	t <sub>F</sub>			0.4	0.9	μs

Note: 1. Pulse Test: Pulse Width=5ms, Duty Cycle≤10%

2. Pulse Test: P<sub>W</sub>=300μs, Duty Cycle≤2%

■ CLASSIFICATION OF h<sub>FE1</sub>

RANK	A	B	C	D	E
RANGE	15 ~ 20	20 ~ 25	25 ~ 30	30 ~ 40	40 ~ 50

## APPLICATION INFORMATION

Table 1. Test Conditions for Dynamic Performance

Reverse Bias Safe Operating Area and Inductive Switching		Resistive Switching
Test Circuits	<p>DUTY CYCLE <math>\leq</math> 10%  <math>t_r, t_f \leq 10\text{ns}</math></p> <p>Note:          PW and <math>V_{cc}</math> Adjusted for Desired <math>I_c</math>  <math>R_B</math> Adjusted for Desired <math>I_{B1}</math></p>	
Circuit Values	<p>Coil Data :  <math>V_{CC}=20V</math>                  FERROXCUBE core #6656                  Full Bobbin ( ~ 16 Turns) #16</p> <p>GAP for 200<math>\mu</math>H/20 A  <math>L_{COIL}=200\mu H</math>      <math>V_{CLAMP}=300V</math></p>	<p><math>V_{CC}=125V</math>  <math>R_C=62\Omega</math>  <math>D1=1n5820</math> or Equiv.  <math>R_B=22\Omega</math></p>
Test Waveforms	<p>OUTPUT WAVEFORMS</p> <p><math>t_1</math> Adjusted to Obtain <math>I_c</math></p> $t_1 = \frac{L_{COIL}(I_{CPK})}{V_{CC}}$ $t_2 = \frac{L_{COIL}(I_{CPK})}{V_{CLAMP}}$ <p>Test Equipment                  Scope-Tektronics 475 or Equivalent</p>	<p><math>t_r, t_f &lt; 10\text{ns}</math>                  Duty Cycle=1.0%  <math>R_B</math> and <math>R_C</math> adjusted for desired <math>I_B</math> and <math>I_C</math></p>

## RESISTIVE SWITCHING PERFORMANCE

Fig. 1 Turn-On Time

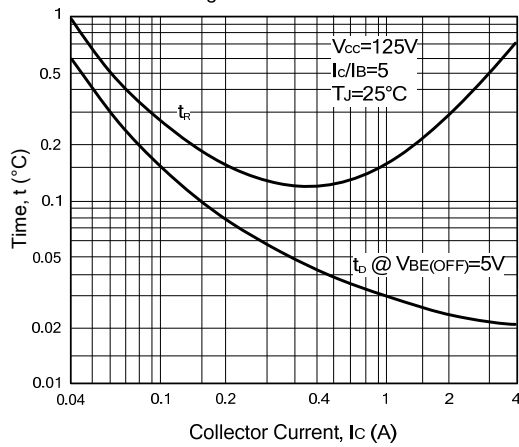


Fig. 2 Turn-Off Time

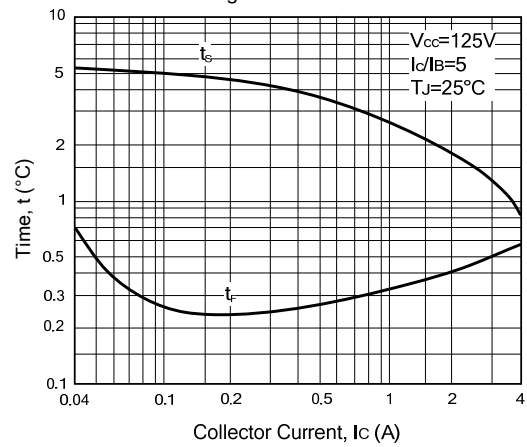


Fig. 3 Typical Thermal Response [ $Z_{\theta JC}(t)$ ]

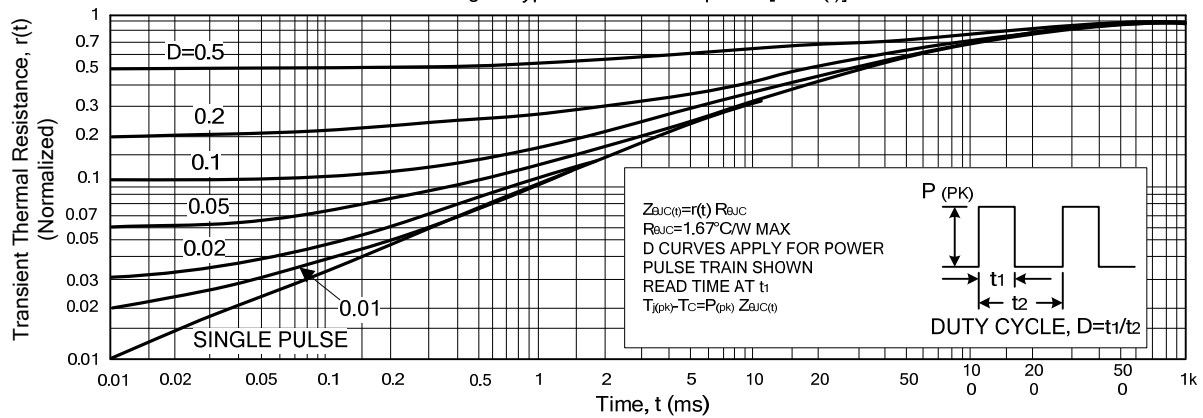
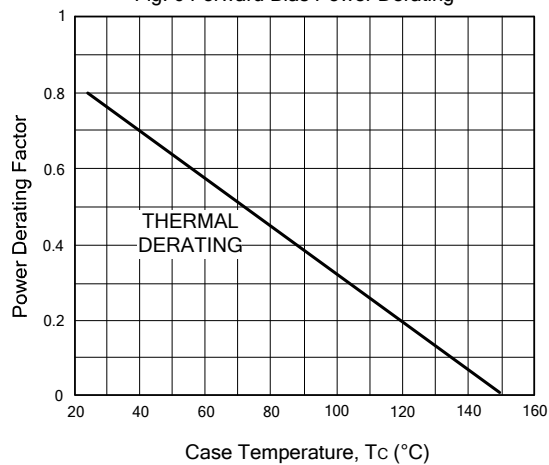


Fig. 6 Forward Bias Power Derating



**■ SAFE OPERATING AREA INFORMATION****FORWARD BIAS**

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C$ - $V_{CE}$  limits of the transistor that must be observed for reliable operation; e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Fig. 4 is based on  $T_C = 25^\circ\text{C}$ ;  $T_{J(PK)}$  is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when  $T_C \geq 25^\circ\text{C}$ . Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Fig. 4 may be found at any case temperature by using the appropriate curve on Fig. 6.

$T_{J(PK)}$  may be calculated from the data in Fig. 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

**REVERSE BIAS**

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 5 gives the complete RBSOA characteristics.

## TYPICAL CHARACTERISTICS

Figure 7. DC Current Gain

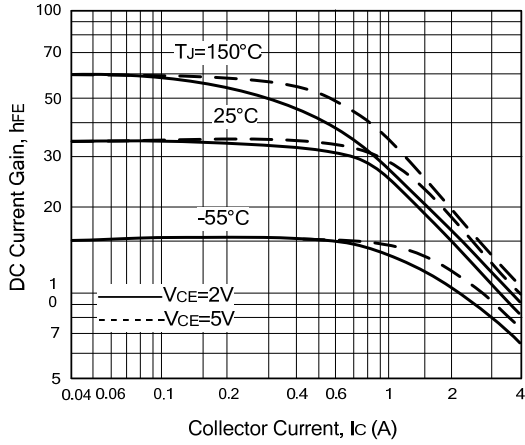


Figure 8. Collector Saturation Region

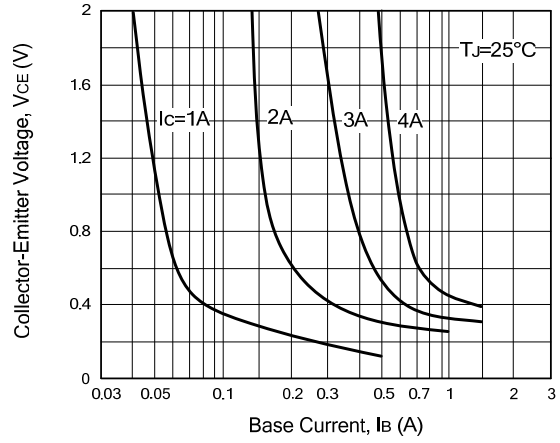


Figure 9. Base-Emitter Voltage

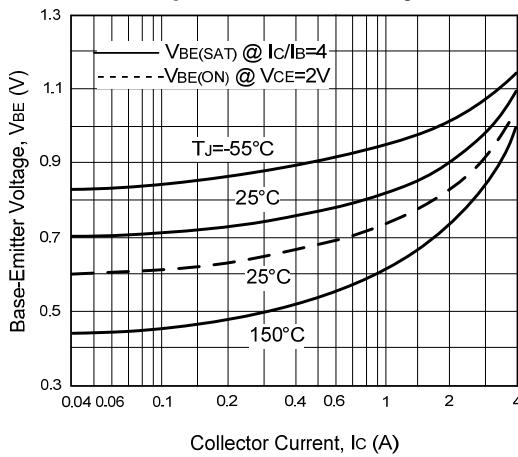


Figure 10. Collector-Emitter Saturation Voltage

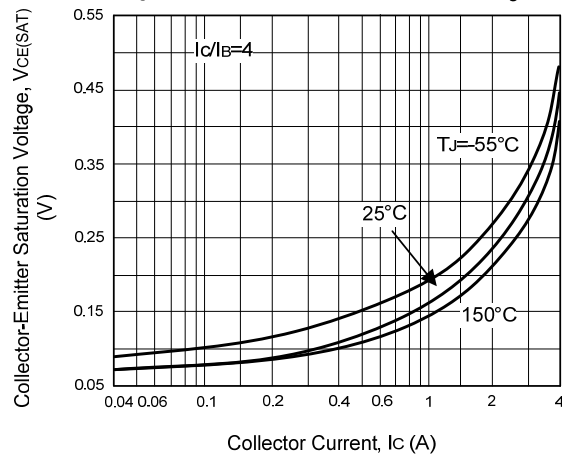


Figure 11. Collector Cutoff Region

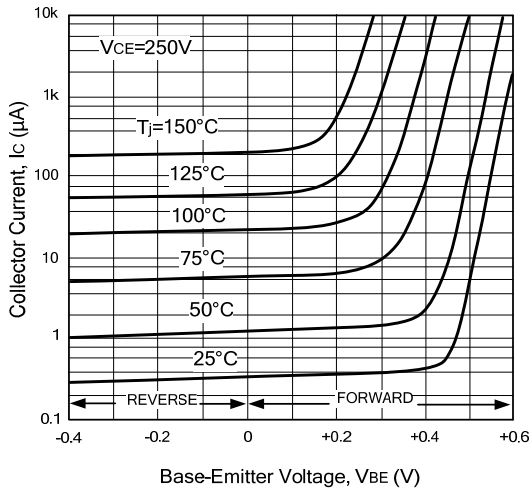
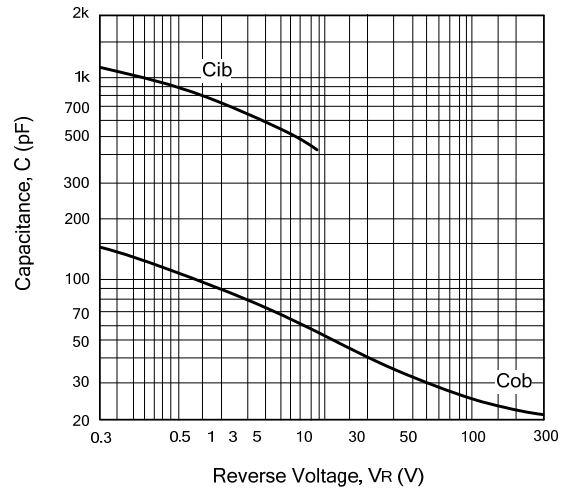


Figure 12. Capacitance



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