## UNISONIC TECHNOLOGIES CO., LTD

### MJE13009-Q

#### **Preliminary**

#### NPN SILICON TRANSISTOR

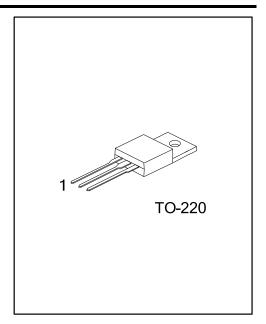
# NPN BIPOLAR POWER TRANSISTOR FOR SWITCHING POWER SUPPLY APPLICATIONS

#### ■ DESCRIPTION

The UTC **MJE13009-Q** is designed for high-voltage, high-speed power switching inductive circuits where fall time is critical. It is particularly suited for 115 and 220 V switch mode applications.

#### ■ FEATURES

- \*  $V_{\text{CEO(SUS)}}400V$
- \* 700V Blocking Capability



#### ■ ORDERING INFORMATION

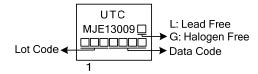
	Ordering Number		Dookogo	Pin Assignment			Dooking	
	Lead Free	Halogen Free	Package	1	2	3	Packing	
ĺ	MJE13009L-Q-TA3-T	MJE13009G-Q-TA3-T	TO-220	В	С	Е	Tube	

Note: Pin Assignment: E: Emitter C: Collector B: Base

MJE13009L-Q-TA3-T

(1)Packing Type
(2)Package Type
(3)Green Package
(3) L: Lead Free, G: Halogen Free and Lead Free

#### MARKING



<u>www.unisonic.com.tw</u> 1 of 4

#### ABSOLUTE MAXIMUM RATING

PARAMETER		SYMBOL	RATINGS	UNIT
Collector-Emitter Sustaining Voltage		$V_{CEO}$	400	V
Collector-Emitter Breakdown Voltage		$V_{CBO}$	700	٧
Emitter-Base Voltage		$V_{EBO}$	9.0	<b>V</b>
Collector Current	Continuous	Ic	8.0	Α
Collector Current	Peak (1)	I <sub>CM</sub>	16	Α
Base Current	Continuous	I <sub>B</sub>	4.0	Α
	Peak (1)	I <sub>BM</sub>	8.0	Α
Emitter Current	Continuous	Ι <sub>Ε</sub>	12	Α
Emiller Current	Peak (1)	I <sub>EM</sub>	24	Α
Power Dissipation (T <sub>C</sub> = 25°C)	ver Dissipation (T <sub>C</sub> = 25°C)		80	W
Junction Temperature		TJ	+150	°C
Storage Temperature		T <sub>STG</sub>	-55~+150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

#### ■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT	
Junction to Ambient	$\theta_{JA}$	62.5	°C/W	
Junction to Case	$\theta_{JC}$	1.56	°C/W	

Note: 1. Pulse Test: Pulse Width = 5.0 ms, Duty Cycle≤10%.

Measurement made with thermocouple contacting the bottom insulated mounting surface of the package (in a location beneath the die), the device mounted on a heatsink with thermal grease applied at a mounting torque of 6 to 8•lbs.

#### ■ ELECTRICAL CHARACTERISTICS (T<sub>C</sub>=25°C, unless otherwise noted)

PARAMETER	SYMBOL	_ TEST CONDITIONS		TYP	MAX	UNIT			
Collector-Emitter Sustaining Voltage	V <sub>CEO(SUS)</sub>	$I_C=10$ mA, $I_B=0$	400			V			
Collector Cutoff Current	Ісво	V <sub>CES</sub> =700V			0.1	mA			
Collector Cuton Current		V <sub>CES</sub> =700V, T <sub>C</sub> =125°C			1.0	mA			
Emitter Cutoff Current	I <sub>EBO</sub>	V <sub>EB</sub> =9.0V, I <sub>C</sub> =0			100	μΑ			
DC Current Gain	h <sub>FE1</sub>	I <sub>C</sub> =2.0A, V <sub>CE</sub> =5.0V	8.0		40				
DC Current Gain	h <sub>FE2</sub>	I <sub>C</sub> =5.0A, V <sub>CE</sub> =5.0V	5.0		30				
	V <sub>CE(SAT)</sub>	I <sub>C</sub> =2.0A, I <sub>B</sub> =0.4A			1.0	V			
Collector Emitter Saturation Voltage		I <sub>C</sub> =5.0A, I <sub>B</sub> =1.0A			2.0	V			
Collector-Emitter Saturation Voltage		I <sub>C</sub> =8.0A, I <sub>B</sub> =2.0A			3.0	V			
		I <sub>C</sub> =5.0A, I <sub>B</sub> =1.0A, T <sub>C</sub> =100°C			3.0	V			
	V <sub>BE(SAT)</sub>	I <sub>C</sub> =2.0A, I <sub>B</sub> =0.4A			1.2	V			
Base-Emitter Saturation Voltage		I <sub>C</sub> =5.0A, I <sub>B</sub> =1.0A			1.6	V			
		I <sub>C</sub> =5.0A, I <sub>B</sub> =1.0A, T <sub>C</sub> =100°C			1.5	V			
Current-Gain-Bandwidth Product	f⊤	I <sub>C</sub> =500mA, V <sub>CE</sub> =10V, f=1.0 MHz	4.0	14		MHz			
Output Capacitance	Сов	$V_{CB}$ =10V, $I_E$ =0, f=0.1MHz		80		pF			
RESISTIVE LOAD (TABLE 1)									
Delay Time	t₀	1051/ 1 5 04		0.025	0.1	μs			
Rise Time	V <sub>CC</sub> =125V, I <sub>C</sub> =5.0A,			0.5	1.5	μs			
Storage Time	ts	I <sub>B1</sub> =I <sub>B2</sub> =1.0A, t <sub>P</sub> =25μs, -Duty Cycle≤1.0%		1.8	3.0	μs			
Fall Time	t <sub>F</sub>	Duty Gyole = 1.070		0.23	0.7	μs			

Note: Pulse Test: Pulse Width≤300µs, Duty Cycle≤2.0%

#### ■ TYPICAL THERMAL RESPONSE

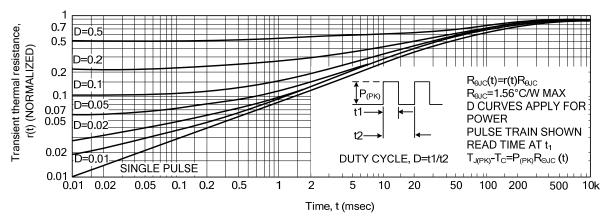


Fig. 1 Typical Thermal Response

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_{C}$ - $V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Fig. 7 is based on  $T_C = 25^{\circ}C$ ;  $T_{J(PK)}$  is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be debated when  $T_C \ge 25^{\circ}C$ . Second breakdown limitations do not debate the same as thermal limitations. Allowable current at the voltages shown on Fig. 7 may be found at any case temperature by using the appropriate curve on Fig. 9.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

Use of reverse biased safe operating area data (Fig. 8) is discussed in the applications information section.

TIME

t2

#### ■ TEST CONDITIONS FOR DYNAMIC PERFORMANCE

**RESISTIVE** REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING **SWITCHING** +125 1000 MTP8P10 ±100μF 150Ω 1μF CIRCUIT 3W )MTP8P10( 3W MUR8100E  $R_{c}$ /clamp=300\ MPF93 MUR105 SCOPE MJE210 R<sub>B2</sub> **TEST** 5.1k 500Ω 150Ω D1 🛦 COMMON -**⊘** V<sub>CE</sub> 3W MTP12N10 500μF ₹51 Voff o 1üF **CIRCUIT VALUES** Inductive  $BV_{\text{CEO (SUS)}}$ **RBSOA** Switching I =10mH L=20mH L=500mH V<sub>CC</sub>=125V R<sub>B2</sub>=0 R<sub>B2</sub>=8 R<sub>B2</sub>=0  $R_C=25\Omega$ V<sub>CC</sub>=15Volts V<sub>CC</sub>=20V  $V_{CC}=15V$ D1=1N5820 OR EQUIV R<sub>B1</sub> selected  $I_{C(PK)}=100mA$ R<sub>B1</sub> selected for desired I<sub>R1</sub> for desired I<sub>B1</sub> t<sub>F</sub> CLAMPED TYPICAL l<sub>C</sub> ♠ t<sub>F</sub> UNCLAMPEDI t2 t1 ADJUSTED TO 25µs WAVEFORMS OBTAIN IC  $Lcoil(I_{CM})$ V<sub>CE</sub> PEAK  $V_{CC}$ Lcoil(I<sub>CM</sub>) t2 ≤ VCLAME t<sub>F</sub>  $V_{\text{CE}}$ Test Equipment Scope-Tektronix t<sub>r</sub>, t<sub>f</sub><10ns 475 or Equivalent DUTY CYCLE=1.0% V<sub>CLAME</sub> RB AND RC ADJUSTED

Table 1. Test Conditions for Dynamic Performance

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