

2N5193 thru 2N5195 (SILICON) MJE5193 thru MJE5195

SILICON PNP POWER TRANSISTORS

... for use in power amplifier and switching circuits, — excellent safe area limits. Complement to NPN 2N5190, 2N5191, 2N5192 and MJE5190, MJE5191, MJE5192.

*MAXIMUM RATINGS

Rating	Symbol	2N5193 MJE5193	2N5194 MJE5194	2N5195 MJE5195	Unit
Collector-Emitter Voltage	V _{CEO}	40	60	80	V _{dc}
Collector-Base Voltage	V _{CB}	40	60	80	V _{dc}
Emitter-Base Voltage	V _{EB}	5.0			V _{dc}
Collector Current	I _C	4.0			A _{dc}
Base Current	I _B	1.0			A _{dc}
Total Device Dissipation @ T _C = 25°C Derate above 25°C	P _D	2N5193 Series	MJE5193 Series		Watts mW/°C
		40 320	60 480		
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-65 to +150			°C/W

THERMAL CHARACTERISTICS

Characteristic	Symbol	2N5193 Series	MJE5193 Series	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3 12	2.08	°C/W

*ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage (1) ($I_C = 0.1 \text{ Adc}, I_B = 0$)	$V_{CEO(sus)}$	2N5193, MJE5193 2N5194, MJE5194 2N5195, MJE5195	40 60 80	— — —	Vdc
Collector Cutoff Current ($V_{CE} = 40 \text{ Vdc}, I_B = 0$) ($V_{CE} = 60 \text{ Vdc}, I_B = 0$) ($V_{CE} = 80 \text{ Vdc}, I_B = 0$)	I_{CEO}	2N5193, MJE5193 2N5194, MJE5194 2N5195, MJE5195	— — —	1.0 1.0 1.0	mA
Collector Cutoff Current ($V_{CE} = 40 \text{ Vdc}, V_{BE(off)} = 1.5 \text{ Vdc}$) 2N5193, MJE5193 ($V_{CE} = 60 \text{ Vdc}, V_{BE(off)} = 1.5 \text{ Vdc}$) 2N5194, MJE5194 ($V_{CE} = 80 \text{ Vdc}, V_{BE(off)} = 1.5 \text{ Vdc}$) 2N5195, MJE5195 ($V_{CE} = 40 \text{ Vdc}, V_{BE(off)} = 1.5 \text{ Vdc}$) 2N5193, MJE5193 $T_C = 125^\circ\text{C}$ ($V_{CE} = 60 \text{ Vdc}, V_{BE(off)} = 1.5 \text{ Vdc}$) 2N5194, MJE5194 $T_C = 125^\circ\text{C}$ ($V_{CE} = 80 \text{ Vdc}, V_{BE(off)} = 1.5 \text{ Vdc}$) 2N5195, MJE5195 $T_C = 125^\circ\text{C}$	I_{CEX}	2N5193, MJE5193 2N5194, MJE5194 2N5195, MJE5195 2N5193, MJE5193 2N5194, MJE5194 2N5195, MJE5195	— — — — — —	0.1 0.1 0.1 2.0 2.0 2.0	mA
Collector Cutoff Current ($V_{CB} = 40 \text{ Vdc}, I_E = 0$) ($V_{CB} = 60 \text{ Vdc}, I_E = 0$) ($V_{CB} = 80 \text{ Vdc}, I_E = 0$)	I_{CBO}	2N5193, MJE5193 2N5194, MJE5194 2N5195, MJE5195	— — —	0.1 0.1 0.1	mA
Emitter Cutoff Current ($V_{BE} = 5.0 \text{ Vdc}, I_C = 0$)	I_{EBO}	2N5193, MJE5193 2N5194, MJE5194 2N5195, MJE5195	— — —	1.0	mA

ON CHARACTERISTICS

DC Current Gain (1) ($I_C = 1.5 \text{ Adc}, V_{CE} = 2.0 \text{ Vdc}$) ($I_C = 4.0 \text{ Adc}, V_{CE} = 2.0 \text{ Vdc}$)	h_{FE}	2N5193, MJE5193, 2N5194, MJE5194, 2N5195, MJE5195 2N5193, MJE5193, 2N5194, MJE5194, 2N5195, MJE5195	25 20 10 7.0	100 80 — —	—
Collector-Emitter Saturation Voltage (1) ($I_C = 1.5 \text{ Adc}, I_B = 0.15 \text{ Adc}$) ($I_C = 4.0 \text{ Adc}, I_B = 1.0 \text{ Adc}$)	$V_{CE(sat)}$	2N5193, MJE5193 2N5194, MJE5194 2N5195, MJE5195	— — —	0.6 1.2	Vdc
Base-Emitter On Voltage (1) ($I_C = 1.5 \text{ Adc}, V_{CE} = 2.0 \text{ Vdc}$)	$V_{BE(on)}$	2N5193, MJE5193 2N5194, MJE5194 2N5195, MJE5195	— — —	1.2	Vdc

DYNAMIC CHARACTERISTICS

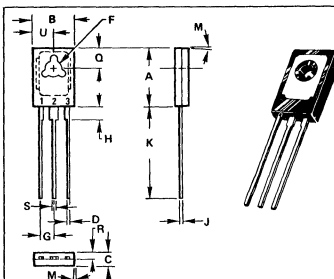
Current-Gain-Bandwidth Product ($I_C = 1.0 \text{ Adc}, V_{CE} = 10 \text{ Vdc}, f = 1.0 \text{ MHz}$)	f_T	2.0	—	MHz
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*Indicates JEDEC Registered Data for 2N5193 Series.

(1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

4 AMPERE POWER TRANSISTORS SILICON PNP

40-80 VOLTS
40 and 60 WATTS

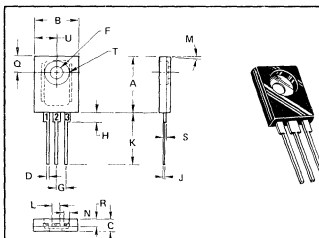


STYLE 1
PIN 1 EMITTER
2. COLLECTOR
3. BASE

2N5193
2N5194
2N5195

CASE 77-03

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.00	0.115	0.118
G	2.36	2.50	0.093	0.095
H	2.18	2.41	0.085	0.095
J	0.38	0.64	0.015	0.025
K	15.38	16.64	0.605	0.655
M	30 TYP	30 TYP		
N	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.88	3.94	0.145	0.155



STYLE 1
PIN 1 BASE
2. COLLECTOR
3. EMITTER

MJE5193
MJE5194
MJE5195

CASE 199-04

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	16.08	16.33	0.633	0.643
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	0.51	0.76	0.020	0.030
F	3.61	3.66	0.142	0.145
G	2.54	2.54	0.100	0.100
H	2.67	2.92	0.105	0.115
J	0.43	0.68	0.017	0.027
K	14.73	14.99	0.580	0.590
L	2.18	2.41	0.085	0.095
M	30 TYP	30 TYP		
N	1.47	1.73	0.058	0.068
Q	4.78	5.03	0.188	0.198
R	1.91	2.16	0.075	0.085
S	0.81	0.86	0.032	0.034
T	6.89	7.24	0.275	0.285
U	6.22	6.48	0.245	0.255

NOTES
1. DIM "G" IS TO CENTER OF LEADS

FIGURE 1 – DC CURRENT GAIN

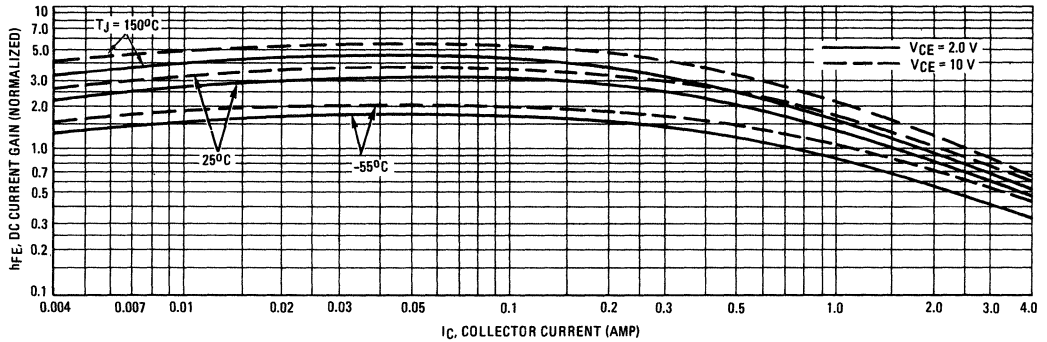


FIGURE 2 – COLLECTOR SATURATION REGION

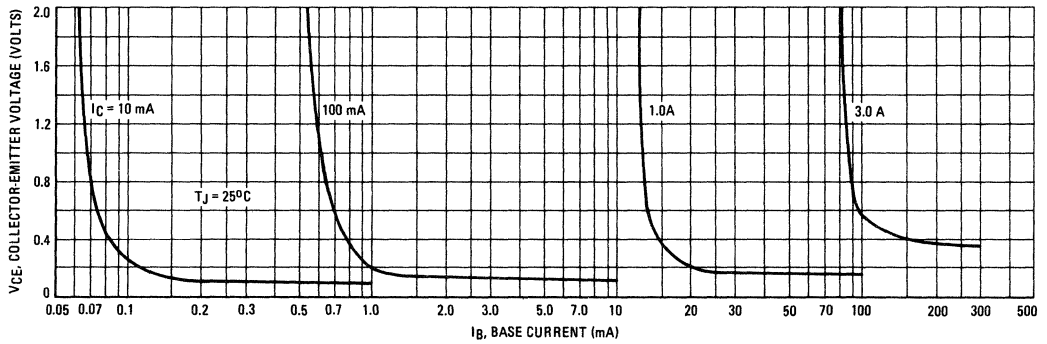


FIGURE 3 – "ON" VOLTAGE

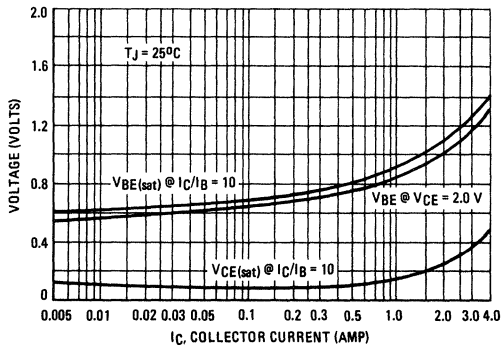


FIGURE 4 – TEMPERATURE COEFFICIENTS

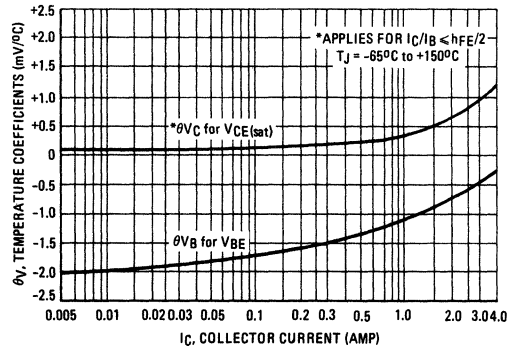


FIGURE 5 – COLLECTOR CUT-OFF REGION

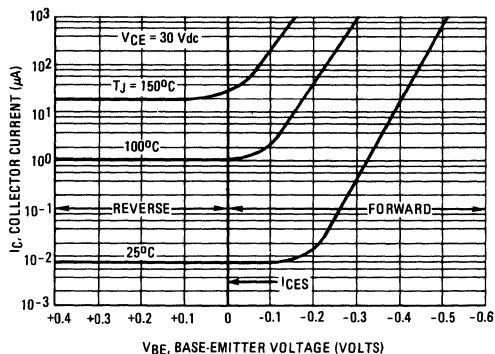


FIGURE 6 – EFFECTS OF BASE-EMITTER RESISTANCE

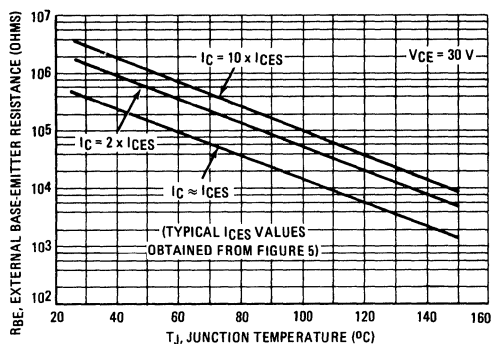


FIGURE 7 – SWITCHING TIME EQUIVALENT CIRCUIT

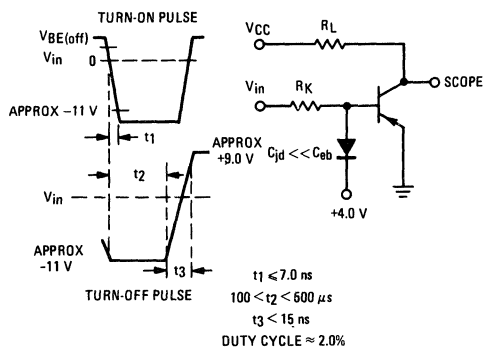


FIGURE 8 – CAPACITANCE

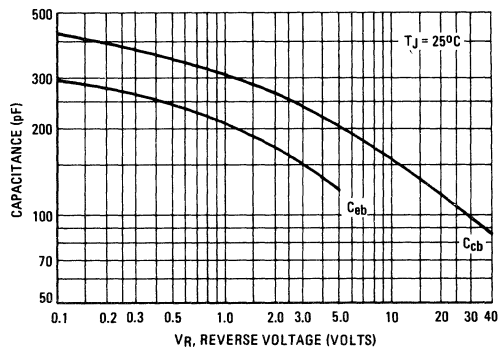


FIGURE 9 – TURN-ON TIME

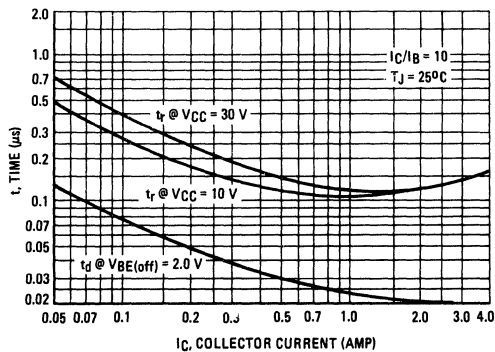
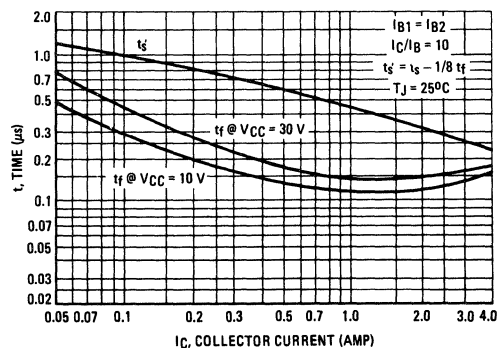
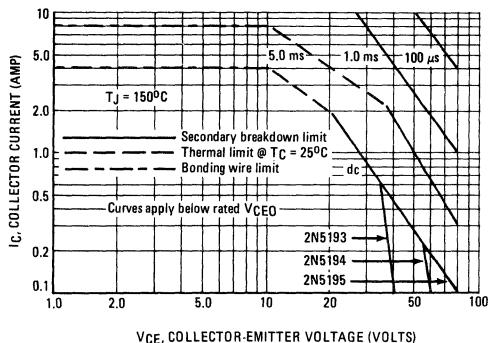


FIGURE 10 – TURN-OFF TIME



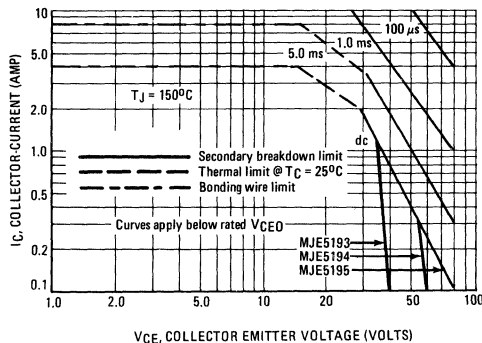
RATING AND THERMAL DATA ACTIVE-REGION SAFE OPERATING AREA

FIGURE 11 – 2N5193, 2N5194, 2N5195

**Note 1:**

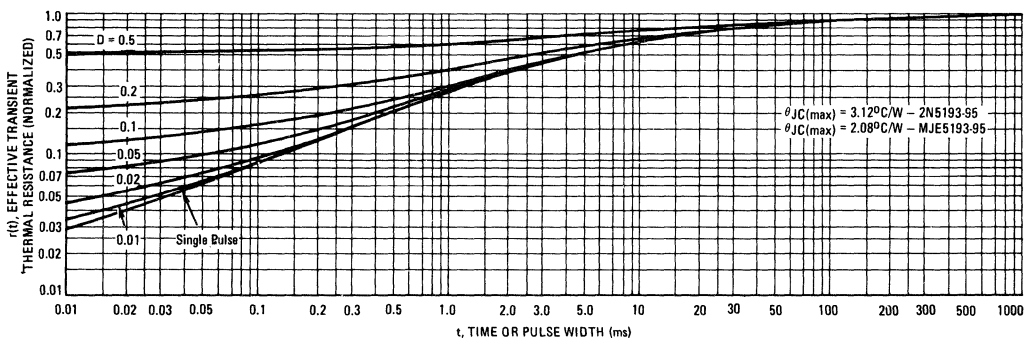
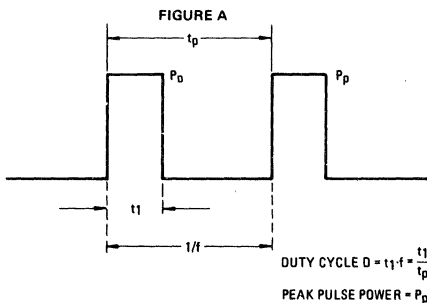
There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

FIGURE 12 – MJE5193, MJE5194, MJE5195



The data of Figures 11 and 12 is based on $T_J(pk) = 150^\circ C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_J(pk) \leq 150^\circ C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

FIGURE 13 – THERMAL RESPONSE

**DESIGN NOTE: USE OF TRANSIENT THERMAL RESISTANCE DATA**

A train of periodical power pulses can be represented by the model shown in Figure A. Using the model and the device thermal response, the normalized effective transient thermal resistance of Figure 13 was calculated for various duty cycles.

To find $\theta_{JC}(t)$, multiply the value obtained from Figure 13 by the steady state value θ_{JC} .

Example:

The 2N5193 is dissipating 50 watts under the following conditions: $t_1 = 0.1$ ms, $t_p = 0.5$ ms. ($D = 0.2$).

Using Figure 13, at a pulse width of 0.1 ms and $D = 0.2$, the reading of $r(t_1, D)$ is 0.27.

The peak rise in junction temperature is therefore:

$$\Delta T = r(t) \times P_p \times \theta_{JC} = 0.27 \times 50 \times 3.12 = 42.2^\circ C$$