400W, 28V High Power RF LDMOS FETs

Description

The MK0540 is a 400-watt, highly rugged, unmatched LDMOS FET, designed for wide-band commercial and industrial applications with frequencies HF to 500MHz. It can be used in Class AB/B and Class C for all typical modulation formats.

•Typical Performance (On Innogration fixture with device soldered):

 $V_{DD} = 28 \text{ Volts}$, $I_{DQ} = 2000 \text{ mA}$, CW.

Freq(MHz)	G _P (dB)	P _{-1dB} (W)	Eff(%)		
500	17	380	60		

•Typical Performance (On Innogration fixture with device soldered):

VDD = 28 Volts, IDQ = 1.2 A, Two tone space 5MHz.

Freq(MHz)	G _P (dB)	Pouт(W)	Eff(%)	IMD3(dBc)
225	21	79	29	-25
300	19.3	89	28	-35
400	16.9	87	31	-39
500	17.2	89	43	-28

• Typical Performance (On Innogration fixture with device soldered):

 V_{DD} = 28 Volts, I_{DQ} = 1.3 A, Two tone space 1MHz.

Freq(MHz)	G _P (dB)	P _{OUT} (W)	Eff(%)	IMD3(dBc)
310	19	100	30	-32
330	20	100	30	-32
360	19.5	100	31	-34
390	18.7	100	33	-36
410	17.2	100	35	-36

Figure 1. Pin Connection

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift

- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 2-30MHz (HF or Short wave communication)
- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 118 -140MHz (Avionics)

- 136-174MHz (Commercial ground communication)
- 160-230MHz (TV VHF III)
- 30-512MHz (Jammer, Ground/Air communication)
- 470-860MHz (TV UHF)
- 100kHz 1000MHz (ISM, instrumentation)

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
DrainSource Voltage	$V_{\scriptscriptstyle DSS}$	+95	Vdc

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GateSource Voltage	$V_{\sf GS}$	-10 to +10	Vdc
Operating Voltage	V_{DD}	+40	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T _c	+150	°C
Operating Junction Temperature	TJ	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case	Rejc	0.3	°C/W
T _C = 85°C, T _J =200°C, DC test	KAJC	0.3	C/VV

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22A114)	Class 2

Table 4. Electrical Characteristics ($T_A = 25$ °C unless otherwise noted)

Characteristic	Symbol	Min	Тур	Max	Unit
DC Characteristics (per half section)					
Drain-Source Voltage	$V_{(BR)DSS}$	95	98		V
V _{GS} =0, I _{DS} =1.0mA	V (BR)DSS	93	90		V
Zero Gate Voltage Drain Leakage Current				1	^
$(V_{DS} = 75V, V_{GS} = 0 V)$	I _{DSS}		 -	ı	μΑ
Zero Gate Voltage Drain Leakage Current				1	^
$(V_{DS} = 28 \text{ V}, V_{GS} = 0 \text{ V})$	DSS			ı	μΑ
GateSource Leakage Current				1	4
$(V_{GS} = 10, V_{DS} = 0 V)$	I _{GSS}	<u> </u>	<u> </u>		μΑ
Gate Threshold Voltage	\/ (4b)		2.19		V
$(V_{DS} = 28V, I_D = 650 \mu A)$	$V_{GS}(th)$		2.19		V
Gate Quiescent Voltage	V		2.0		V
(V _{DD} = 28 V, I _D = 1.0 A, Measured in Functional Test)	$V_{GS(Q)}$	<u>——</u>	3.0	<u> </u>	V
Common Source Input Capacitance	0		187		۲
$(V_{GS} = 0V, V_{DS} = 28 V, f = 1 MHz)$	C _{ISS}		107		pF
Common Source Output Capacitance			70		۲
(V _{GS} = 0V, V _{DS} =28 V, f = 1 MHz)	Coss		79		pF
Common Source Feedback Capacitance			4.0		
$(V_{GS} = 0V, V_{DS} = 28 V, f = 1 MHz)$	C _{RSS}		4.6		pF

Functional Tests (In Demo Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 2000 mA, f = 500 MHz, CW Signal Measurements.

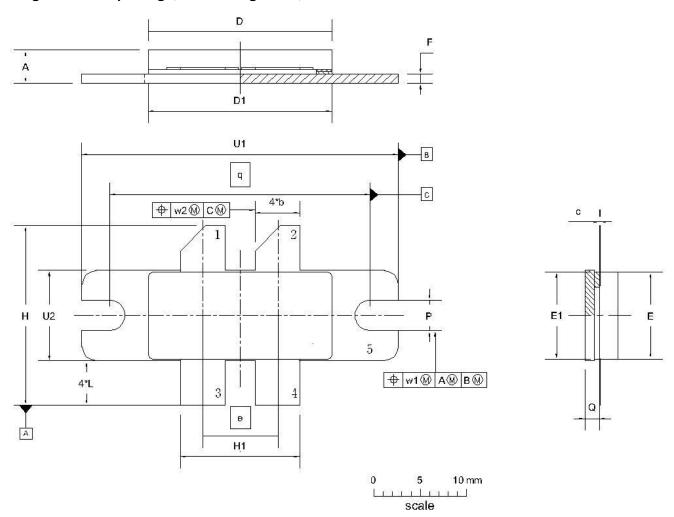
Power Gain	Gp	 17		dB
Drain Efficiency@P1dB	$\eta_{\scriptscriptstyle D}$	 60		%
1 dB Compression Point	P _{-1dB}	 380	——	W
Input Return Loss	IRL	 -7		dB

Load Mismatch (In Innogration Test Fixture, 50 ohm system): $V_{DD} = 28 \text{ Vdc}$, $I_{DQ} = 2000 \text{ mA}$, f = 500 MHz

VSWR 20:1 at 380W pulse CW Output Power	No Device Degradation
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Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads



UNIT	A	b	С	D	D_1	e	E	E ₁	F	Н	H1	L	p	Q	q	U ₁	U_2	W_1	W_2
mm	4.72 3.43	3.94 3.68	0.15 0.08	20.02 19.61	19.96 19.66	8.89	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	12.83 12.57	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.155 0.145	0.006 0.003	0.788 0.772	0.786 0.774	0.35	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.505 0.495	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE		REFERENCE		EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA	PROJECTION	IOOOE DATE
PKG-B4E					03/12/2013

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Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2017/2/22	Rev 1.0	Preliminary Datasheet
2017/3/17	Rev 2.0	Product Datasheet
2017/3/17	Rev 3.0	Modification on typo of upper frequency from 1000MHz to 500MHz

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