

MK0560VPX LDMOS TRANSISTOR

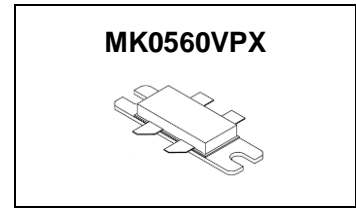
Document Number: MK0560VPX
Preliminary Datasheet V1.0

600W, 50V High Power RF LDMOS FETs

Description

The MK0560VPX is a 600-watt capable, high performance, unmatched LDMOS FET, designed for wide-band commercial and industrial applications with frequencies HF to 0.5 GHz.

It is featured for high power and high ruggedness, suitable for Industrial, Scientific and Medical application, as well as FM radio, VHF TV and Aerospace applications.



- Typical performance(on 1.6-30MHz wideband test board with device soldered)

Signal: pulse CW, pulse width:100us, duty cycle:10%,Vgs=3.25V,Vds=50V,Idq=100mA

Freq(MHz)	Pin(dBm)	Psat(dBm)	Psat(W)	IDS(A)	Gain(dB)	η (%)
1.6	29	56.8	479	1.63	27.8	62
5	27	56.9	490	1.488	29.9	70
10	26.6	56.7	468	1.436	30.1	70
15	29.6	56.7	468	1.416	27.1	71
20	33.2	56.9	490	1.455	23.7	72
25	33.1	56.7	468	1.449	23.6	69
30	32.8	56.7	468	1.47	23.9	68

Signal: CW Vgs=3.25V,Vds=50V, Idq=100mA

Freq(MHz)	Pin(dBm)	Psat(dBm)	Psat(W)	IDS(A)	Gain(dB)	η (%)
10	29.7	56.9	490	13.6	27.2	72
20	33.6	56.8	479	13.4	23.2	71
30	34.8	56.8	479	13.7	22	70

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 160-230MHz (TV VHF III)
- 136-174MHz (Commercial ground communication)
- Laser Exciter
- Synchrotron
- MRI
- Plasma generator
- Weather Radar

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+125	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc

MK0560VPX LDMOS TRANSISTOR

Document Number: MK0560VPX
Preliminary Datasheet V1.0

Storage Temperature Range	T _{stg}	-65 to +150	°C
Case Operating Temperature	T _c	+150	°C
Operating Junction Temperature	T _j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T _c = 85°C, T _j =200°C, DC test	R _{θJC}	0.35	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (T_A = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

DC Characteristics (per half section)

Drain-Source Voltage V _{GS} =0, I _{DS} =1.0Ma	V _{(BR)DSS}		125		V
Zero Gate Voltage Drain Leakage Current (V _{DS} = 75V, V _{GS} = 0 V)	I _{DSS}	—	—	1	μA
Zero Gate Voltage Drain Leakage Current (V _{DS} = 50 V, V _{GS} = 0 V)	I _{DSS}	—	—	1	μA
Gate--Source Leakage Current (V _{GS} = 10 V, V _{DS} = 0 V)	I _{GSS}	—	—	1	μA
Gate Threshold Voltage (V _{DS} = 50V, I _D = 600 μA)	V _{GS(th)}	—	2.65	—	V
Gate Quiescent Voltage (V _{DD} = 50 V, I _D = 100 mA, Measured in Functional Test)	V _{GS(Q)}	—	3.25	—	V
Common Source Input Capacitance (V _{GS} = 0V, V _{DS} =50 V, f = 1 MHz)	C _{ISS}		TBD		pF
Common Source Output Capacitance (V _{GS} = 0V, V _{DS} =50 V, f = 1 MHz)	C _{OSS}		TBD		pF
Common Source Feedback Capacitance (V _{GS} = 0V, V _{DS} =50 V, f = 1 MHz)	C _{RSS}		TBD		pF

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 55 Vdc, I_{DQ} = 100 mA, f = 15MHz, pulse width:100us, duty cycle:20%

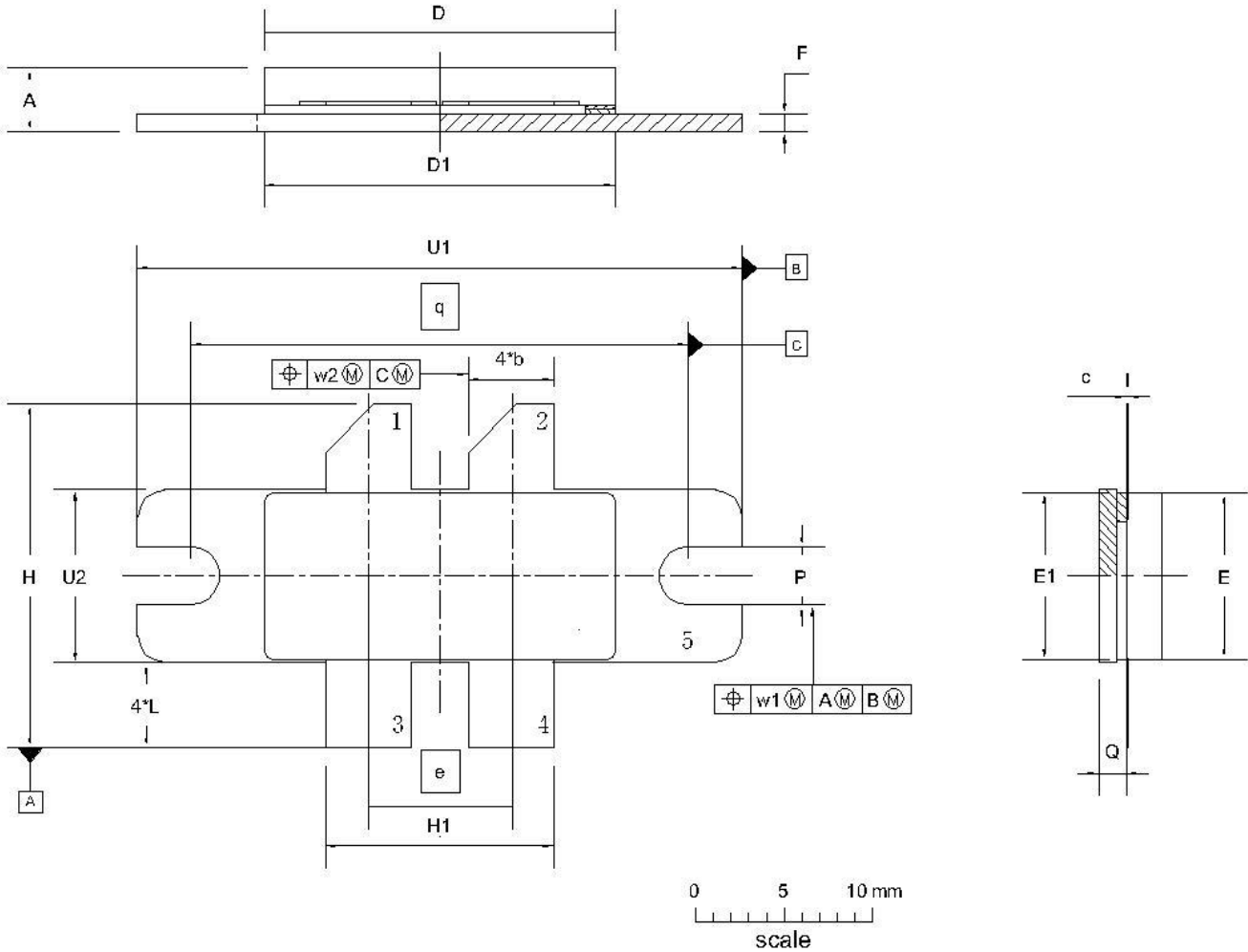
Load open, at 500W Pulsed CW Output Power	No Device Degradation
---	-----------------------

MK0560VPX LDMOS TRANSISTOR

Document Number: MK0560VPX
Preliminary Datasheet V1.0

Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads



UNIT	A	b	C	D	D ₁	e	E	E ₁	F	H	H ₁	L	p	Q	q	U ₁	U ₂	W ₁	W ₂
mm	4.72	3.94	0.15	20.02	19.96	8.89	9.50	9.53	1.14	19.94	12.83	5.33	3.38	1.70	27.94	34.16	9.91	0.25	0.51
	3.43	3.68	0.08	19.61	19.66		9.30	9.25	0.89	18.92	12.57	4.32	3.12	1.45		33.91	9.65		
inches	0.186	0.155	0.006	0.788	0.786	0.35	0.374	0.375	0.045	0.785	0.505	0.210	0.133	0.067	1.100	1.345	0.390	0.01	0.02
	0.135	0.145	0.003	0.772	0.774		0.366	0.364	0.035	0.745	0.495	0.170	0.123	0.057		1.335	0.380		

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B4E					03/12/2013

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2018/3/28	Rev 1.0	Preliminary Datasheet Creation

Disclaimers

Specifications are subject to change without notice. Innogration believes the information contained within this data sheet to be accurate and reliable. However, no responsibility is assumed by Innogration for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Innogration . Innogration makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose. "Typical" parameters are the average values expected by Innogration in large quantities and are provided for information purposes only. These values can and do vary in different applications and actual performance can vary over time. All operating parameters should be validated by customer's technical experts for each application. Innogration products are not designed, intended or authorized for use as components in applications intended for surgical implant into the body or to support or sustain life, in applications in which the failure of the Innogration product could result in personal injury or death or in applications for planning, construction, maintenance or direct operation of a nuclear facility. For any concerns or questions related to terms or conditions, pls check with Innogration and authorized distributors

Copyright © by Innogration (Suzhou) Co.,Ltd.