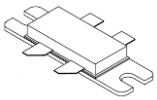
MK1040VP LDMOS TRANSISTOR

Document Number: MK1040VP
Preliminary Datasheet V1.0

400W, 50V High Power RF LDMOS FETs

MK1040VP



Description

The MK1040VP is a 400-watt, high performance, internally matched LDMOS FET, designed for wide-band commercial and industrial applications with frequencies 0.5 to 1GHz.

It is featured for high power and high ruggedness, suitable for Industrial, Scientific and Medical application, as well as UHF TV and Aerospace applications.

- Typical performance(on 0.5-1GHz wideband test board with device soldered)

Signal：pulse CW, pulse width:100us，duty cycle:10%,Vgs=2.99V,Vds=50V,Idq=120mA

Freq(MHz)	Pin(dBm)	Psat(dBm)	Psat(W)	IDS(A)	Gain(dB)	η(%)
500	43.2	57.4	550	2.36	14.2	47%
600	41.2	57.8	603	1.89	16.6	64%
700	41.7	56.5	447	1.58	14.8	57%
800	40.7	56.1	407	1.89	15.4	43%
900	40.8	56.7	468	2.067	15.9	45%
1000	40.5	56	400	1.44	15.5	56%

- Typical performance(on 915MHz narrow band test board with device soldered)

Vgs=2.97V,Vds=50V, Idq=100mA Frequency 915MHz

Signal	Pin(dBm)	Psat(dBm)	Psat(W)	IDS(A)	Gain(dB)	η(%)
10% 100us	39.5	57.3	537	1.8	17.8	60%
20% 100us	40.1	57.4	550	1.89	17.3	58.5%
20% 1ms	40.1	57	500	3.55	16.9	56.5%

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+125	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit

Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	0.35	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (T_A = 25 ℃ unless otherwise noted)

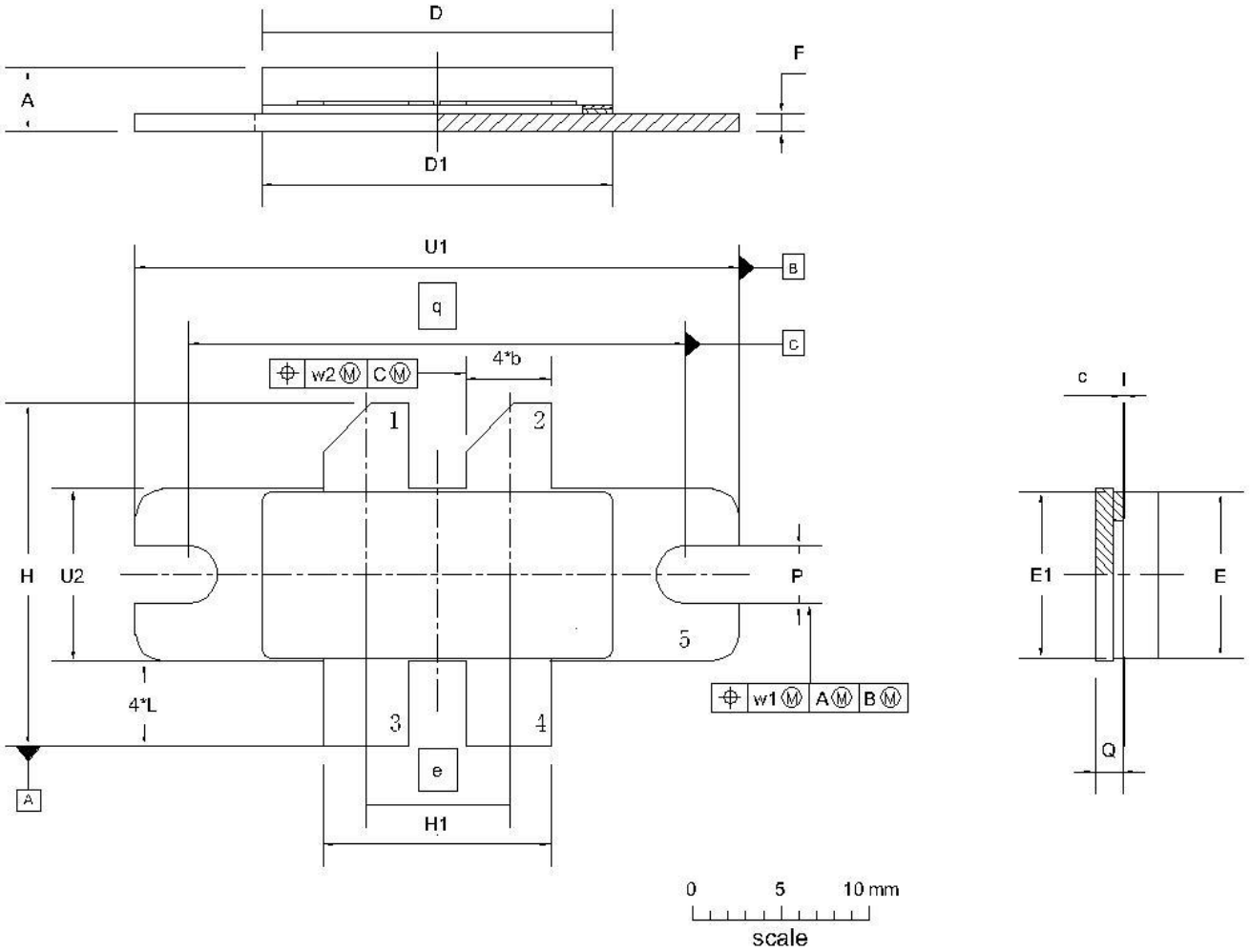
Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics (per half section)					
Drain-Source Voltage V_{GS}=0, I_{DS}=1.0mA	$V_{(BR)DSS}$		125		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50 V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 μA)	V_{GS}(th)	——	2.65	——	V
Gate Quiescent Voltage (V_{DD} = 50 V, I_D = 100 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3.25	——	V

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 50 Vdc, I_{DQ} = 100 mA, f = 915MHz, pulse width:100us, duty cycle:20%

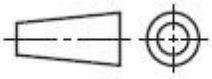
VSWR 10:1, at 500W Pulsed CW Output Power	No Device Degradation

Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads



UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H1	L	p	Q	q	U_1	U_2	W_1	W_2
mm	4.72 3.43	3.94 3.68	0.15 0.08	20.02 19.61	19.96 19.66	8.89	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	12.83 12.57	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.155 0.145	0.006 0.003	0.788 0.772	0.786 0.774	0.35	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.505 0.495	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B4E					03/12/2013

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2017/6/27	Rev 1.0	Preliminary Datasheet Creation

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