MK1160VP LDMOS TRANSISTOR

Document Number: MK1160VP
Preliminary Datasheet V1.0

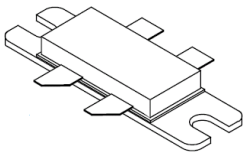
1000-1100MHz, 50V, 600W, RF Power LDMOS Transistor

Description

The MK1160VP is a 600-watt, internally matched LDMOS FETs, designed for civilian pulsed avionics amplifier applications with frequencies from 1000 MHz to 1100 MHz.

There is no guarantee of performance when this part is used in applications designed outside of these frequencies.

MK1160VP



- Typical Performance(On Innogration fixture with device soldered):

V_{DD} = 50 Volts, I_{DQ} = 100 mA, Pulse CW, Pulse Width=10 us, Duty cycle=10% .

Frequency	Gain(dB)	P_{3dB} (W)	η_D@P_{3dB} (%)
1030 MHz	13.9	700	46.5
1060 MHz	14.3	680	48.6
1090 MHz	14.5	664	50.7

Note: This device is only used as single-ended device.

Applications and Features

- Avionics: Mode-S, TCAS,JTIDS,DME and TACAN
- Thermally Enhanced Industry Standard Package
- High Reliability Metallization Process
- Excellent thermal Stability and Excellent Ruggedness
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+110	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+54	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case Case Temperature 80℃, 600 W Pulsed, 100uS Pulse Width, 10% Duty Cycle	RθJC	0.07	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit

DC Characteristics

Zero Gate Voltage Drain Leakage Current (V_{DS} = 115V, V_{GS} = 0 V)	I_{DSS}			100	μA
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50 V, V_{GS} = 0 V)	I_{DSS}			10	μA
Gate--Source Leakage Current (V_{GS} = 6 V, V_{DS} = 0 V)	I_{GSS}			10	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 μA)	$V_{GS}(th)$		2.25		V
Gate Quiescent Voltage (V_{DD} = 50 V, I_D = 100 mA, Measured in Functional Test)	$V_{GS(Q)}$		2.8		V

Functional Tests (On Innogration Test Fixture, 50 ohm system) : V_{DD} = 50 Vdc, I_{DQ} = 100 mA, f = 1090 MHz, Pulsed CW, Pulse Width=10us, Duty cycle=10% .

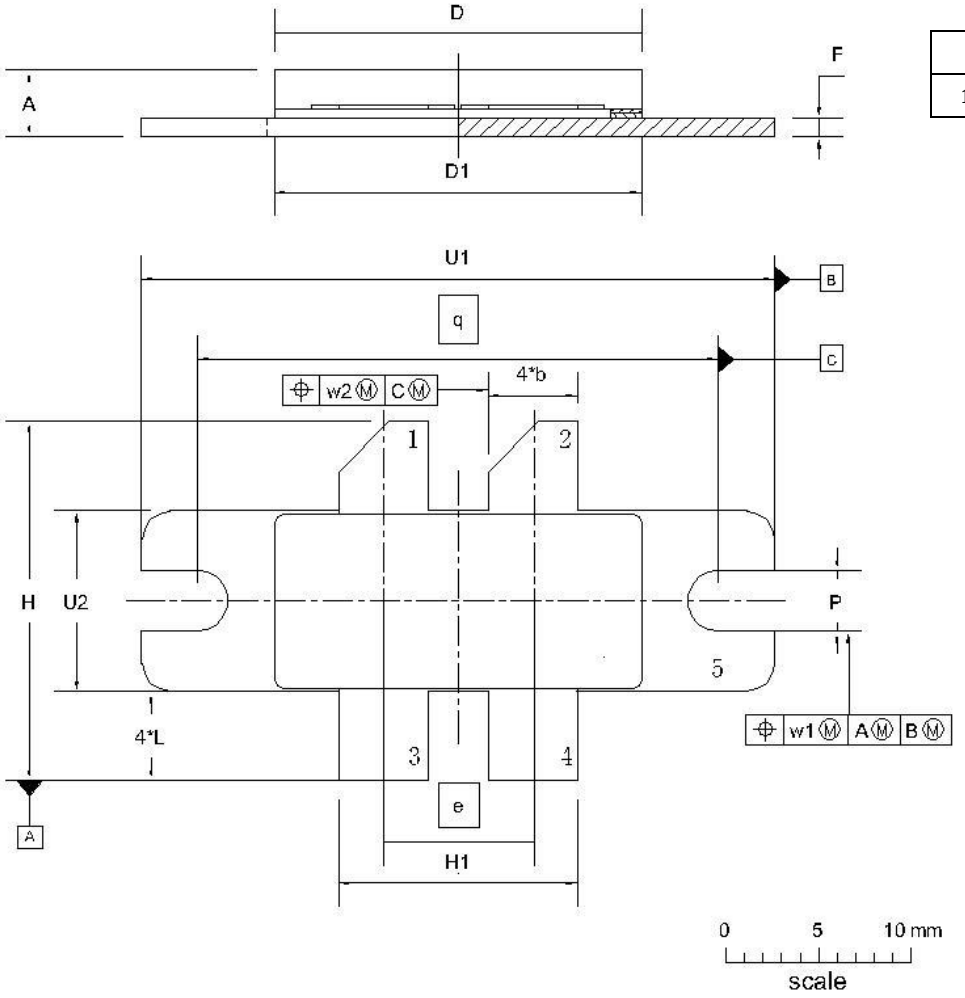
Characteristic	Symbol	Min	Typ	Max	Unit
Max Gain	Gp		14.5		dB
3dB Compression Point	P_{3dB}		664		W
Drain Efficiency	η_D		50.7		%
Input Return Loss	IRL		-7		dB

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 50 Vdc, I_{DQ} = 100 mA, f = 1090MHz

VSWR 10:1 at 600W Pulsed CW Output Power	No Device Degradation

Package Outline

Eared Flanged Ceramic Package; 2 mounting holes; 4 leads



Drain		Gate		Source
1	2	3	4	5

UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H1	L	p	Q	q	U_1	U_2	W_1	W_2
mm	4.72 3.43	4.93 4.67	0.15 0.08	20.02 19.61	19.96 19.66	7.90	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	12.98 12.73	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.194 0.184	0.006 0.003	0.788 0.772	0.786 0.774	0.311	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.511 0.501	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B4E					03/12/2013

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2017/7/27	Rev 1.0	Preliminary Datasheet

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